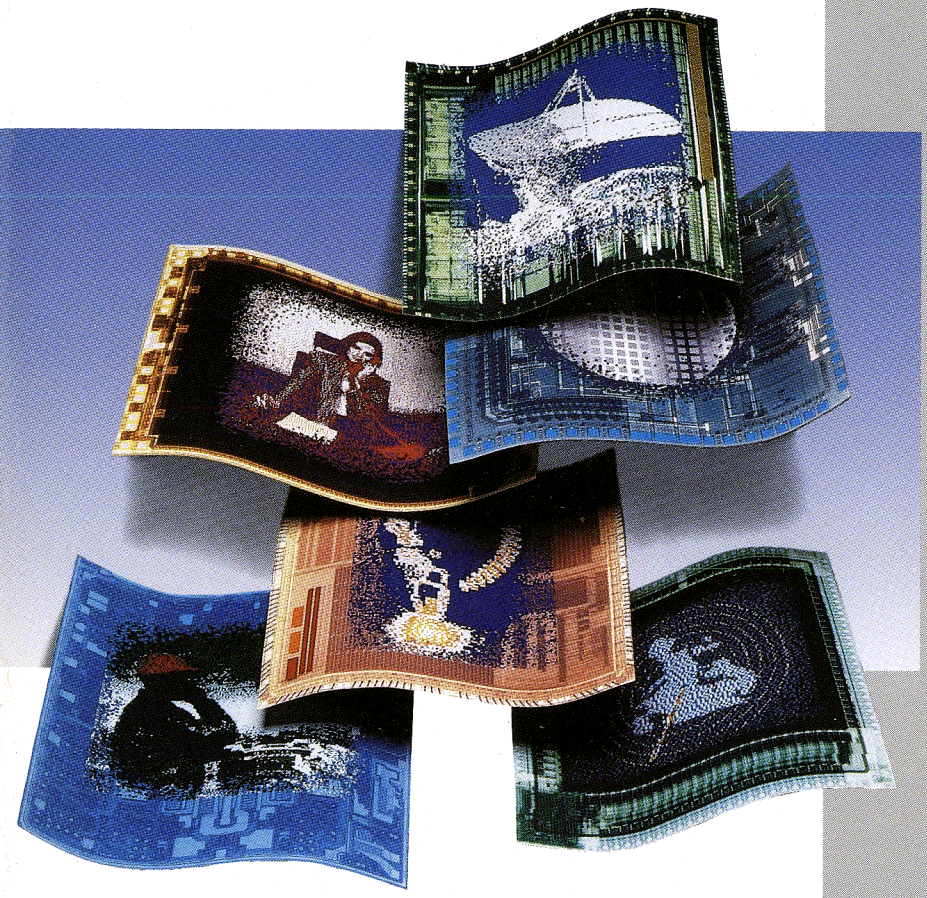
Consumer

IC Handbook

September 1991



GEC PLESSEY

SEMICONDUCTORS

CONSUMER
IC Handbook

GEC PLESSEY
SEMICONDUCTORS

Foreword

GEC Plessey Semiconductors offers over 100 integrated circuits for a wide range of applications in consumer electronic equipment.

For Satellite/Cable/TV, the **SP4000** series of high speed dividers are specifically designed for use in frequency synthesised tuning systems – featuring low current, low radiation, ECL/TTL outputs and operating frequencies up to 2.5GHz. The **SP5000** series comprises frequency synthesisers for TV, VCR, Cable and Satellite applications. For the TV/VCR market, both 3-wire and I^2C types of addressing are catered for – the **SP5020/5021/5024** and **5026** for 3-wire and the **SP5510/5511/5512** and **5514** for I^2C. For the satellite market, again, both types of addressing are offered – the **SP5055/5066** for I^2C and the **SP5054** for 3-wire. For fixed frequency applications, as in Cable TV, the **SP5011** is available, together the latest synthesiser from GPS: the **SP5070**, which operates up to 2.4GHz.

The **MV1815** is a single-chip Teletext decoder incorporating on-chip data slicer, dual acquisition circuitry and RGB logic. Using the MV1815, a completeTeletext system can be built with just the addition of a single DRAM.

For **DBS TV signal decoding (MAC)**, GPS offers a comprehensive range of video, sound and control chips, a Teletext interface circuit and a signal input processor/data recovery circuit. These are supported by a range of high performance video graphics products which includes the **VP101** 30/50MHz triple 8-bit video DAC and the **ZN454E** triple 4-bit video DAC with an update rate of 100MHz and linearity error of 0.25 LSB.

In TV and video systems, the **ZNA134** can be used to generate all horizontal, vertical, mixed blanking and synchronising pulses necessary for raster generation in either 625 or 525 line systems. The ZNA234 generates cross hatch, dot and grey scale television test patterns.

MA818/828 is a new family of PWM waveform generator chips, designed for digital motor speed control and uninterruptible power supply applications.

Add to these the GPS range of remote control devices, precision timers and display drivers also detailed in this handbook and you have an impressive catalogue of integrated circuits, tailor-made to satisfy the requirements of the most demanding areas of consumer product design.

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High Speed Dividers

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SP4362	÷ 64, VHF/UHF, high sensitivity, ECL O/P	5	1	Bipolar	1-3
SP4633	÷ 64, non self-oscillating, high sensitivity, ECL O/P, ESD protection on-chip	5	1	Bipolar	1-6
SP4653	÷ 256, VHF/UHF, high sensitivity, ECL O/P	5	1	Bipolar	1-9
SP4660	÷ 256, VHF/UHF, high sensitivity, ECL O/P ESD protection on-chip	5	1	Bipolar	1-12
SP4666	÷ 64/256, switchable, high sensitivity, LPF on-chip	5	1	Bipolar	1-15
SP4676	÷ 128/136, ÷ 64/68 , high sensitivity,very low power	5	950MHz	Bipolar	1-19
SP4731	÷ 64, high sensitivity, high output, ECL O/P	5	1.3	Bipolar	1-23
SP4740	÷ 256, TTL O/P	5	1.3	Bipolar	1-26
SP4751	÷ 256, high sensitivity, high output swing	5	1.3	Bipolar	1-29
SP4902	÷ 2, low power, high sensitivity	5	2.5	Bipolar	1-32
SP4904	÷ 4, low power, high sensitivity	5	2.5	Bipolar	1-35
SP4908	÷ 8 prescaler	5	2.5	Bipolar	1-38
SP4914	÷ 128 prescaler	5	2.5	Bipolar	1-41
SP4916	÷ 512 prescaler	5	2.5	Bipolar	1-44
SP4982	÷ 8192 prescaler	5	2.5	Bipolar	1-47

Satellite TV Receiver Circuits

Type No.	Function	Supply voltage (V) (typ)	IF Frequency (MHz)	Process	Page
SL1451	PLL demodulator with threshold extension	8.2	380-700	Bipolar	2-3
SL1452	Wideband FM detector	5	300-1000	Bipolar	2-5
SL1454	Wideband FM detector for low IF	5	70-150	Bipolar	2-9
SL1455	Quadrature detector with threshold extension	5	380-700	Bipolar	2-13

DBS TV Signal Decoding (MAC)

Type No.	Function	Supply voltage (typ)	Process	Page
MV1710	MAC video circuit	5V	CMOS	3-3
MV1720	MAC control circuit	5V	CMOS	3-11
MV1732	MAC sound circuit	5V	CMOS	3-23
MV1733	MAC sound circuit	5V	CMOS	3-77
MV1745	MAC Teletext interface circuit	5V	CMOS	3-32
SL1700	MAC signal input processor and data recovery circuit	10V(V_{CCA}), 5V(V_{CCD})	Bipolar	3-39

Video Graphics

Type No.	Function	Minimum clock rate (MHz)	DAC max. rise time (ns) 10% to 90%	Linearity error (LSB, typ.)	Process	Page
MV95308	8-bit video DAC	30	6.0	±0.5	CMOS	3-45
MV95338	Triple 8-bit video DAC	30	9.0	±0.3	CMOS	3-50
SP973T8	8-bit flash ADC (TTL/CMOS O/Ps)	30	-	±0.5/ ±1.0	Bipolar	3-57
VP101	Triple 8-bit video DAC	30/50	9.0	±0.3	CMOS	3-63
ZN454E	Triple 4-bit video DAC	100 (typ.)	3.0	0.25	Bipolar	3-70

TV/Cable/Satellite Tuner PLL Circuits(1)

Type No.	Function	Frequency	Page
SP5000A	Single chip frequency synthesiser with 3-wire control	1024MHz	1-50
SP5011	8-channel cable/satellite up/down converter for USA	See data	1-55
SP5020	Single chip frequency synthesiser for TV tuning	1.3GHz	1-59
SP5021	Single chip frequency synthesiser for TV tuning	1GHz	1-66
SP5024	SP5510 pin/Toshiba TD6358, TD6359 program compatible synthesiser	1.3GHz	1-73
SP5026	SP5510 pin/Toshiba TD6380, TD6382 function compatible synthesiser	1.3GHz	1-79
SP5050	PLL tuning controller for satellite receivers, 3-wire serial data bus (with pre-amp)	1.8/2GHz	1-91
SP5051	PLL tuning controller for satellite receivers, 3-wire serial data bus	1.8/2GHz	1-91
SP5054	Higher frequency version of SP5024	2.5GHz	1-96
SP5055 (2)	Higher frequency version of SP5510	2.5GHz	1-103
SP5056 (2)	Higher frequency version of SP5511	2.5GHz	1-110
SP5060	Fixed modulus frequency synthesiser for satellite receivers	2.0GHz	1-117
SP5070	Fixed modulus frequency synthesiser for satellite receivers	2.5GHz	1-121
SP5502 (2)	Bi-directional I²C bus 4 address synthesiser	1.3GHz	1-125
SP5510 (2)	Bi-directional I²C bus controlled synthesiser	1.3GHz	1-132
SP5511 (2)	Bi-directional I²C bus controlled synthesiser	1.3GHz	1-140
SP5512 (2)	Bi-directional I²C bus controlled synthesiser	1.3GHz	1-148
SP5514 (2)	As SP5510 but with SCL rate of 500kHz	1.3GHz	1-156

NOTES
1. All are bipolar ICs and operate from a single +5V supply.
2. Purchase of GEC Plessey Semiconductors' I²C components conveys a licence under the Philips I²C Patent Rights to use these components in I²C systems, provided that the systems conform to the I²C Standard Specification as defined by Philips.

Video Modulation

Type No.	Function	Frequency	Process	Page
SL5066	Video modulator	900MHz	Bipolar	1-163

Product index (continued)

Teletext and TV Signal Generators

Type No.	Function	Supply	Process	Page
MR9735	625-line video generator,6 languages (3)	+ 5V,15mA / + 12V,72mA	NMOS	4-3
MV1815	625-line single chip teletext decoder,14 languages (4)	5V	CMOS	4-15
MV1820	Video programme delivery control interface circuit	5V	CMOS	4-30
ZNA134	CCIR/EIA TV synchronising pulse generator	+ 5V,100mA	Bipolar	4-35
ZNA234E	TV pattern generator	+ 5V,135mA	Bipolar	4-43

NOTES
3. English, German, Swedish/Finnish, Danish and Italian character sets available; see page 4-3.
4. English, German, Swedish/Finnish, Italian, French (Belgian), Spanish, Czech, Polish, Romanian, Hungarian, Turkish, Serbo-Croat, Danish, American.

Remote Control

Type No.	Function	Supply voltage (V) (Typ)	Supply current (mA) (Typ)	Process	Page
MV500	32-code PPM transmitter, 3 switchable data rates	+ 3 to + 10	0.5	CMOS	4-3
MV601	32-code PPM receiver to complement MV500	+ 5V	1.4	CMOS	4-15
MV2000	Keyboard encoder and PPMtransmitter(5)	+ 9V	2.5(6)	CMOS	4-30
SL486	Infra red preamplifier	+ 10V	6	Bipolar	4-35
SL490B	32-code PPM transmitter, infra-red, ultrasonic or radio	+ 9	6	Bipolar	4-43

NOTES
5. 88key + 3-input shift decoder.
6. 0.1μA on standby.

Precision Timers and Display Circuits

Type No.	Function	Supply voltage (V) (Typ)	Supply current (mA) (Typ)	Process	Page
ZN1034	Precision counter timer	+ 5	3.5	Bipolar	7-3
ZN1036	Programmable counter timer	+ 5V	3.8	Bipolar	7-23
ZN1040	Universal count/display circuit	+ 5V	90	Bipolar	7-44
ZN1044	Programmable counter timer	+ 5V	3.8	Bipolar	7-65

PWM Waveform Generator Circuits

The GEC Plessey Semiconductors range of PWM generator chips are designed to meet all PWM waveform synthesis needs fo AC Motor Control and Uninterruptible Power Supply (UPS) applications. The devices generate fully-digital asynchronous PWM, implementing any power waveform read either from an external ROM/EPROM or from an on-chip ROM.

Full programmability via a simple micro interface (the MOTEL™ interface) allows use with any chosen power electronics. Once programmed, the devices run without intervention until parameters, for example, motor speed, need to be changed.

Useful features such as forward/reverse control, zero power frequency setting for DC injection braking, selectable minimum pulse width and underlap are also provided

Type No.	No.of phases	Power waveform storage	Standard waveform options	Power frequency range	Carrier frequency range	Package options	Page
MA818	3	External ROM/ EPROM	Any waveform, user-programmable in external ROM/EPROM	0 to 4kHz 12-bit accuracy	0 to 24kHz	DIL and Quad J-lead	6-3
MA828-1	3	On-chip ROM	$x(t) = A\ [sin\ (\omega t) + {}^1/_6\ sin\ (3\omega t)]$	0 to 4kHz 12-bit accuracy	0 to 24kHz	DIL and Small Outline	6-15
MA828-2			$x(t) = A\ sin\ (\omega t)$				
MA828-X			Any waveform to order				
MA838-1	1	On-chip ROM	$x(t) = A\ [sin\ (\omega t) + {}^1/_6\ sin\ (3\omega t)]$	0 to 4kHz 12-bit accuracy	0 to 24kHz	DIL and Small Outline	6-27
MA838-2			$x(t) = A\ sin\ (\omega t)$				
MA838-X			Any waveform to order				

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Section 1

High Speed Dividers
TV/Cable/Satellite Tuner PLLs

3057-1.0

SP4632

1GHz ÷ 64 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4632 ÷64 prescaler is one of GPS' range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4632 incorporates an on-chip preamplifier with differential inputs and has a balanced ECL outputs.

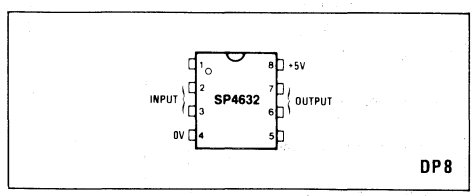


Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs

ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C
Operating temperature range	0°C to +80°C

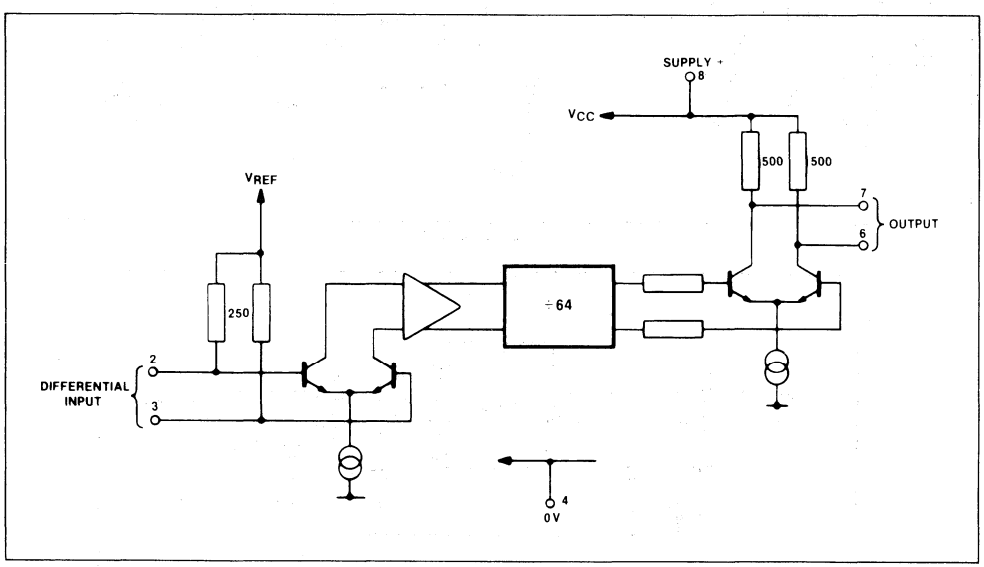


Fig.2 SP4632 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		25	35	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave (50 ohms system)
80MHz			8	17.5	mV	
150MHz			4	10	mV	
300MHz			3	10	mV	
500MHz			3	10	mV	
700MHz			3	10	mV	
900MHz			4	10	mV	
1GHz			6	17.5	mV	
Input overload	2,3	200			mV	80MHz to 1GHz operating frequency
Input impedance	2,3		50		ohms	See Fig.5
			2		pF	
Output voltage no load	6	0.8			V p-p	fin = 1GHz V_{CC} = 5V
	7	0.8			V p-p	
Output voltage with load as Fig.3	6	0.55			V	fin = 1GHz V_{CC} = 5V
	7	0.55			V	
Output impedance	6		0.5		kohms	
	7		0.5		kohms	
Output imbalance	6,7		0.1		V	

NOTE

The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

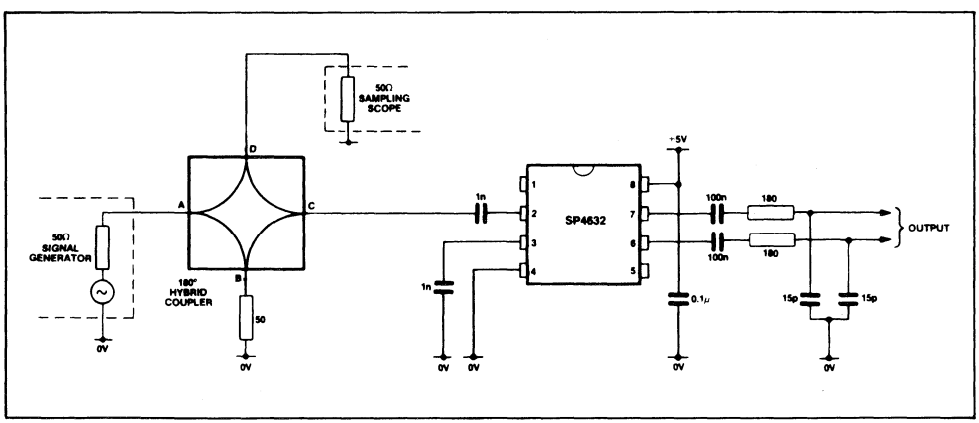


Fig.3 Test circuit

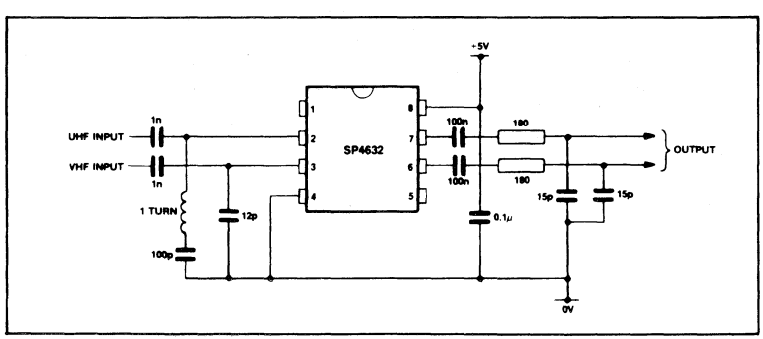


Fig.4 Application circuit

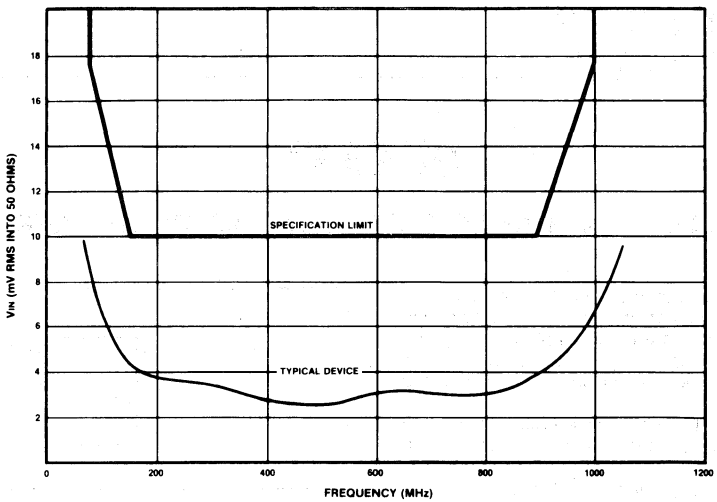


Fig.5 Typical input sensitivity

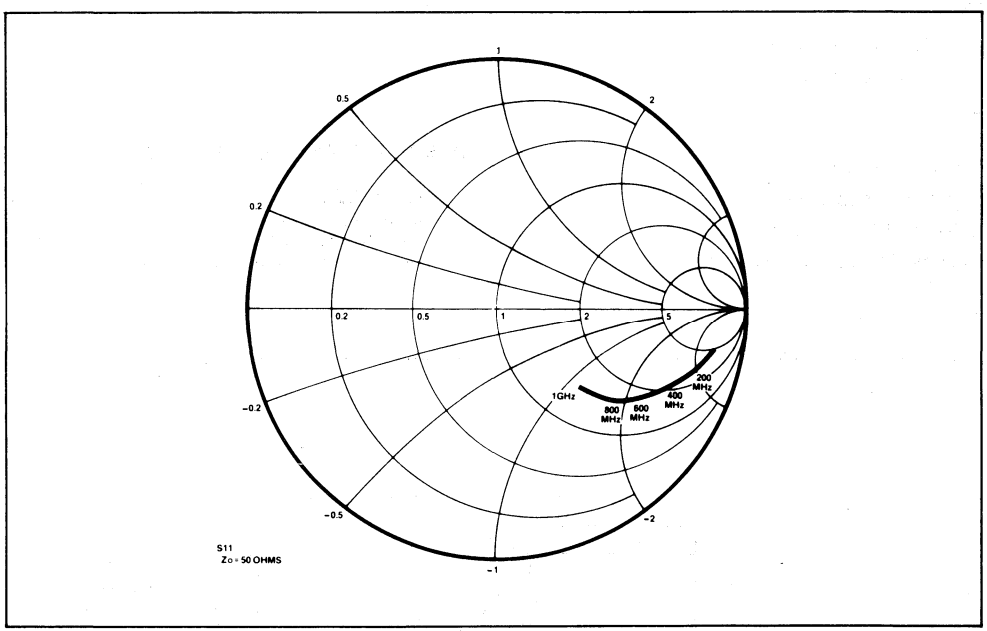


Fig.6 Typical input impedance

3058-1.0

SP4633

1GHz ÷ 64 NON SELF OSCILLATING PRESCALER

The SP4633 ÷64 prescaler is one of GPS' range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4633 incorporates a two-stage preamplifier which gives good low frequency sensitivity and prevents self-oscillation.

Electostatic protection is provided on all pins.

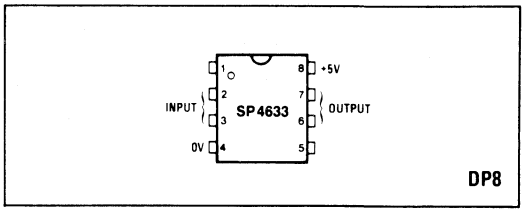


Fig.1 Pin connections - top view

FEATURES

- Does Not Self Oscillate
- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C
Operating temperature range	0°C to +80°C

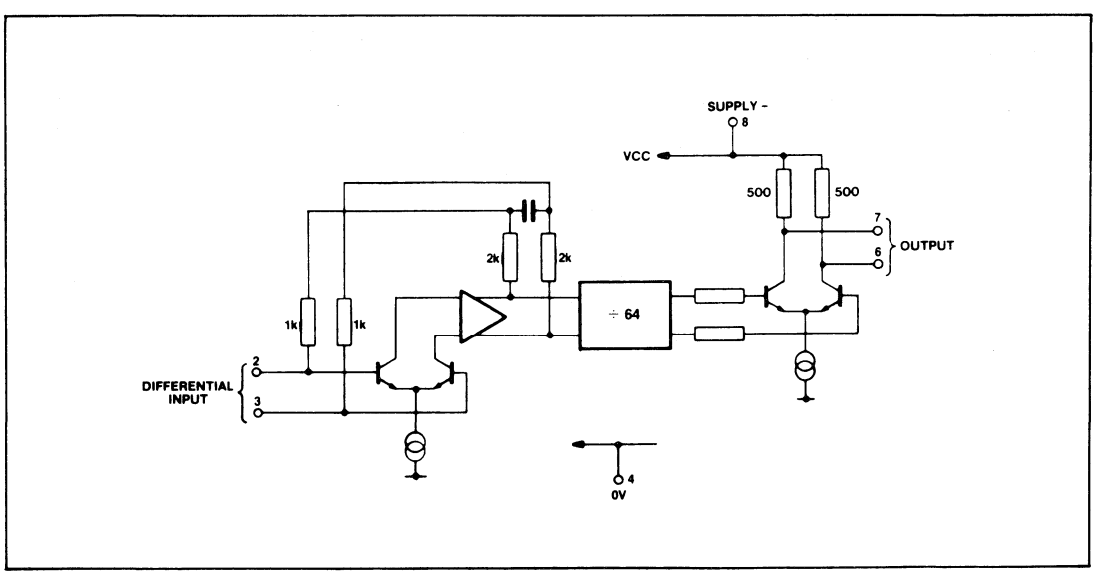


Fig.2 SP4633 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		32	45	mA	V_{CC} + 5V
Input sensitivity	2,3					RMS sinewave (50 ohms system)
50MHz to 400MHz			1.5	5	mV	
600MHz			2	7.5	mV	
800MHz			3	10	mV	
1000MHz			5	15	mV	
Input overload	2,3	300			mV	50MHz to 1GHz operating frequency
Input impedance	2,3		50		ohms	See Fig.5
			2		pF	
Output voltage no load	6	0.8			V p-p	f_{in} = 1GHz V_{CC} = 5V
	7	0.8			V p-p	
Output voltage with load as Fig.3	6	0.55			V	f_{in} = 1GHz V_{CC} = 5V
	7	0.55			V	
Output impedance	6		0.5		kohms	
	7		0.5		kohms	
Output imbalance	6,7		0.1		V	

NOTE
The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

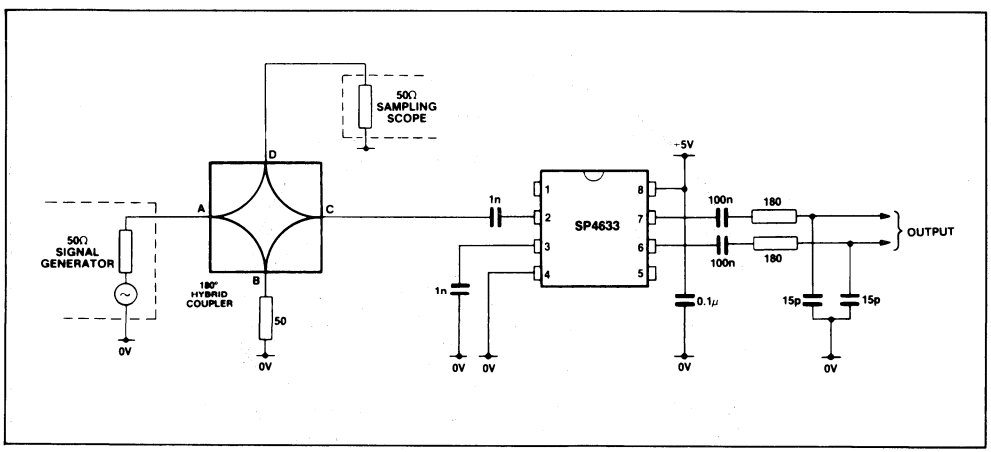


Fig.3 Test circuit

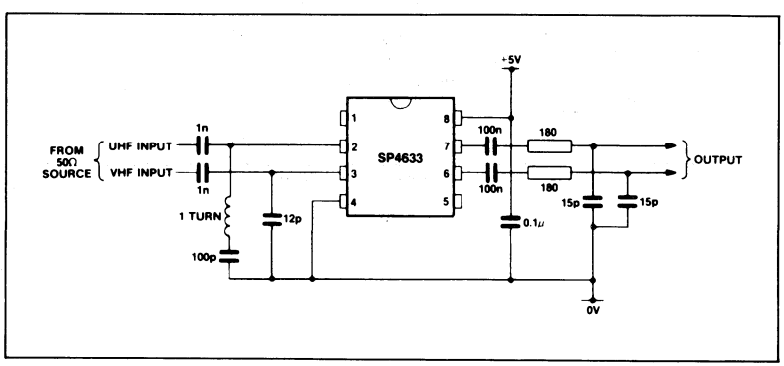


Fig.4 Application circuit

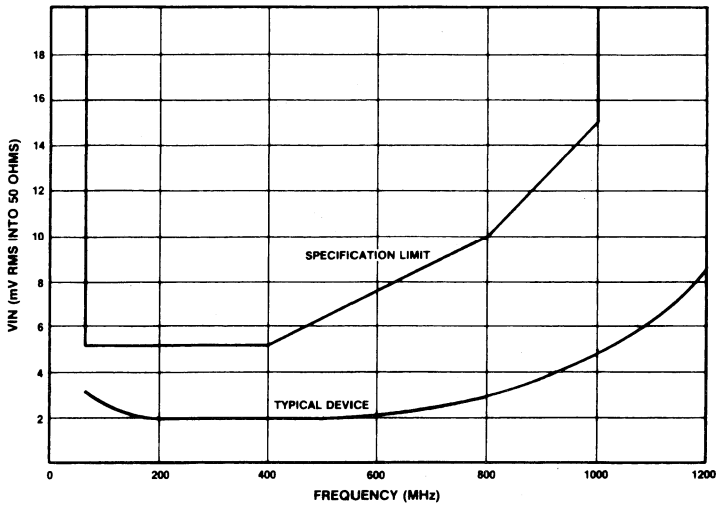


Fig.5 Typical input sensitivity

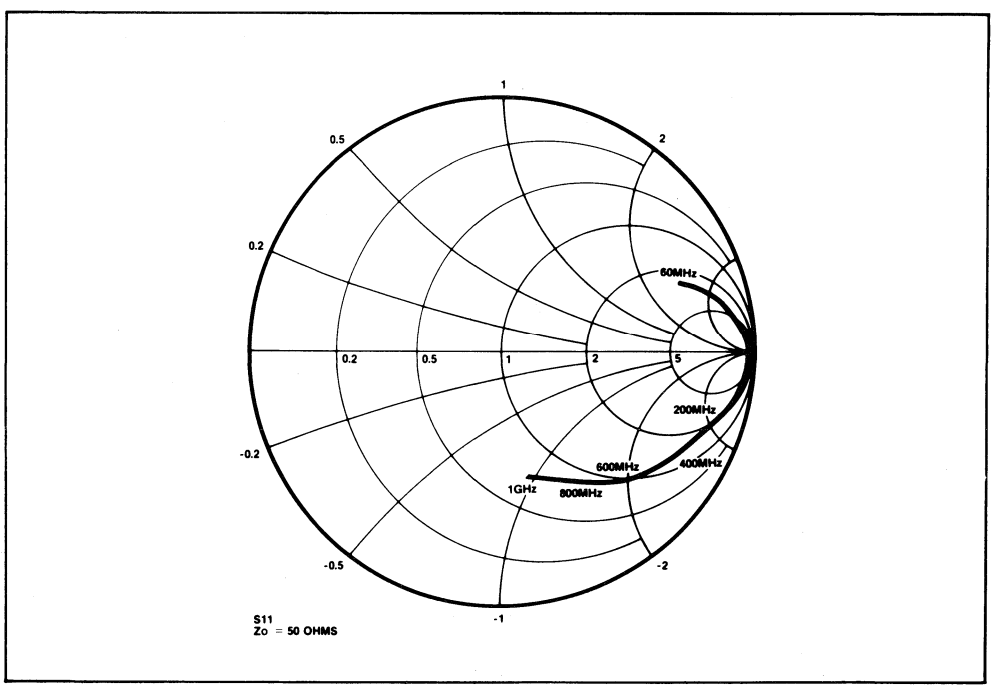


Fig.6 Typical input impedance

3059-1.0

SP4653

1GHz ÷ 256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4653 ÷256 prescaler is one of GPS' range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4653 incorporates an on-chip preamplifier with differential inputs and has a balanced ECL outputs.

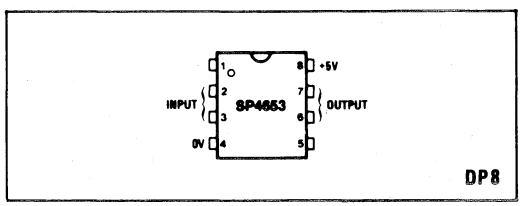


Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C
Operating temperature range	0°C to +80°C

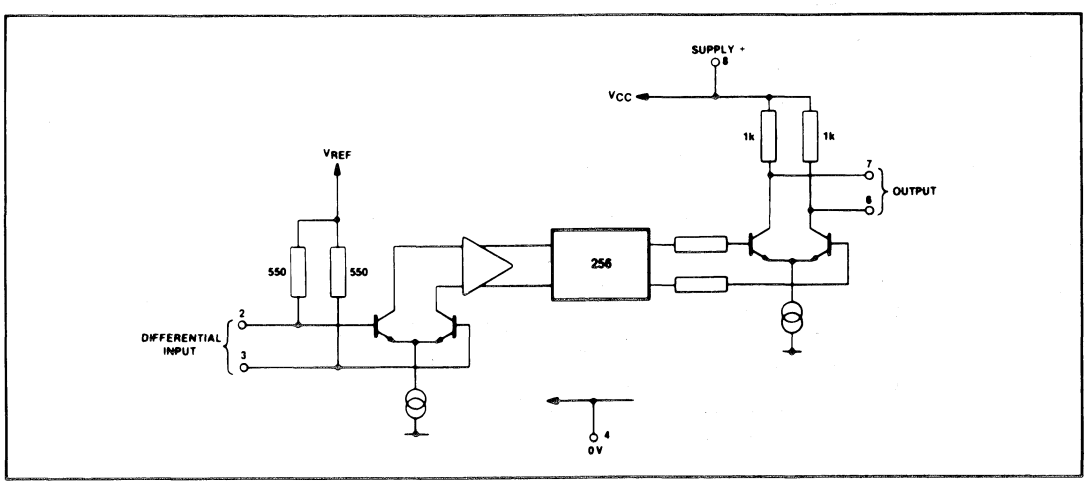


Fig.2 SP4653 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		25	35	mA	V_{CC} = 5V
Input sensitivity	2,3			17.5		RMS sinewave
70MHz			8	14	mV	
150MHz			4	10	mV	
300MHz			3	10	mV	
500MHz			3	10	mV	
700MHz			3	10	mV	
900MHz			4	10	mV	
1050MHz			6	14	mV	
Input overload	2,3	200			mV	70MHz to 1050MHz operating frequency
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage no load	6	0.8			V p-p	fin = 1GHz V_{CC} = 5V
	7	0.8			V p-p	
Output voltage load as Fig.3	6	0.6			V p-p	fin = 1GHz V_{CC} = 5V
	7	0.6			V p-p	
Output impedance	6		1		kohms	
	7		1		kohms	
Output imbalance	6,7		0.1		V	

NOTE
The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

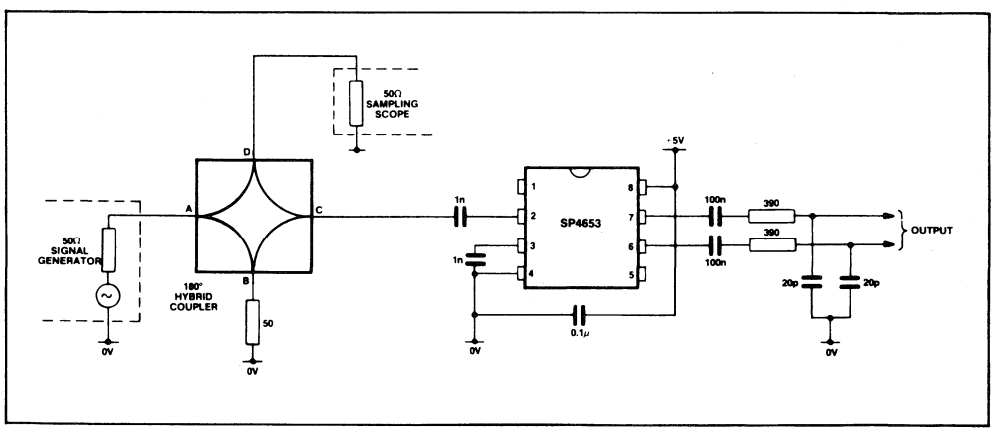


Fig.3 Test circuit

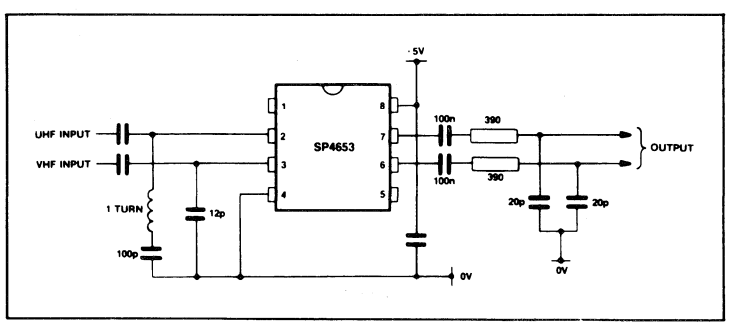


Fig.4 Application circuit

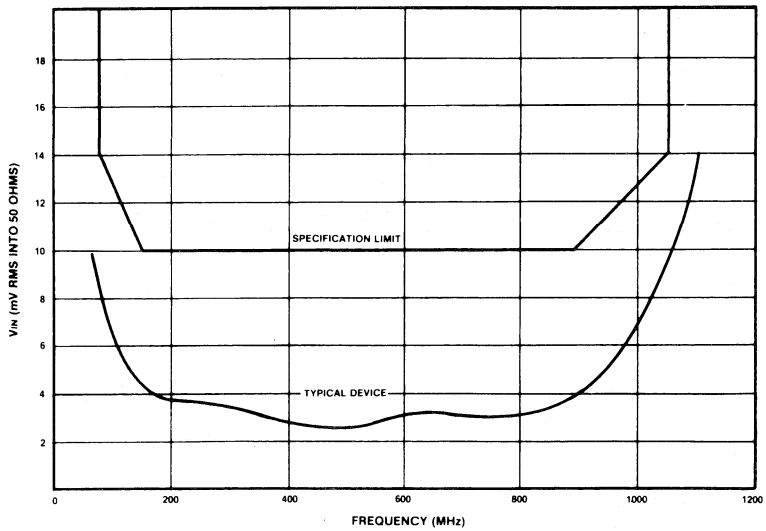


Fig.5 Typical input sensitivity

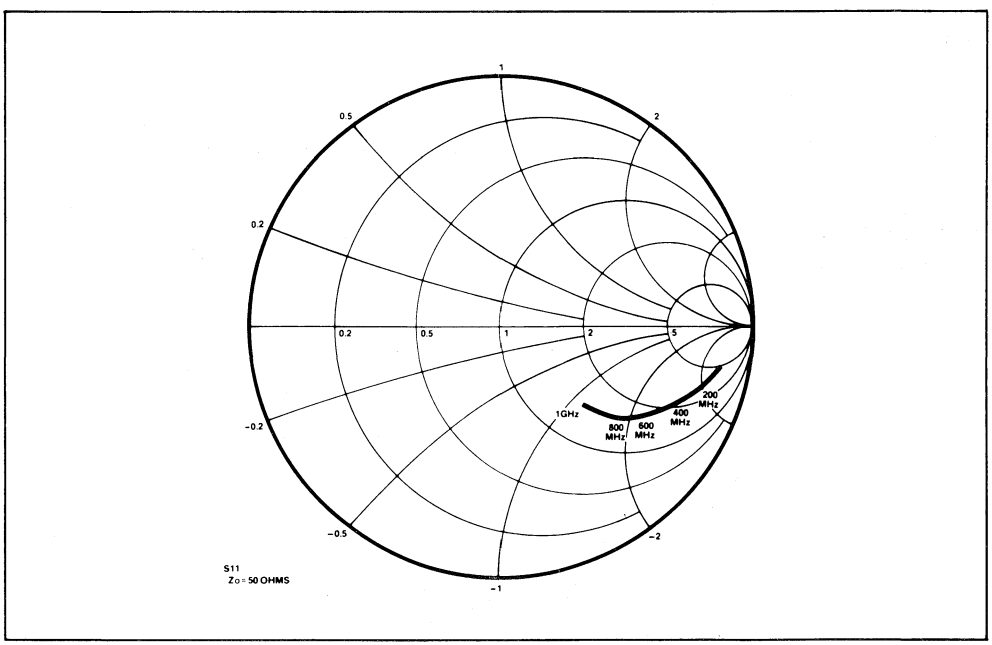


Fig.6 Typical input impedance

SP4660

1GHz ÷ 256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4660 ÷256 prescaler is one of GPS' range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4660 incorporates an on-chip preamplifier with differential inputs and has a balanced ECL outputs.

Electostatic protection is provided on all pins.

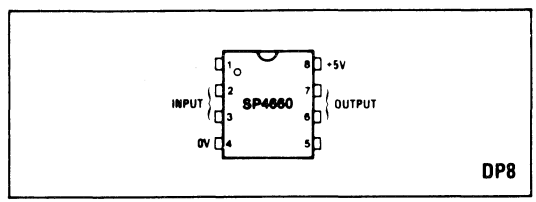


Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity from 50MHz to 1GHz
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C
Operating temperature range	0°C to +80°C

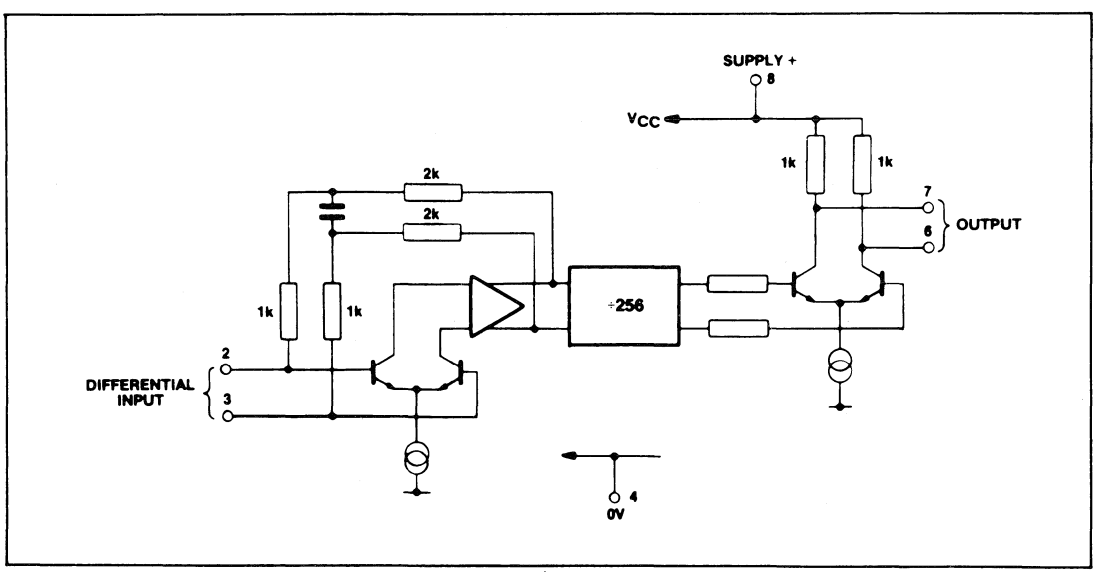


Fig.2 SP4660 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		32	45	mA	Vcc = 5V
Input sensitivity	2,3					RMS sinewave
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
Input overload	2,3					
		300			mV	50MHz to 1.0GHz
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage no load	6	0.8			V p-p	fin = 1GHz Vcc = 5V
	7	0.8			V p-p	
Output voltage load	6	0.6			V p-p	fin = 1GHz Vcc = 5V
as Fig.3	7	0.6			V p-p	
Output impedance	6		1		kohms	
	7		1		kohms	
Output imbalance	6,7			0.1	V	

NOTE
The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

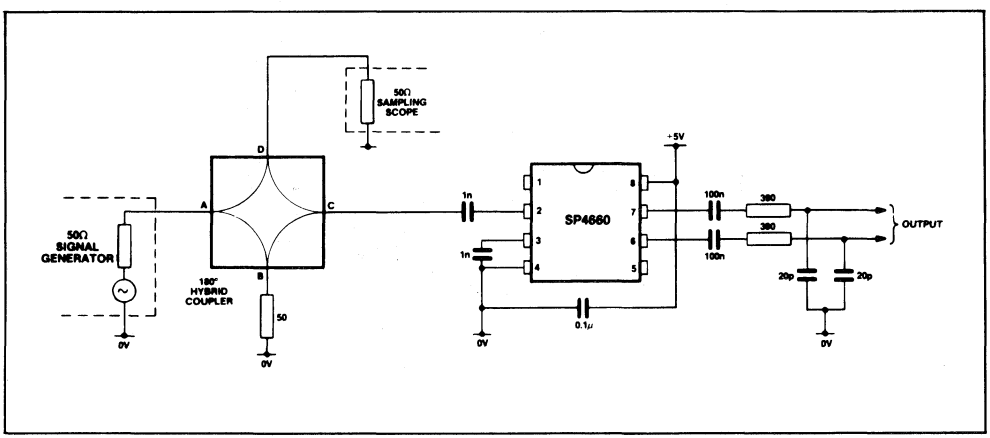


Fig.3 Test circuit

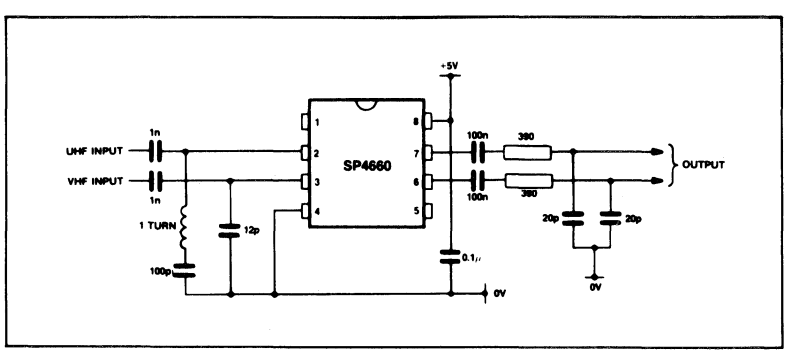


Fig.4 Application circuit

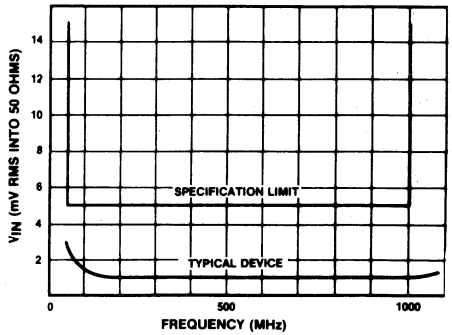


Fig.5 Typical input sensitivity

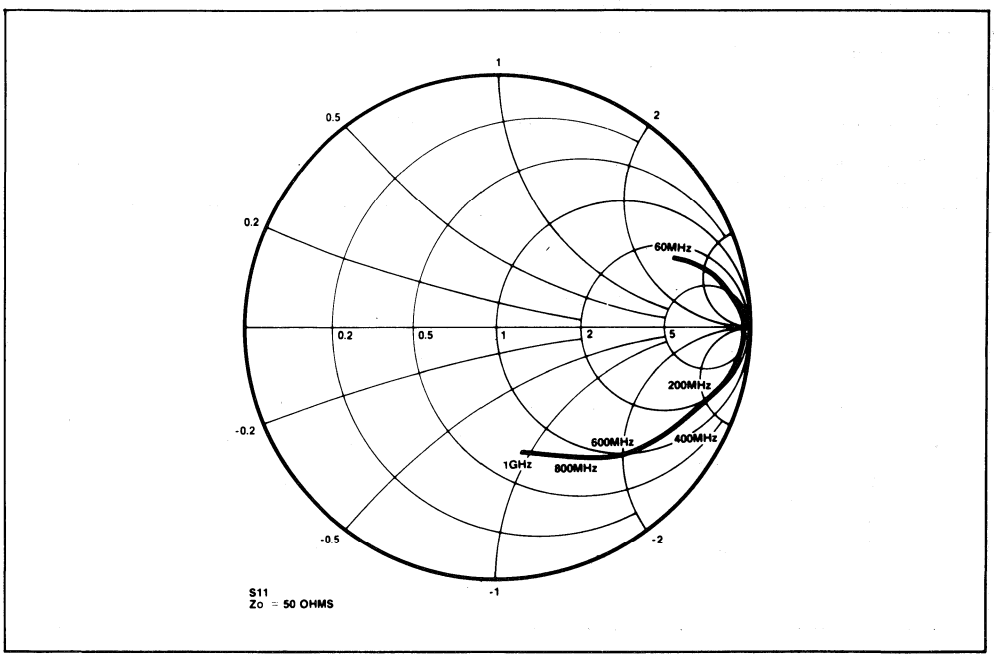


Fig.6 Typical input impedance

SP4666

1.0GHz ÷ 64/256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4666 is a selectable division ratio high speed divider capable of replacing ECL prescalers such as SP4632 and SP4653 with a single part in applications with alternative ÷64 and ÷256 division requirements.

A switched low pass filter with -3dB points at 5.3MHz and 15.6MHz is connected before the output stage to reduce the harmonic content to very low levels.

Electrostatic protection is provided on all pins.

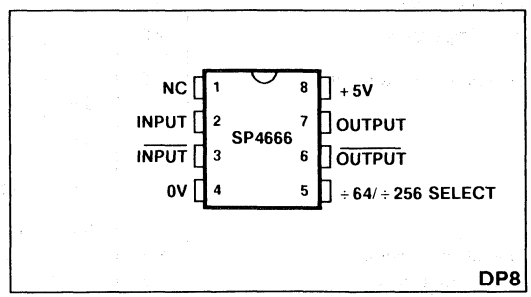


Fig 1 Pin Connections - top view

FEATURES

- Switched Low Pass Filter for Very Low Output Radiation
- Low Supply Current
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection on Chip

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	VCC + 7V
Input voltage	2.5v p-p
Storage temperature range	-55°C to +125°C
Operating temperating range	0°C to +80°C

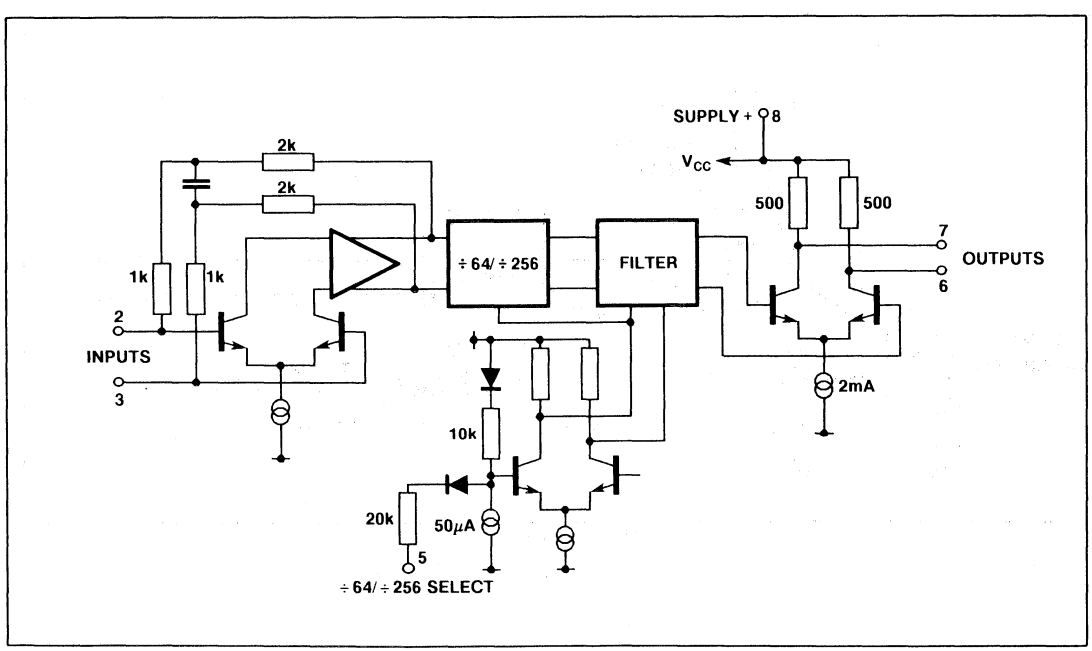


Fig. 2 SP4666 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Tamb = 0°C to +80°C, VCC = +4.5V to +5.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	8		23	30	mA	VCC = 5V
Input sensitivity	2,3					RMS sinewave
50MHz			2.5	10	mV	
200MHz to 1050MHz			0.5	5	mV	
Input overload	2,3	500			mV	
Input impedance	2,3		50		ohms	See fig.6
			2		pF	
Output voltage with 12pF load	6,7					
		0.8	1		Vp-p	÷64 mode fin = 100MHz
		0.8	1		Vp-p	÷256 mode
		0.4	0.5		Vp-p	÷64 mode fin = 1000MHz
		0.7	0.9		Vp-p	÷256 mode
Output impedance	6,7		500		ohms	
Output imbalance	6,7		0.1		V	
Voltage for ÷256 operation	5			0.5	V	
Voltage for ÷64 operation	5	3.5			V	See Note 1
Sink current for ÷256 operation	5			250	µA	V pin 5 = 0V

NOTES
1. Pin 5 has an internal pull up and may be left open circuit for ÷64 operation
2. The difference between the maximum input sensitivity and minimum overload figures is the dynamic range of the device. For correct operation the input signal must be maintained between these limits at all frequencies

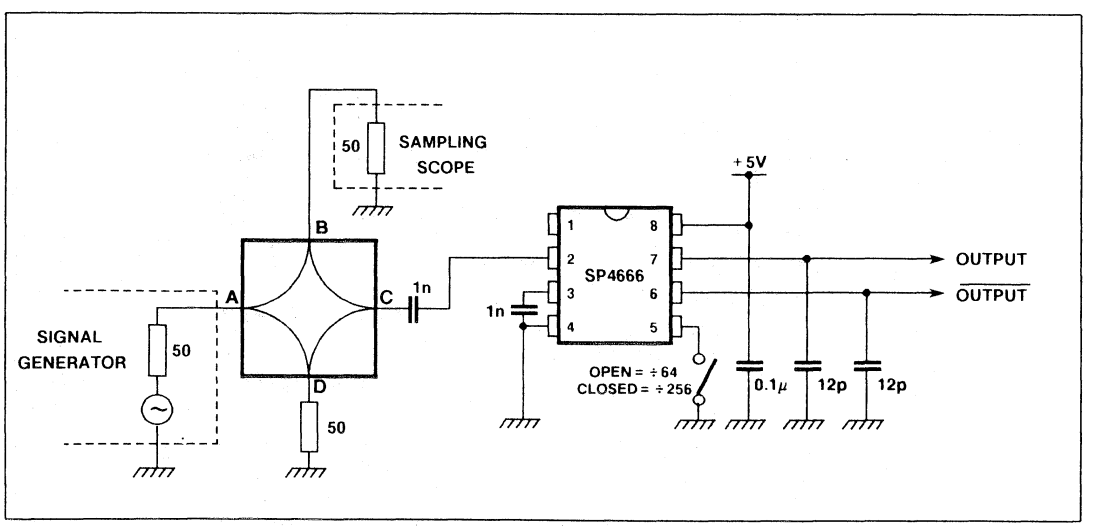


Fig. 3 Test circuit

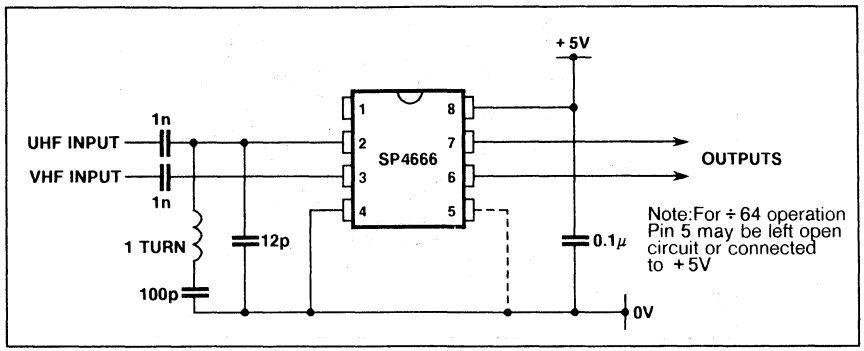


Fig.4 Application circuit

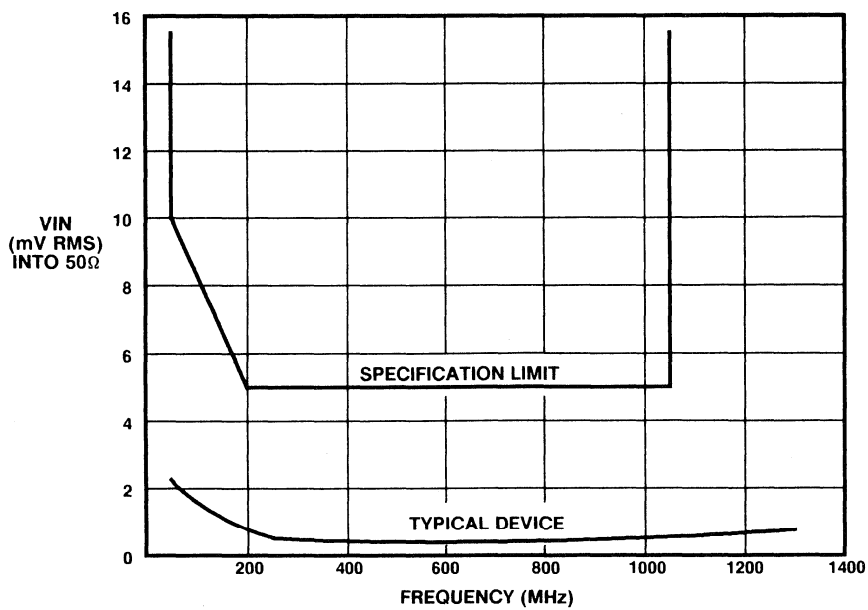


Fig.5 Typical input sensivity

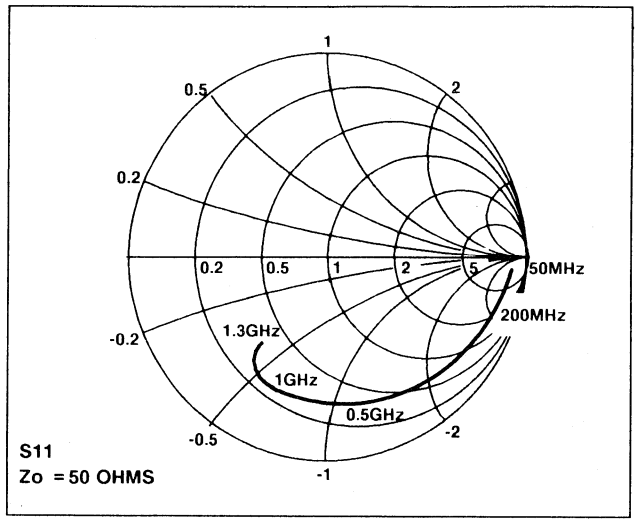


Fig.6 Typical input impedance

SP4676

950MHz ÷ 128/136, ÷ 64/68 VERY LOW RADIATION DUAL MODULUS PRESCALER

The SP4676 ÷ 128/136, ÷64/68 prescaler is one of GPS' range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in 8-pin plastic DIL (DP8) or miniature plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4676 incorporates an on chip preamplifier and has a single ECL output. The control input is latched and synchronised making the device highly tolerant to delays in the control loop.

Electrostatic protection is provided on all pins.

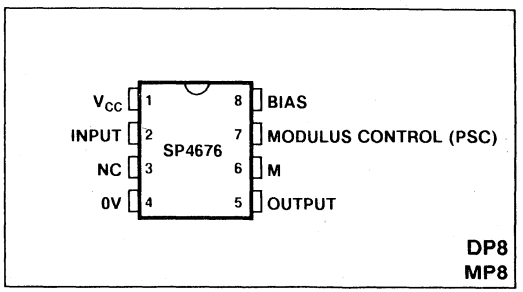


Fig 1 Pin Connections - top view

FEATURES

- Low Supply Current
- Very Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- Latched and Synchronised Modulus Control Input
- Single ECL Output
- Electrostatic Protection on Chip

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{CC} + 7V
Input voltage	2.5v p-p
Storage temperature range	-55°C to +125°C
Control input voltage (PSC)	-0.5V to V_{CC}
Operating temperating range	0°C to +70°C

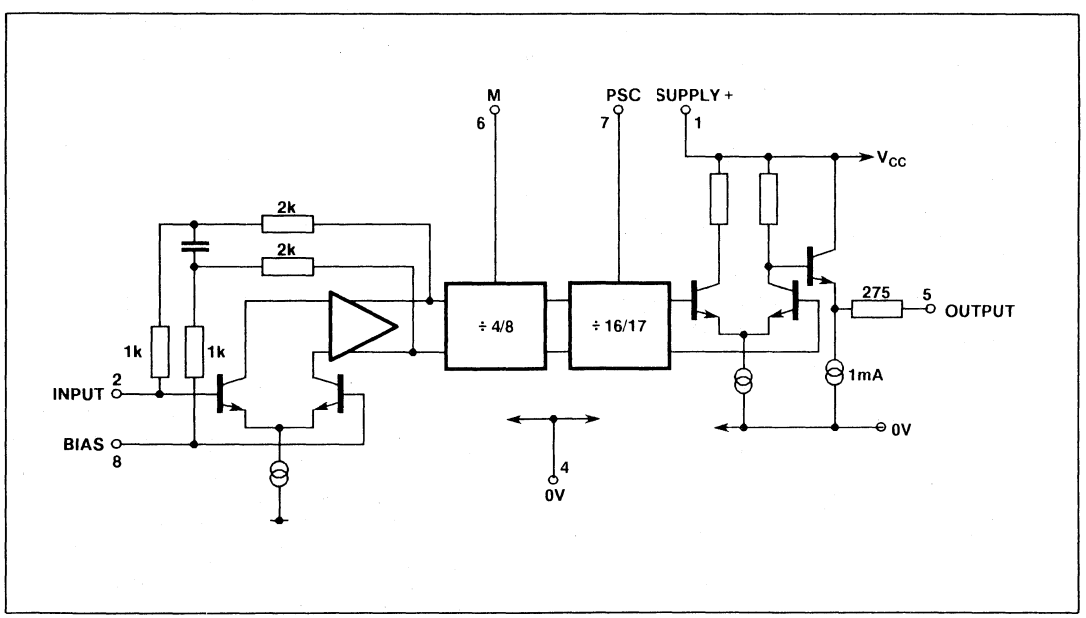


Fig. 2 SP4676 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Tamb = 0°C to +70°C, VCC = +4.5V to +5.5V with 10ns rise and fall time on PSC input.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	1		16	21	mA	VCC = 5V
Input sensitivity (see Fig. 3)	2					RMS sinewave
Input overload 50 to 950MHz (see note)	2	400			mV	
Input impedance	2		50 2		ohms pF	
Output voltage	5		1.2		Vp-p	15pF load, fo ≤3.5MHz
		1.0			Vp-p	15pF load, fo ≤7.5MHz
High level input voltage	7	$0.7V_{CC}$			V	÷68/136 mode
Low level input voltage	7			$0.3V_{CC}$	V	÷64/128 mode
High level input current	7			10	µA	
High level input voltage	6	$0.6V_{CC}$			V	÷64/68 mode
Low level input voltage	6			$0.4V_{CC}$	V	÷128/136 mode
High level input current	6			10	µA	

NOTE
The difference between the maximum input sensitivity and minimum overload figures is the dynamic range of the device. For correct operation the input signal must be maintained between these limits at all frequencies

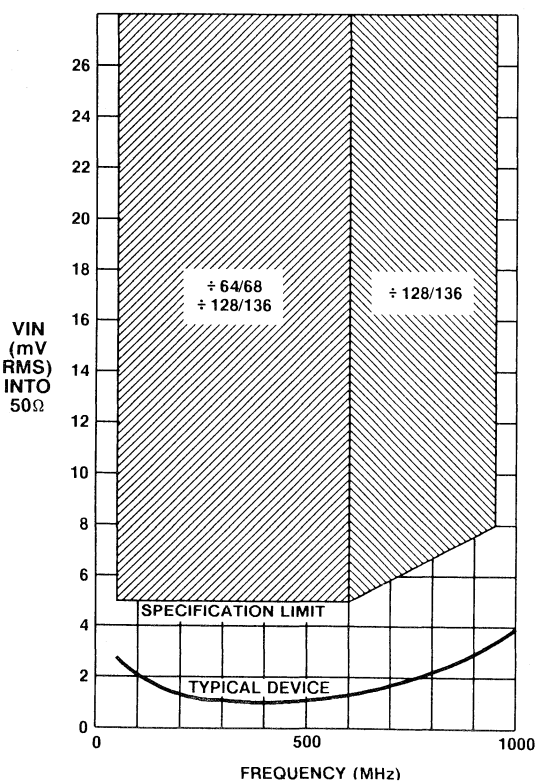


Fig. 3 Typical input sensitivity

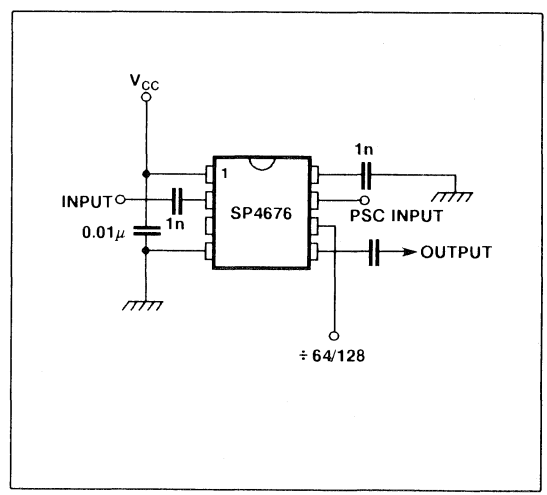


Fig. 4 Typical application circuit

NOTES(Refer to Fig. 6 opposite)

1. The PSC input is sampled at 2 points in each output half cycle, the sampling points being 25% and 50% of the high or low output period from the output transitions (see Fig. 6a).
2. The PSC input must be high for both sampling points in a high or low output period to increase the division ratio for that output period (see Fig. 6b).
3. The rising edge of the swallow pulse should occur at least 30ns before the 25% sampling point.
4. The division ratio may only be increased for either the positive or negative portion of any output cycle.

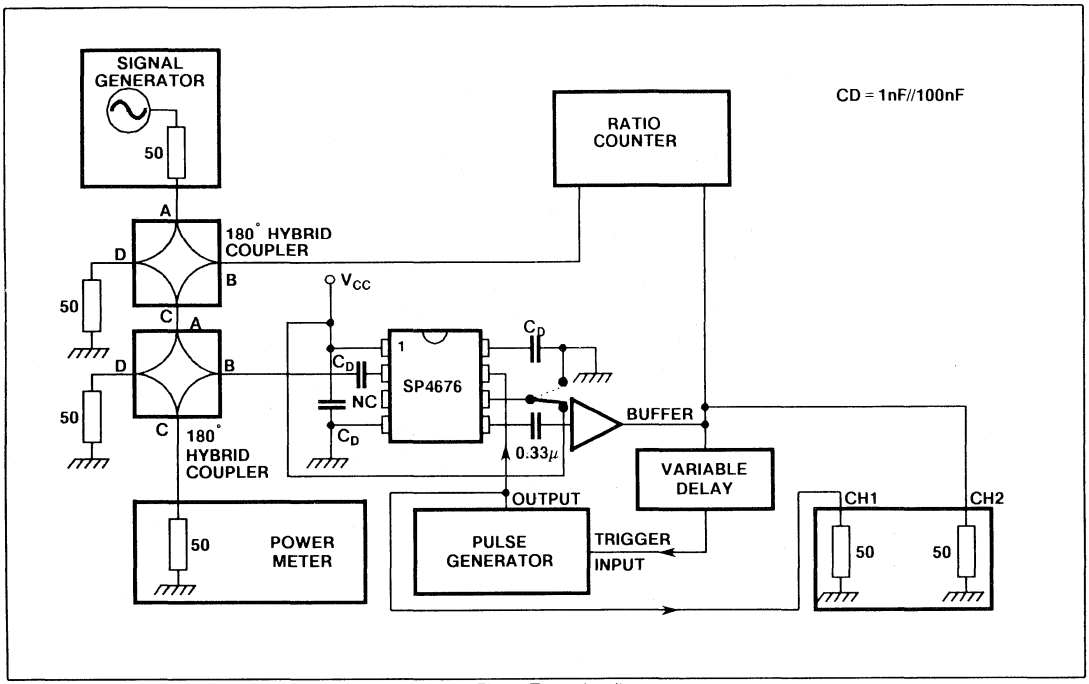


Fig. 5 Test circuit

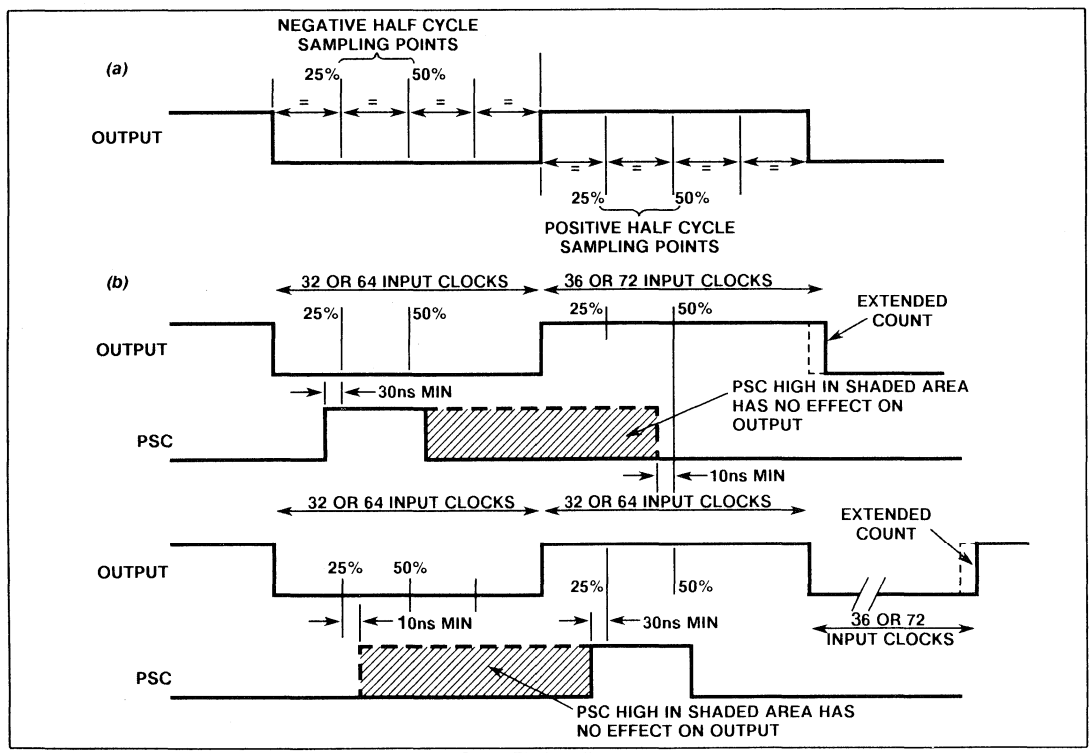


Fig. 6 Timing diagram

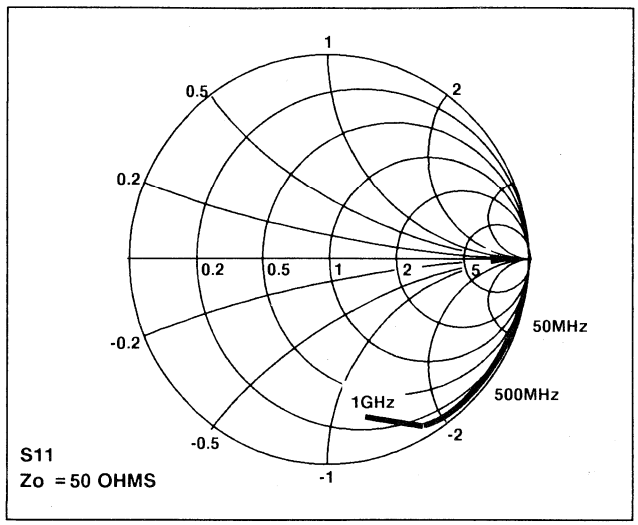


Fig.7 Typical input impedance

3061-1.0

SP4731

1.3GHz ÷ 64 HIGH OUTPUT SWING LOW CURRENT PRESCALER

The SP4731 ÷64 prescaler is one of GPS' range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4731 incorporates an on-chip preamplifier with differential inputs and has a balanced ECL outputs.

Electostatic protection is provided on all pins.

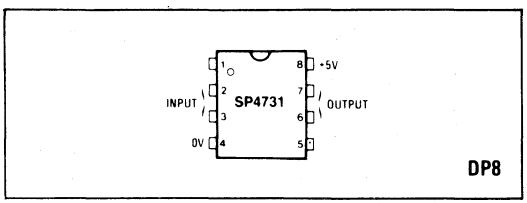


Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- High Output Swing
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C
Operating temperature range	0°C to +80°C

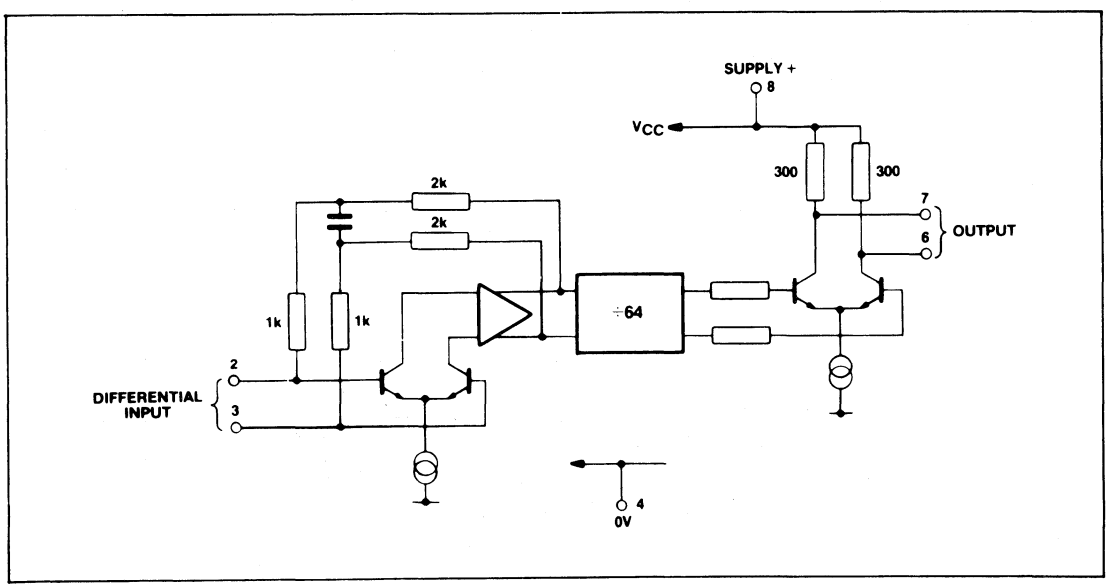


Fig.2 SP4731 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C Vcc = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		35	50	mA	Vcc = 5V
Input sensitivity	2,3					RMS sinewave (50 ohms system)
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
1.1GHz			1.5	10	mV	
1.2GHz			2	15	mV	
1.3GHz			4	20	mV	
Input overload	2,3	400			mV	50MHz to 500MHz
		300			mV	500MHz to 1.3GHz
Input impedance	2,3		50		ohms	See Fig.5
			2		pF	
Output voltage no load	6	1.0			V p-p	} fin = 1.3GHz Vcc = 5V
	7	1.0			V p-p	
Output voltage load	6	0.8			V p-p	} fin = 1.3GHz Vcc = 5V
as Fig.3	7	0.8			V p-p	
Output impedance	6		0.3		kohms	
	7		0.3		kohms	
Output imbalance	6,7			0.1	V	

NOTE
The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

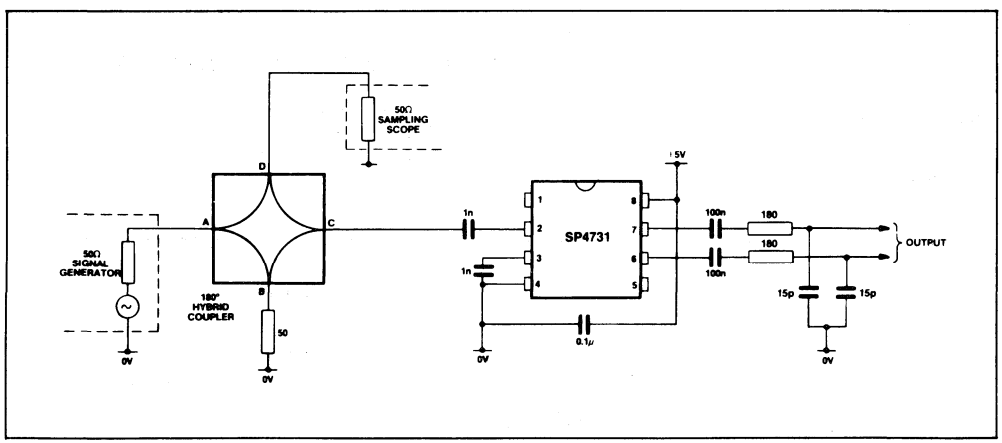


Fig.3 Test circuit

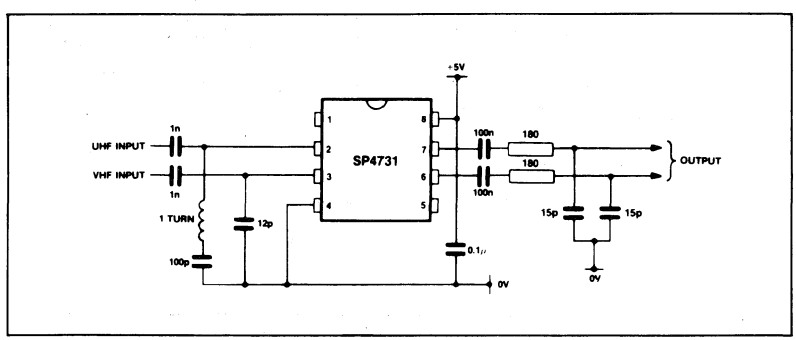


Fig.4 Application circuit

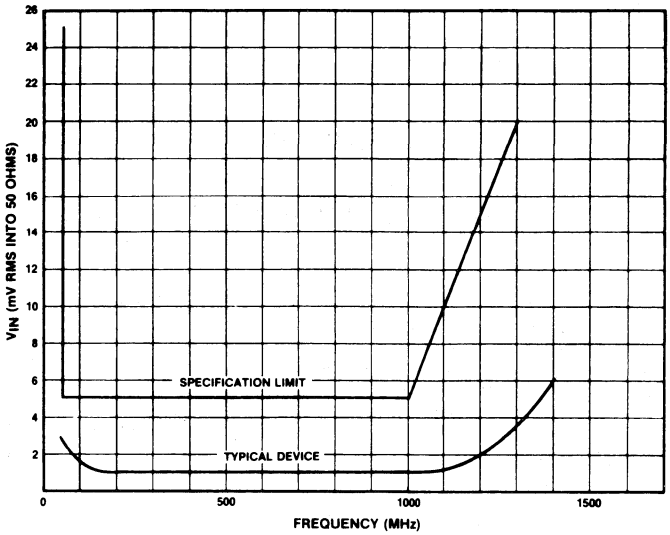


Fig.5 Typical input sensitivity

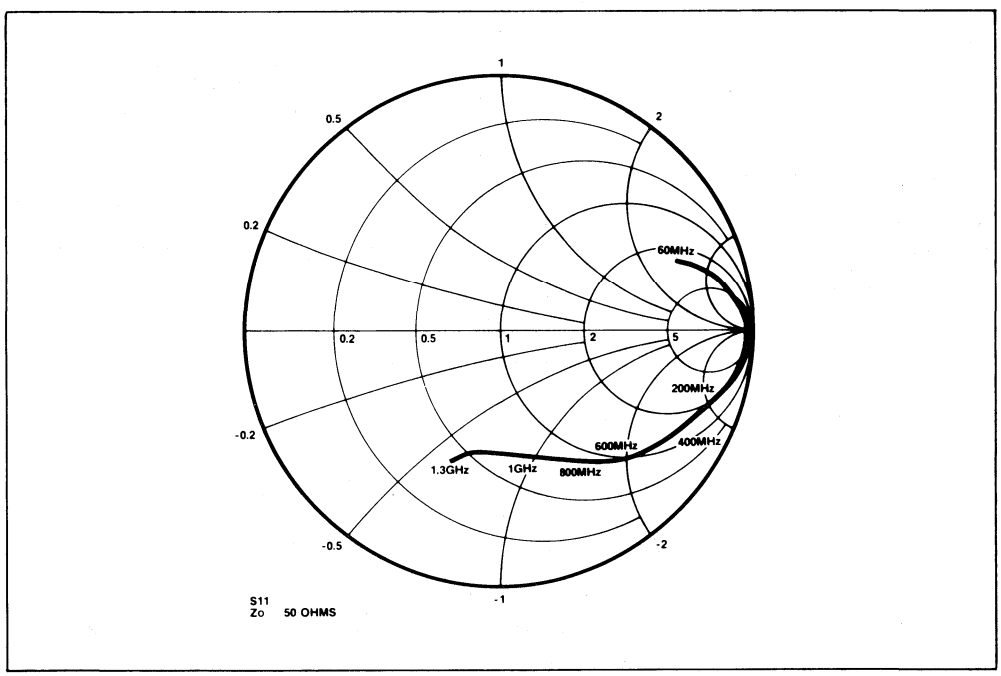


Fig.6 Typical input impedance

3062-1.0

SP4740

1.3GHz ÷ 256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4740 ÷256 prescaler is one of GPS' range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in 8-pin plastic DIL (DP8) or miniature plastic DIL (MP8) package. Spurious radiation has been reduced from all stages.

The SP4740 incorporates an on-chip preamplifier with differential inputs and has a balanced ECL outputs.

Electostatic protection is provided on all pins.

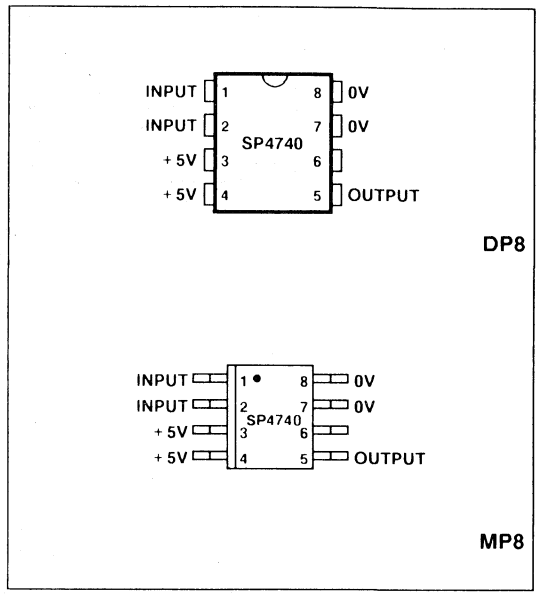


Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- TTL Output
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C
Operating temperature range	0° C to +80° C

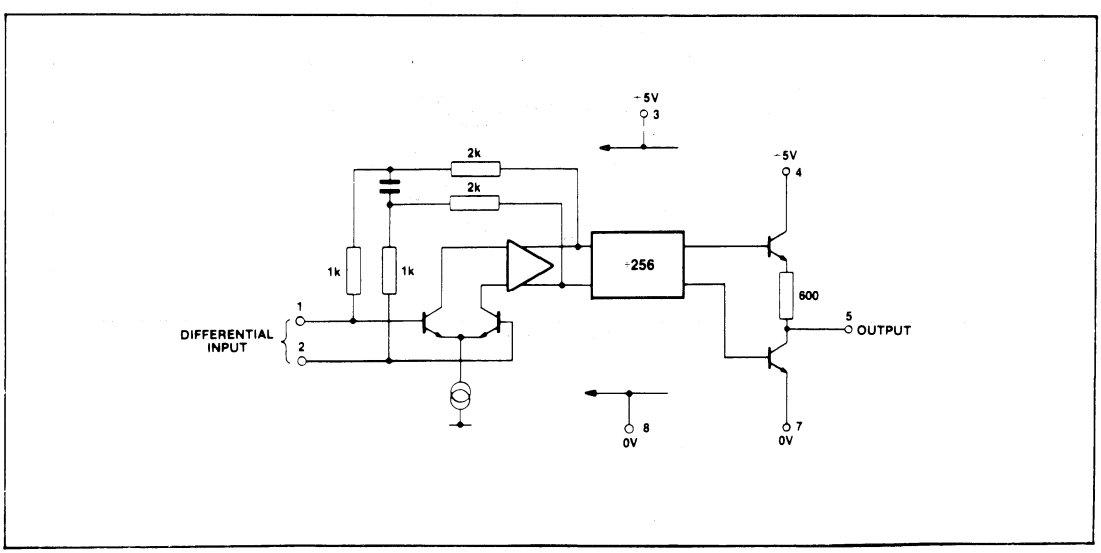


Fig.2 SP4740 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0° C to +70° C V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		35	50	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
1.1GHz			1.5	10	mV	
1.2GHz			2	15	mV	
1.3GHz			4	20	mV	
Input overload	2,3	400			mV	50MHz to 500MHz
		300			mV	500MHz to 1.3GHz
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage						
High	5	3.3			V	Sourcing 0.2mA
Low	5			0.4	V	Sinking 2mA

NOTE
The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

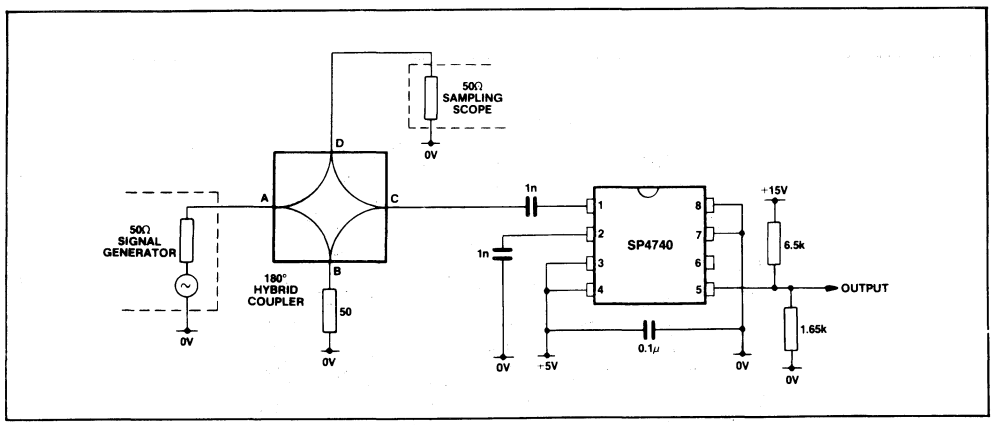


Fig.3 Test circuit

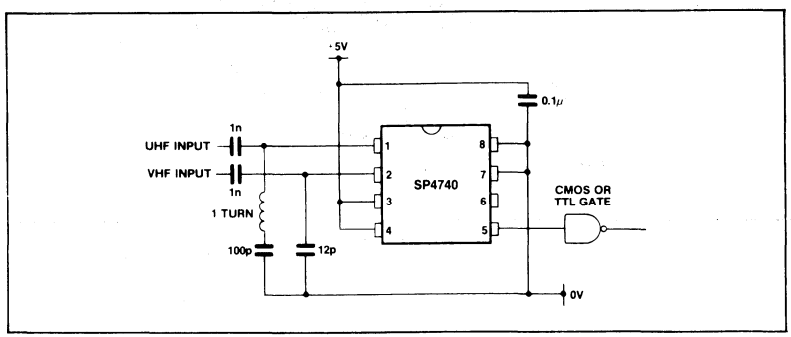


Fig.4 Application circuit

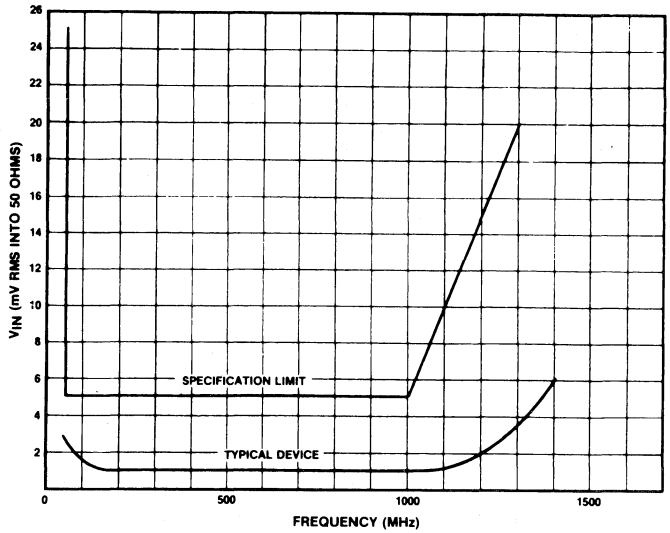


Fig.5 Typical input sensitivity

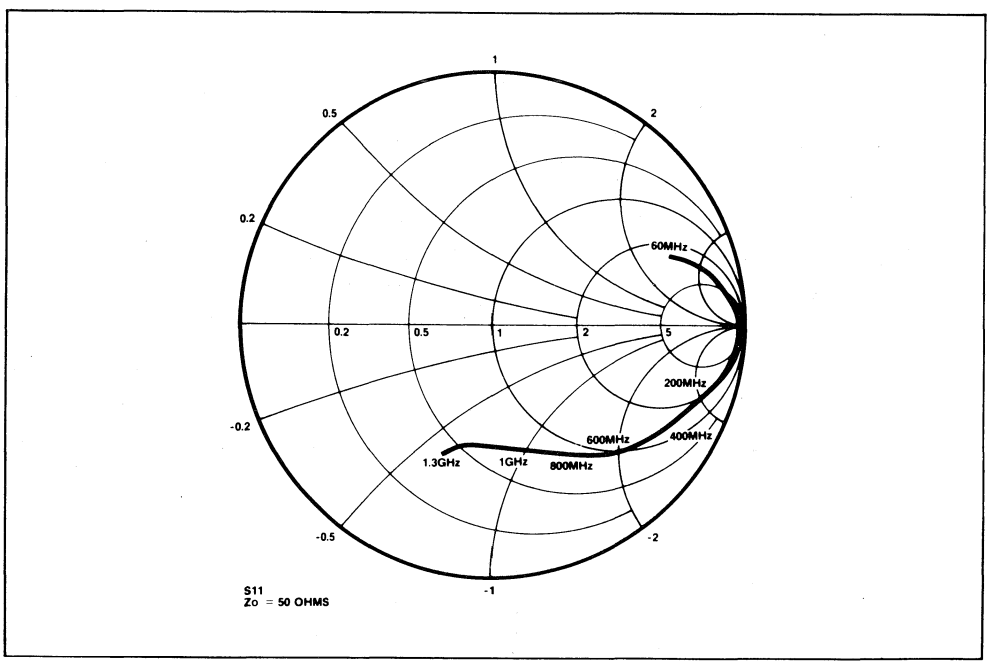


Fig.6 Typical input impedance

SP4751

1.3GHz ÷ 256 HIGH OUTPUT SWING LOW CURRENT PRESCALER

The SP4751 ÷256 prescaler is one of GPS' range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4751 incorporates an on-chip preamplifier with differential inputs and has a balanced ECL outputs.

Electostatic protection is provided on all pins.

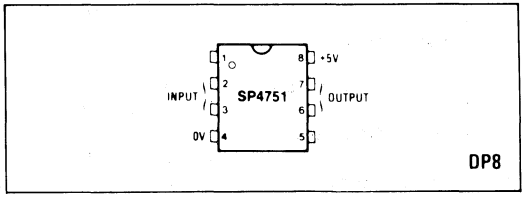


Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- High Output Swing
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C
Operating temperature range	0°C to +80°C

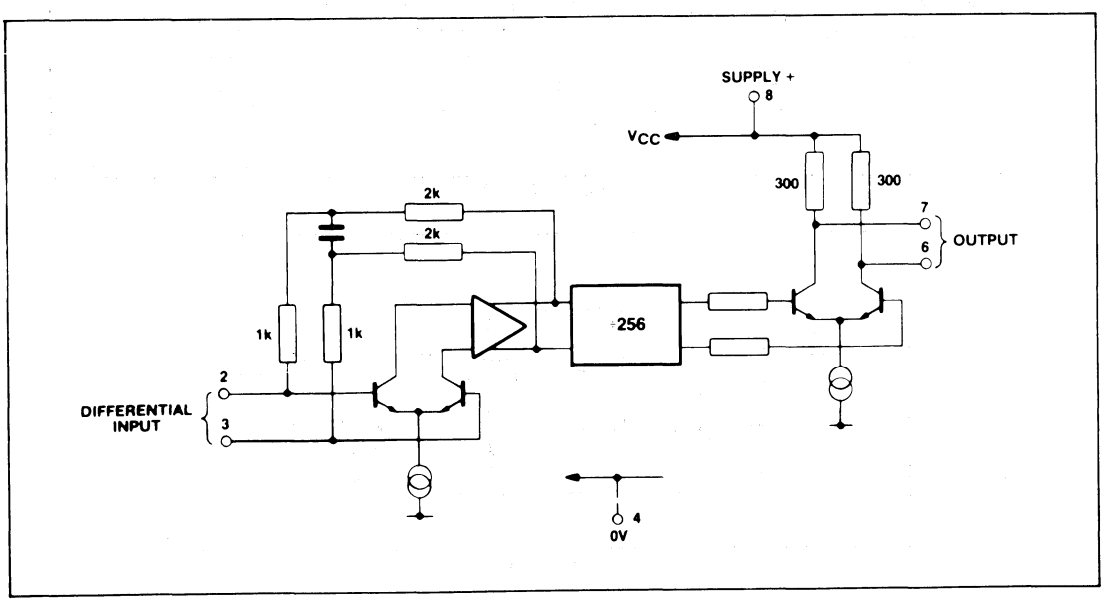


Fig.2 SP4751 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		35	50	mA	Vcc = 5V
Input sensitivity	2,3					RMS sinewave
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
1.1GHz			1.5	10	mV	
1.2GHz			2	15	mV	
1.3GHz			4	20	mV	
Input overload	2,3	400			mV	50MHz to 500MHz
		300			mV	500MHz to 1.3GHz
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage no load	6	1.0			V p-p	fin = 1.3GHz Vcc = 5V
	7	1.0			V p-p	
Output voltage load	6	0.8			V p-p	fin = 1.3GHz Vcc = 5V
as Fig.3	7	0.8			V p-p	
Output impedance	6		0.3		kohms	
	7		0.3		kohms	
Output imbalance	6,7			0.1	V	

NOTE
The difference between the maximum input sensitivity and minimum overload voltages is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

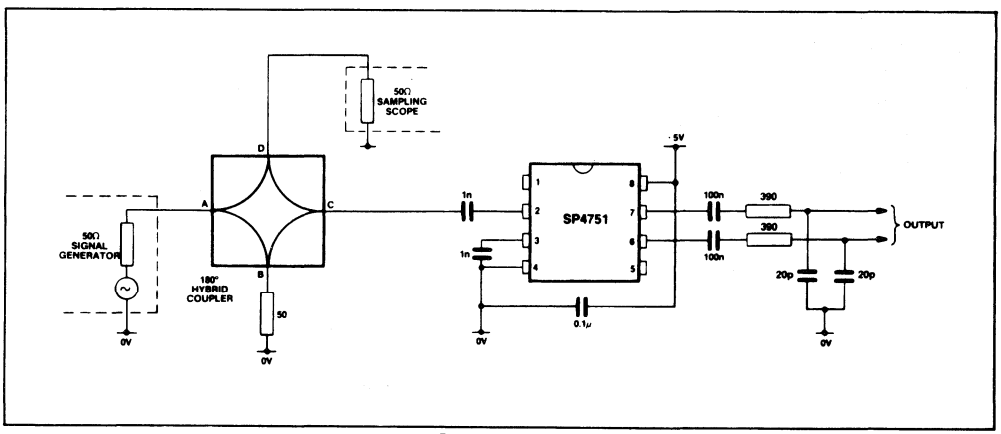


Fig.3 Test circuit

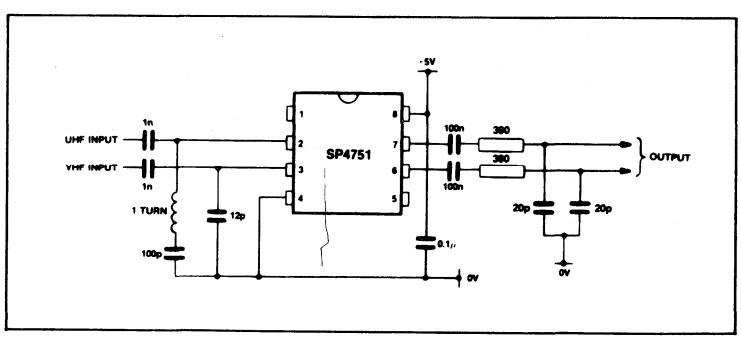


Fig.4 Application circuit

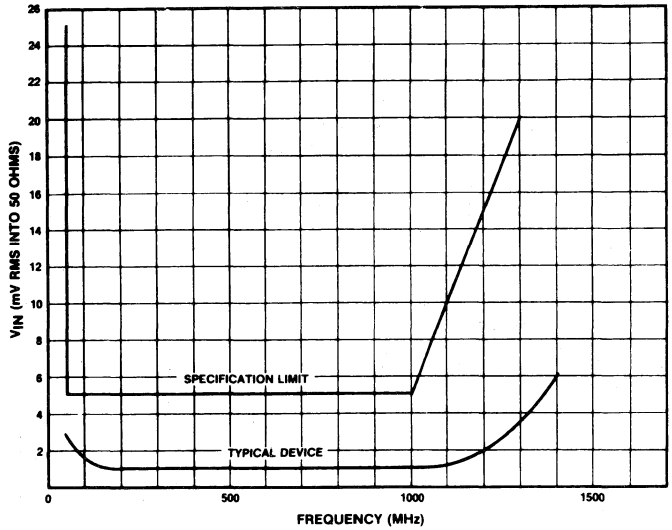


Fig.5 Typical input sensitivity

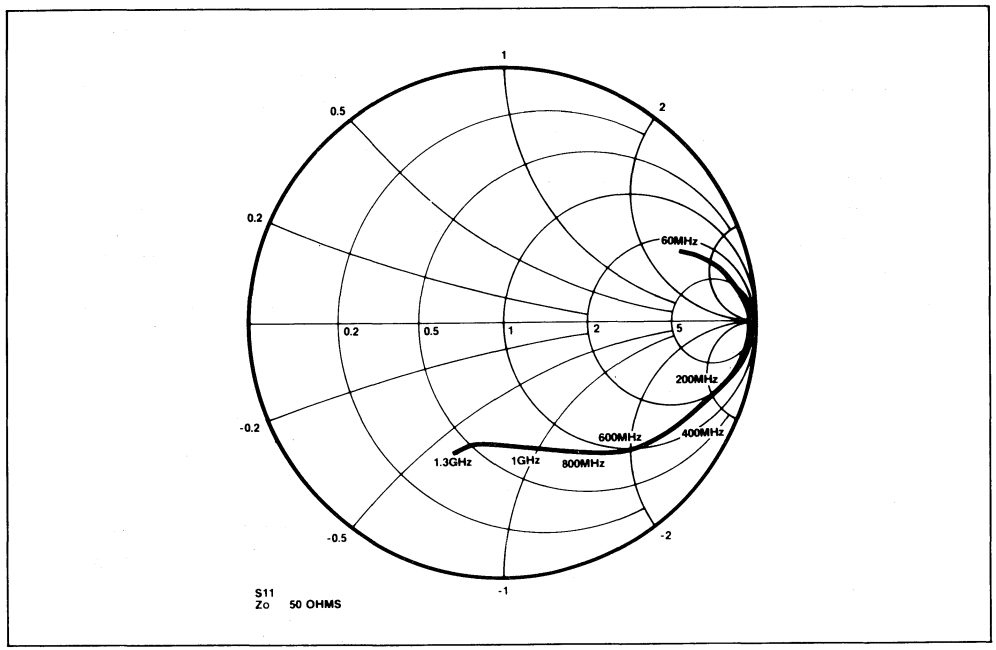


Fig.6 Typical input impedance

2244-1.0

SP4902

2.5GHz ÷ 2 PRESCALER

The SP4902 is one of a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 2.5GHz
- Silicon Technology for Low Phase Noise
- Very Low Power Dissipation 300mW
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Full ESD Protection

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

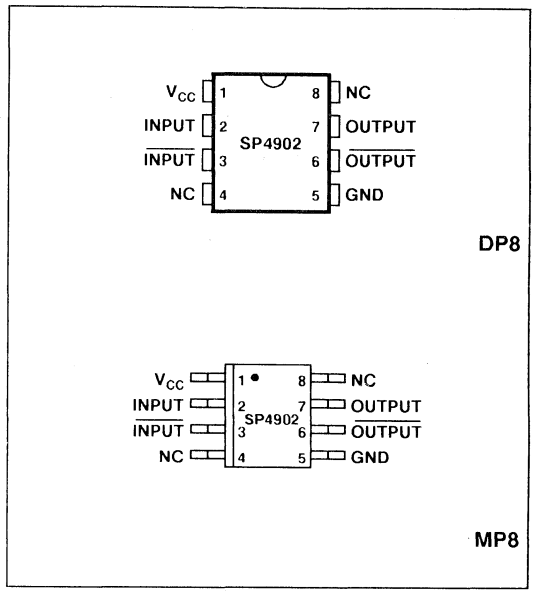


Fig 1 Pin Connections - top view

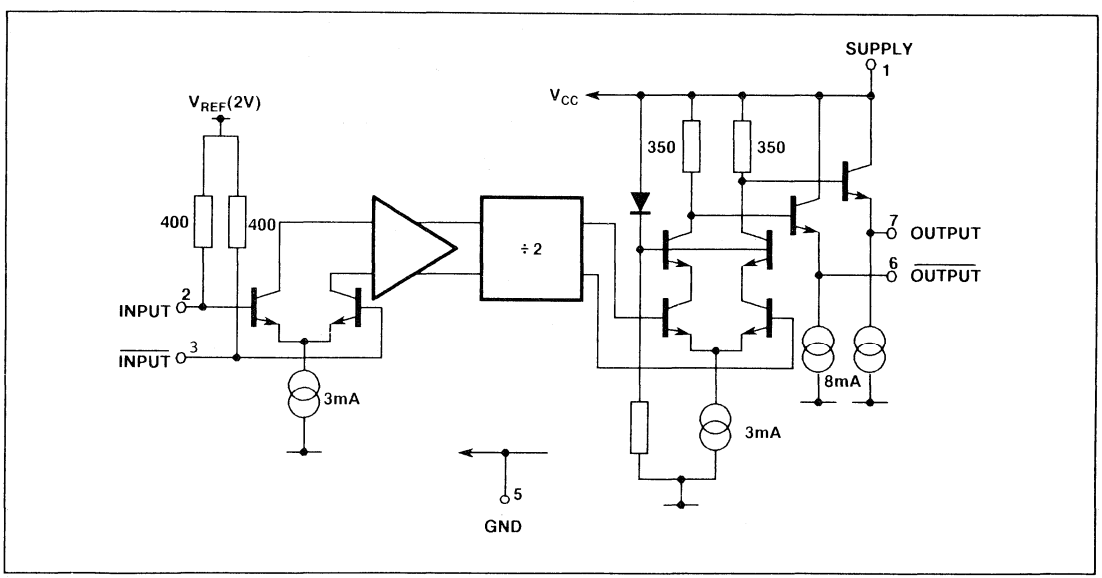


Fig 2 SP4902 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} = +4.75V to +5.25V Tamb = -10°C to +85°C

Characteristic	Pin.	Value			Units	Conditions
		Min.	Typ	Max.		
Supply current	1		60	75	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
500MHz to 1800MHz				50	mV	measured in 50Ω system. see
2500MHz				100	mV	Figs.3&4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with fin = 500MHz	6,7	0.45	0.55		Vp-p	V_{CC} = 5V Load as Fig.4
Output voltage with fin = 2500MHz	6,7	0.15	0.2		Vp-p	V_{CC} = 5V Load as Fig.4

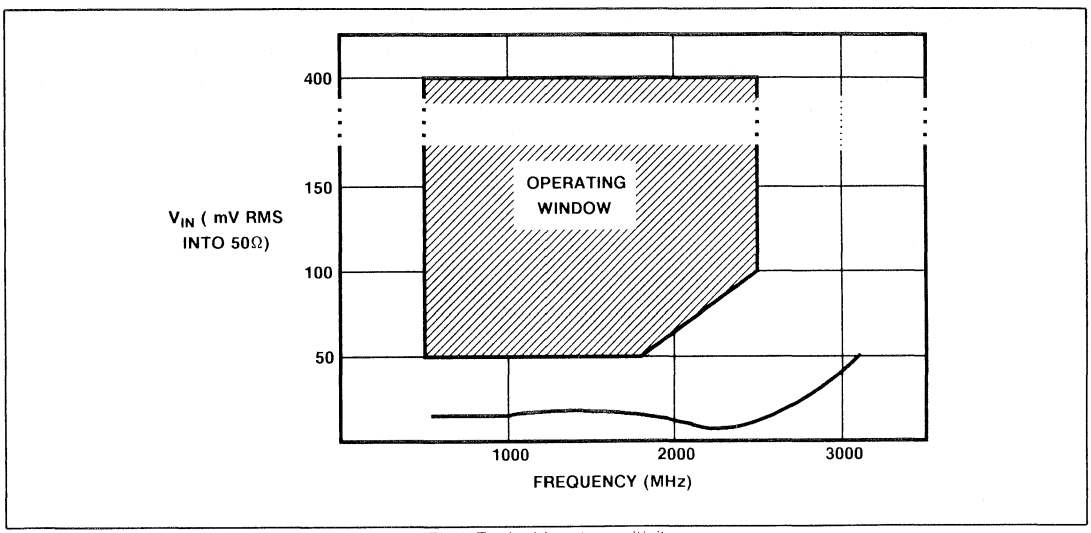


Fig.3 Typical input sensitivity

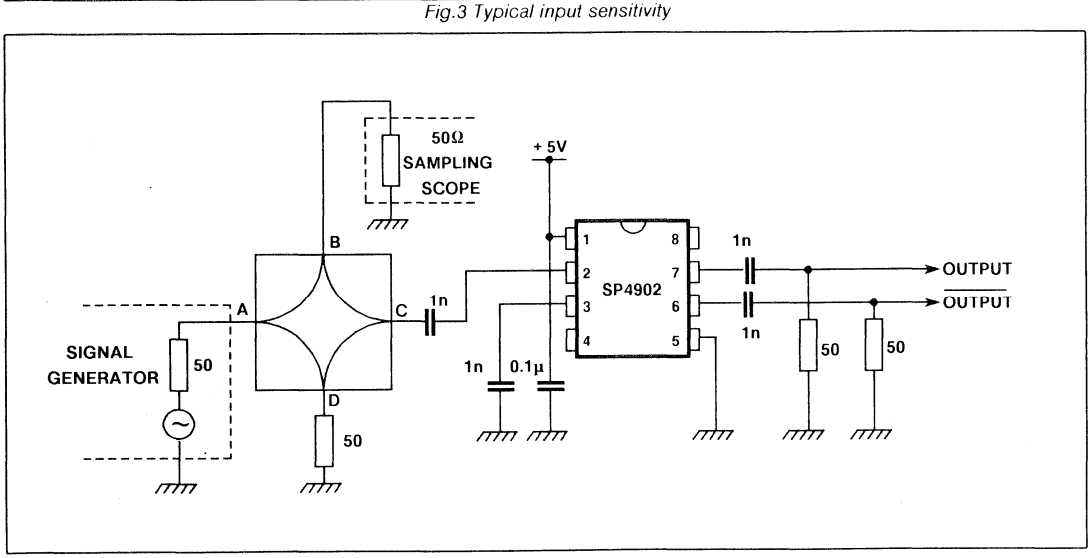


Fig.4 Test circuit

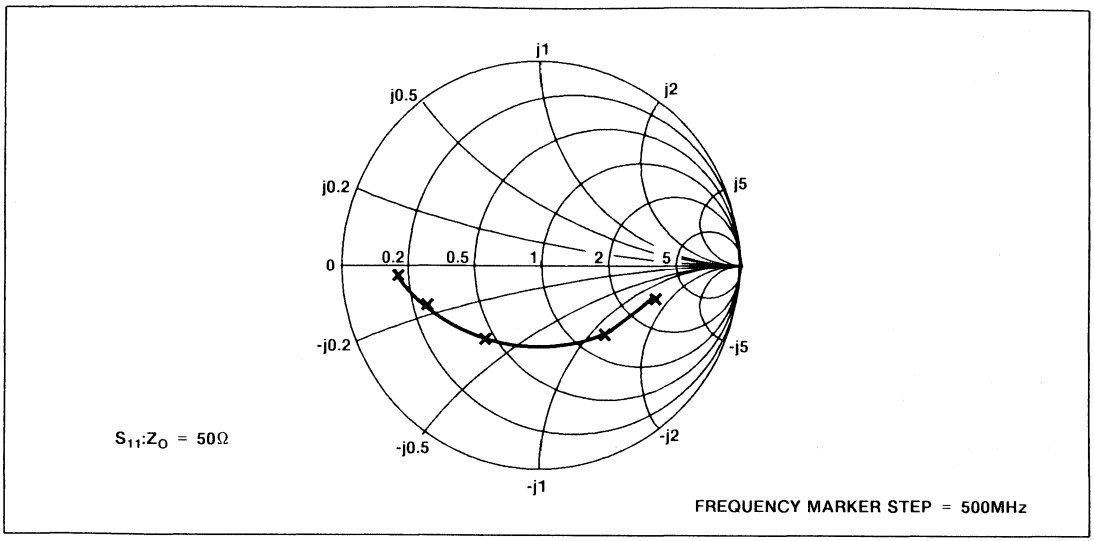


Fig.5 Typical input impedance

2245-1.0

SP4904

2.5GHz ÷ 4 PRESCALER

The SP4904 is one of a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 2.5GHz
- Silicon Technology for Low Phase Noise
- Very Low Power Dissipation 300mW
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Full ESD Protection

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

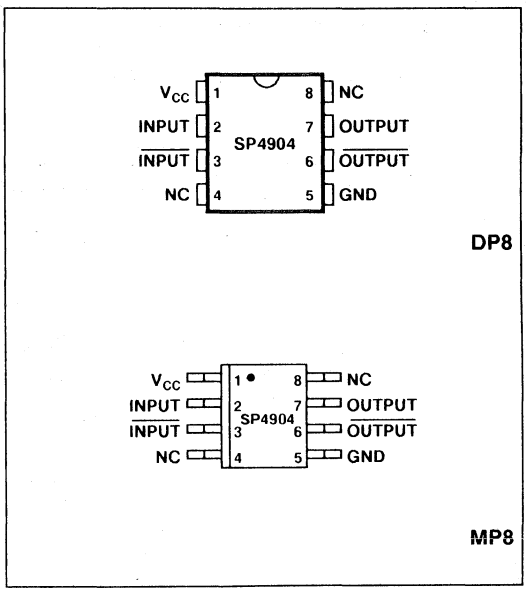


Fig 1 Pin Connections - top view

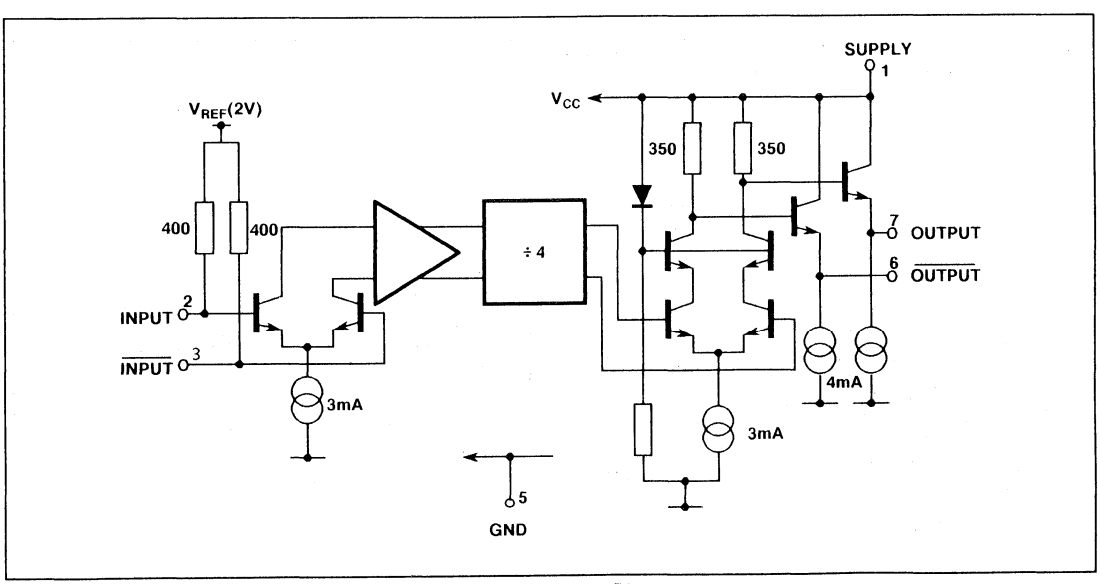


Fig 2 SP4904 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} = +4.75V to +5.25V Tamb = -10°C to +85°C

Characteristic	Pin.	Value			Units	Conditions
		Min.	Typ	Max.		
Supply current	1		60	75	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
500MHz to 1800MHz				50	mV	measured in 50Ω system. see
2500MHz				100	mV	Figs.3&4
Input impedance (series equivalvent)	2,3		50		Ω	
			2		pF	
Output voltage with fin = 500MHz	6,7	0.45	0.55		Vp-p	V_{CC} = 5V Load as Fig.4

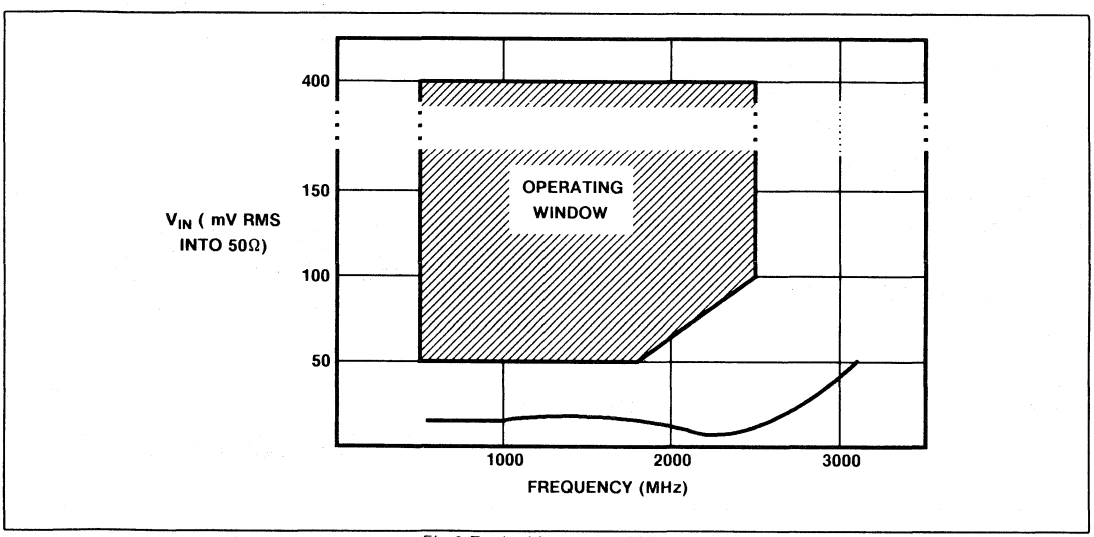


Fig.3 Typical input sensitivity

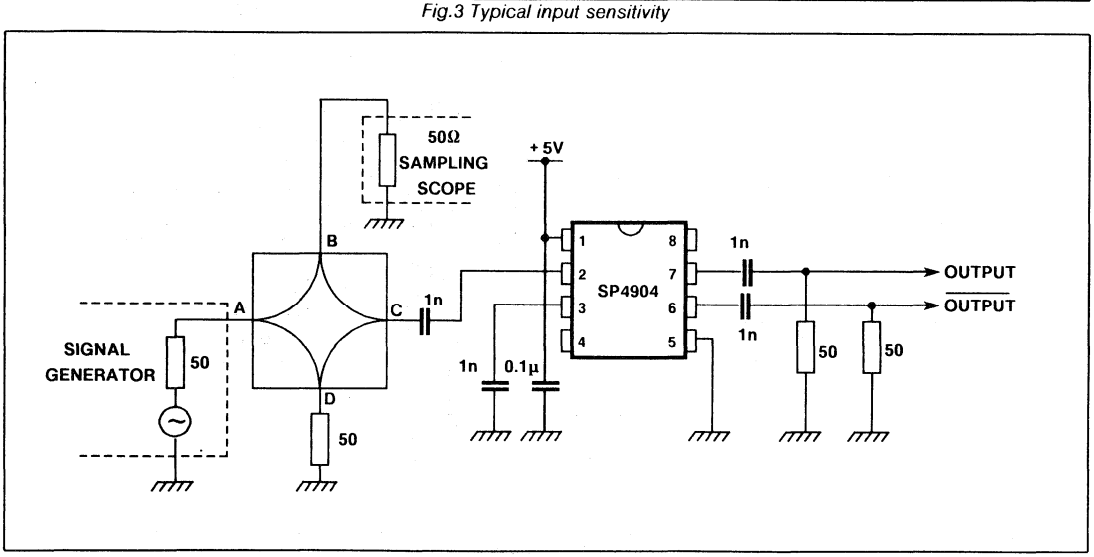


Fig.4 Test circuit

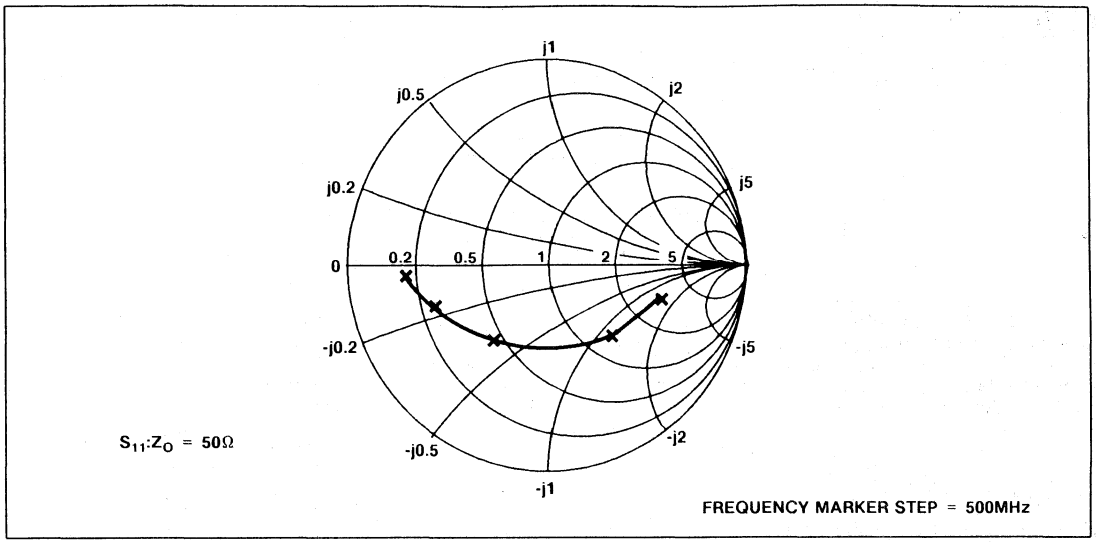


Fig.5 Typical input impedance

2273-1.0

SP4908

2.5GHz ÷ 8 PRESCALER

The SP4908 is one of a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 2.5GHz
- Silicon Technology for Low Phase Noise
- Very Low Power Dissipation 300mW
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Full ESD Protection

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

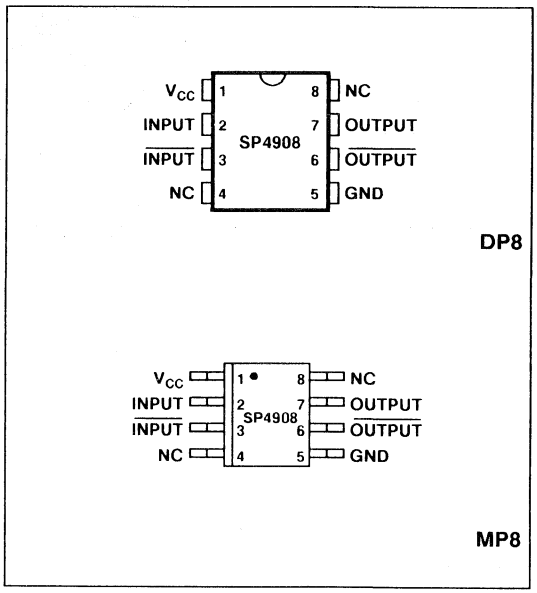


Fig 1 Pin Connections - top view

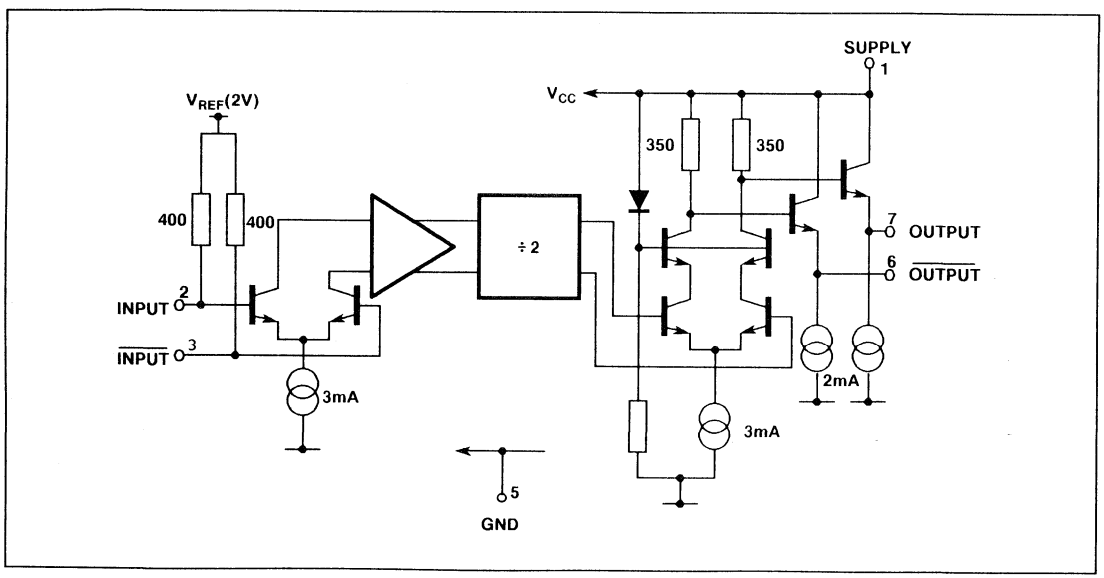


Fig 2 SP4908 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} = +4.75V to +5.25V Tamb = -10°C to +85°C

Characteristic	Pin.	Value			Units	Conditions
		Min.	Typ	Max.		
Supply current	1		60	75	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
500MHz to 1800MHz				50	mV	measured in 50Ω system. see
2500MHz				100	mV	Figs.3&4
Input impedance (series equivalvent)	2,3		50		Ω	
			2		pF	
Output voltage with fin = 500MHz	6,7	0.45	0.55		Vp-p	V_{CC} = 5V Load as Fig.4

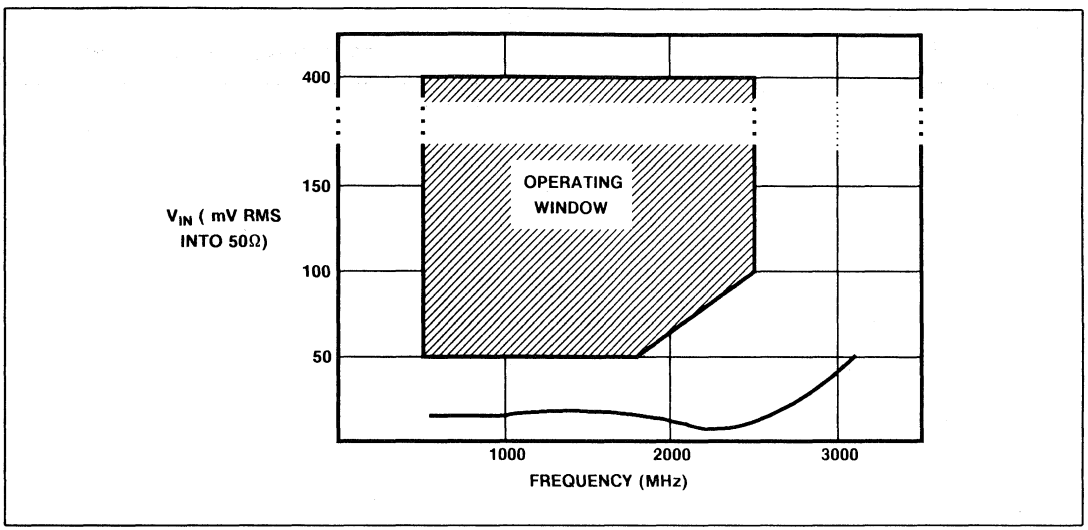


Fig.3 Typical input sensitivity

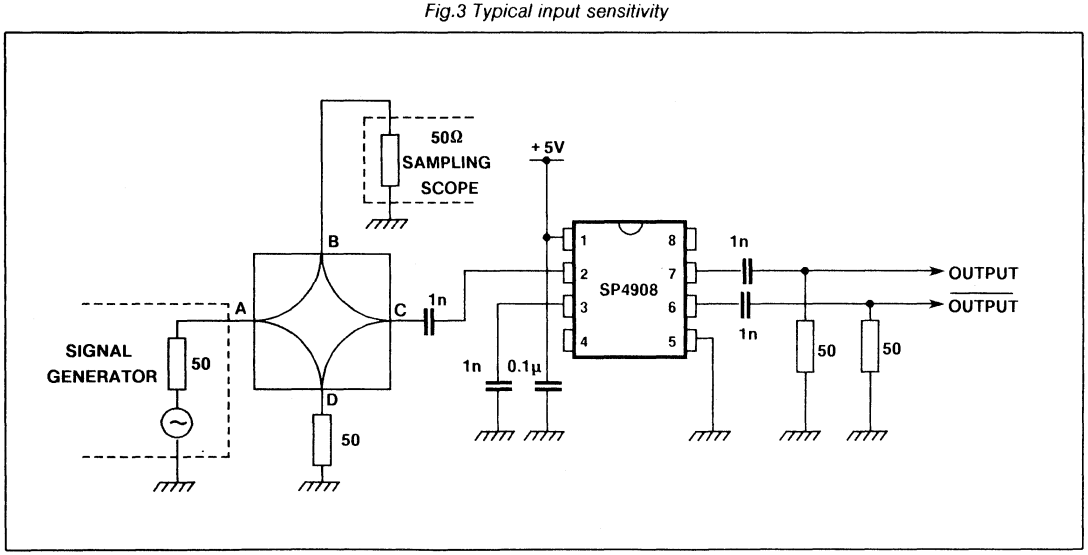


Fig.4 Test circuit

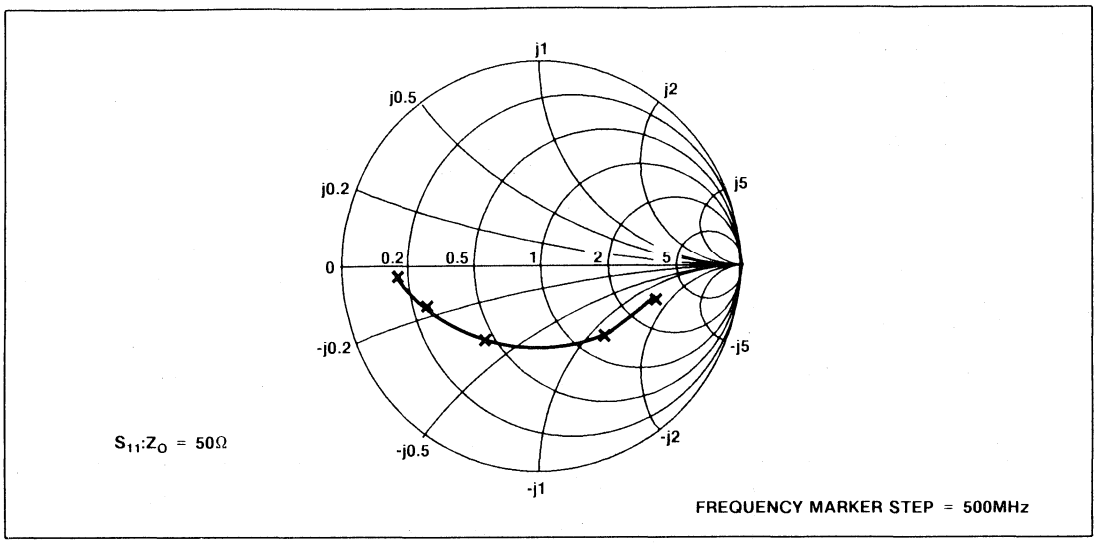


Fig.5 Typical input impedance

2274-1.0

SP4914

2.5GHz ÷ 128 PRESCALER

The SP4914 is one of a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage.

FEATURES

- High Speed Operation 2.5GHz
- Silicon Technology for Low Phase Noise
- Very Low Power Dissipation 250mW
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Full ESD Protection

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

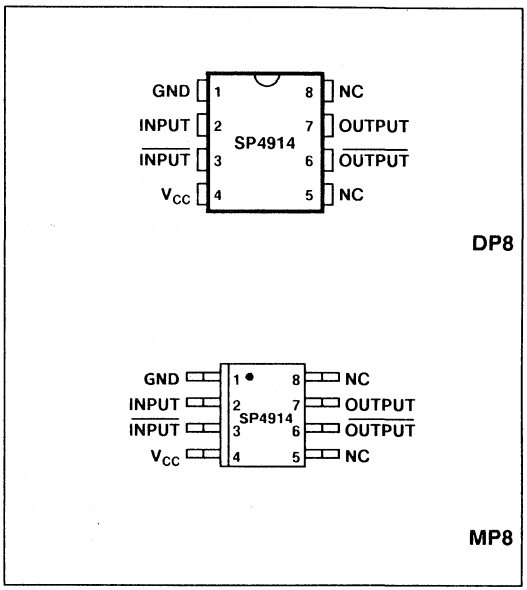


Fig 1 Pin Connections - top view

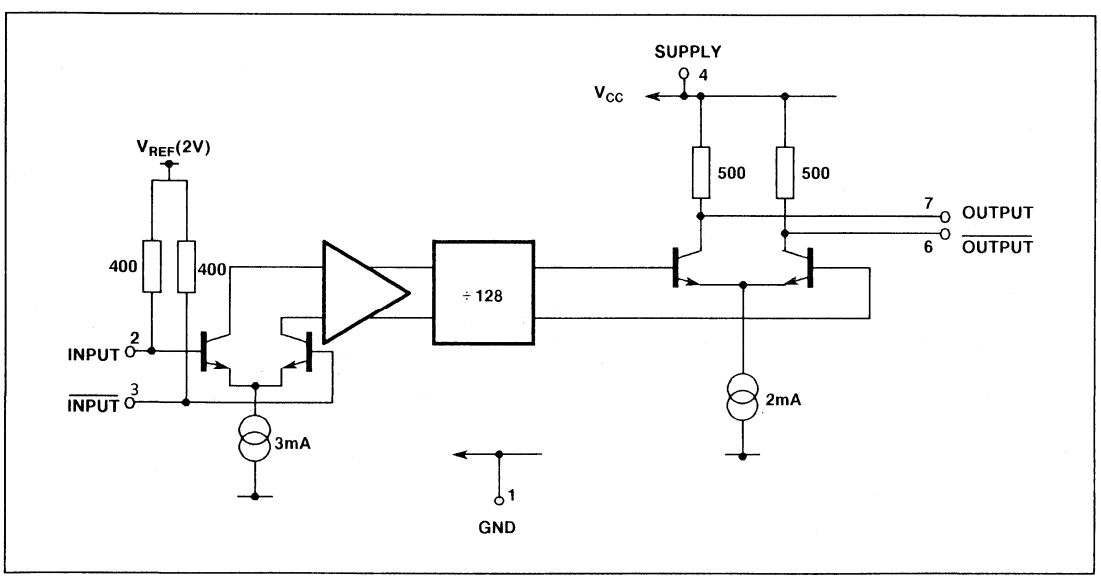


Fig 2 SP4914 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} = +4.75V to +5.25V Tamb = -10°C to +85°C

Characteristic	Pin.	Value			Units	Conditions
		Min.	Typ	Max.		
Supply current	4		50	65	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
500MHz to 1800MHz				50	mV	measured in 50Ω system. see
2500MHz				100	mV	Figs.3&4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with fin = 2500MHz	6,7	0.8	1		Vp-p	V_{CC} = 5V No load
Output voltage with fin = 2500MHz	6,7	0.5	0.8		Vp-p	V_{CC} = 5V Load as Fig.4

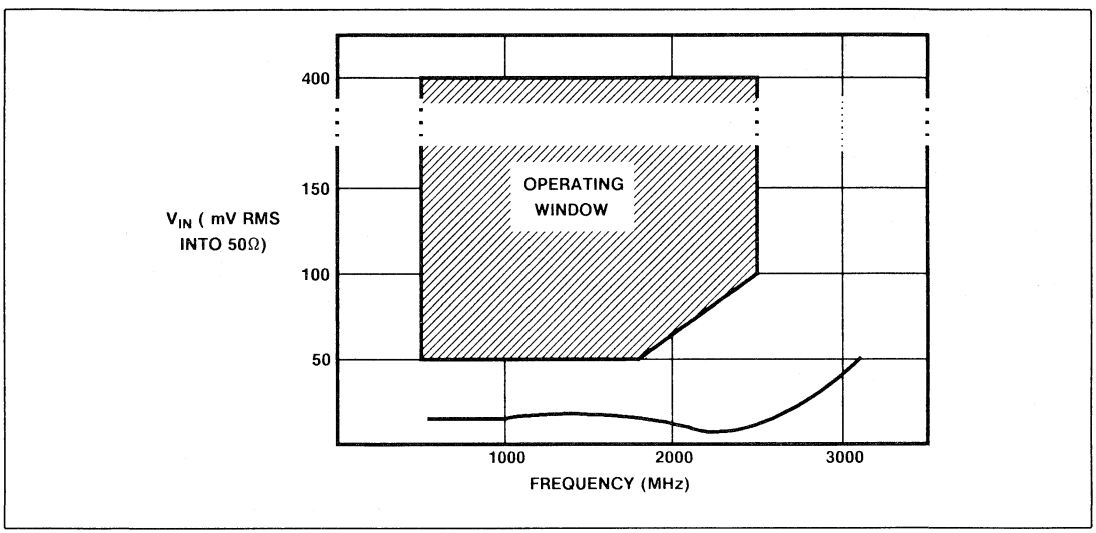


Fig.3 Typical input sensitivity

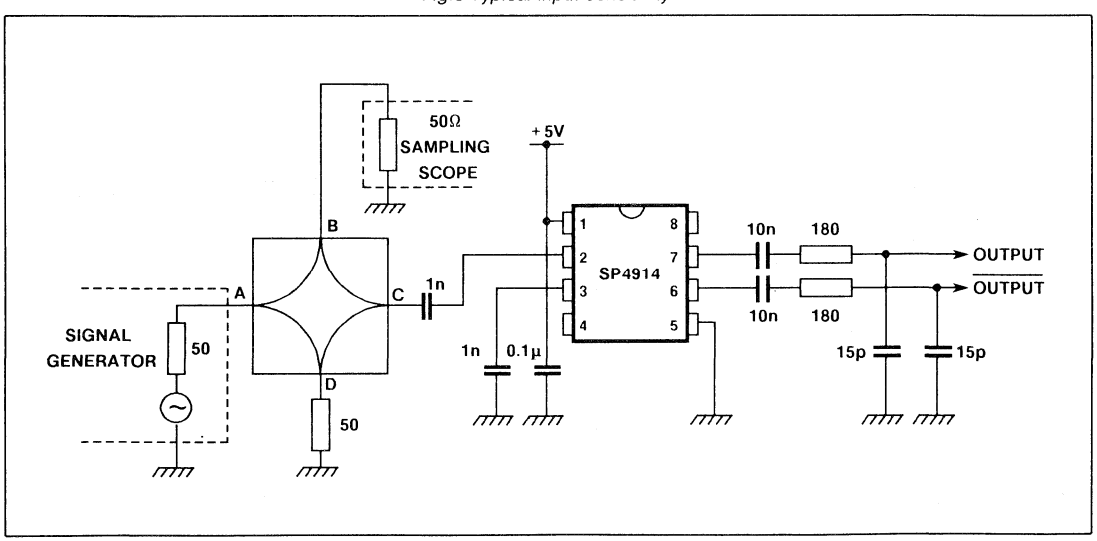


Fig.4 Test circuit

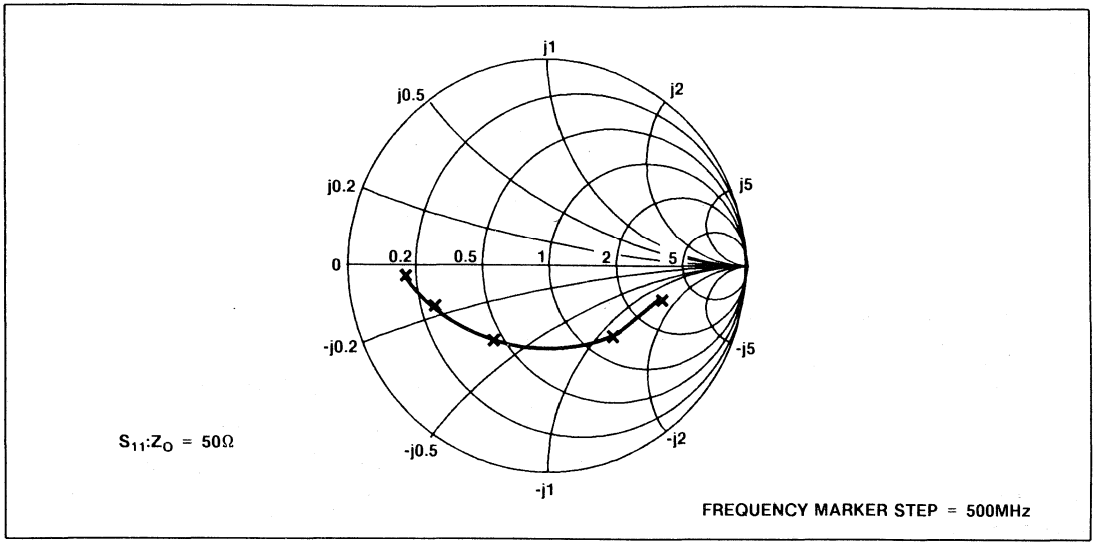


Fig.5 Typical input impedance

2275-1.0

SP4916

2.5GHz ÷ 512 PRESCALER

The SP4916 is one of a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage.

FEATURES

- High Speed Operation 2.5GHz
- Silicon Technology for Low Phase Noise
- Very Low Power Dissipation 250mW
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Full ESD Protection

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

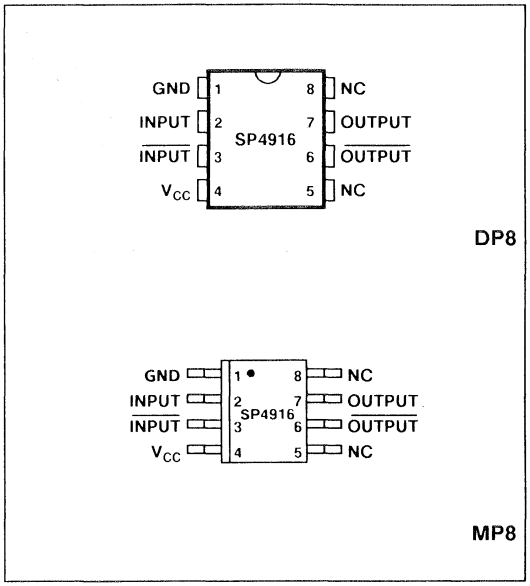


Fig 1 Pin Connections - top view

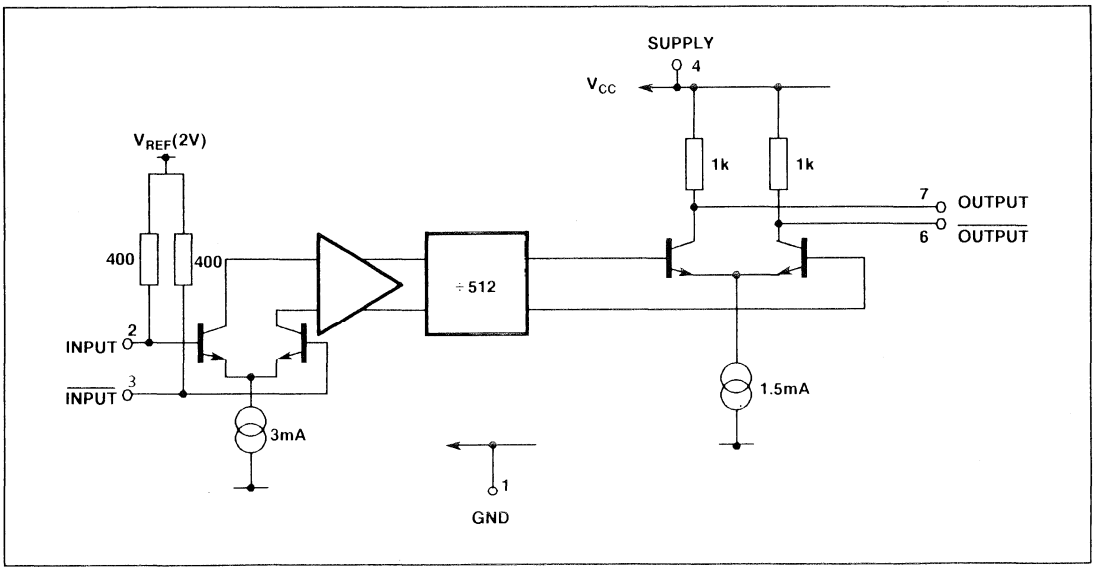


Fig 2 SP4916 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} = +4.75V to +5.25V Tamb = -10°C to +85°C

Characteristic	Pin.	Value			Units	Conditions
		Min.	Typ	Max.		
Supply current	4		50	65	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
500MHz to 1800MHz				50	mV	measured in 50Ω system. see
2500MHz				100	mV	Figs.3&4
Input impedance (series equivalvent)	2,3		50		Ω	
			2		pF	
Output voltage with fin = 2500MHz	6,7	1.2	1.5		Vp-p	V_{CC} = 5V No load
Output voltage with fin = 2500MHz	6,7	0.8	1.3		Vp-p	V_{CC} = 5V Load as Fig.4

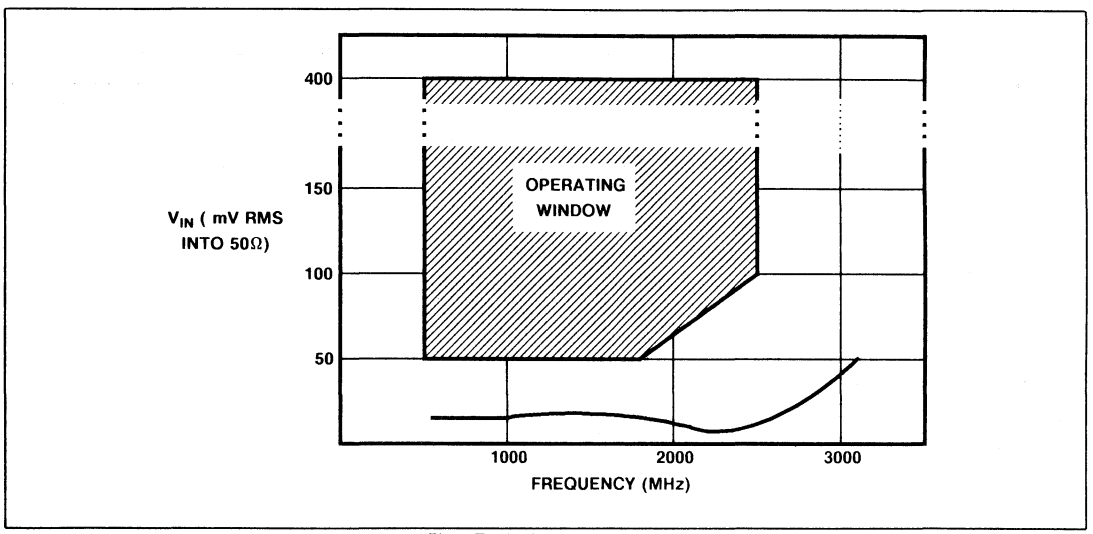


Fig.3 Typical input sensitivity

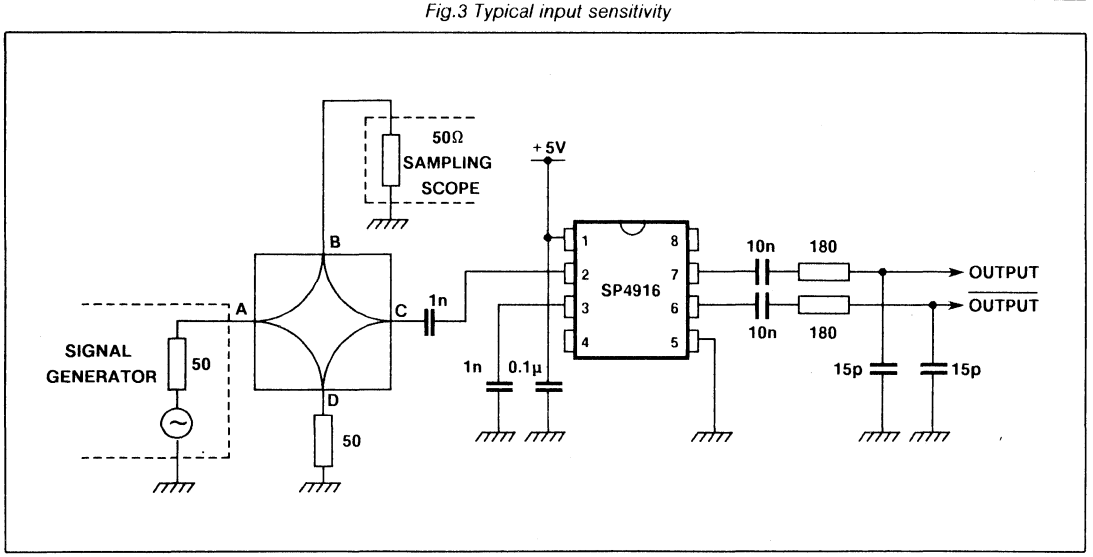


Fig.4 Test circuit

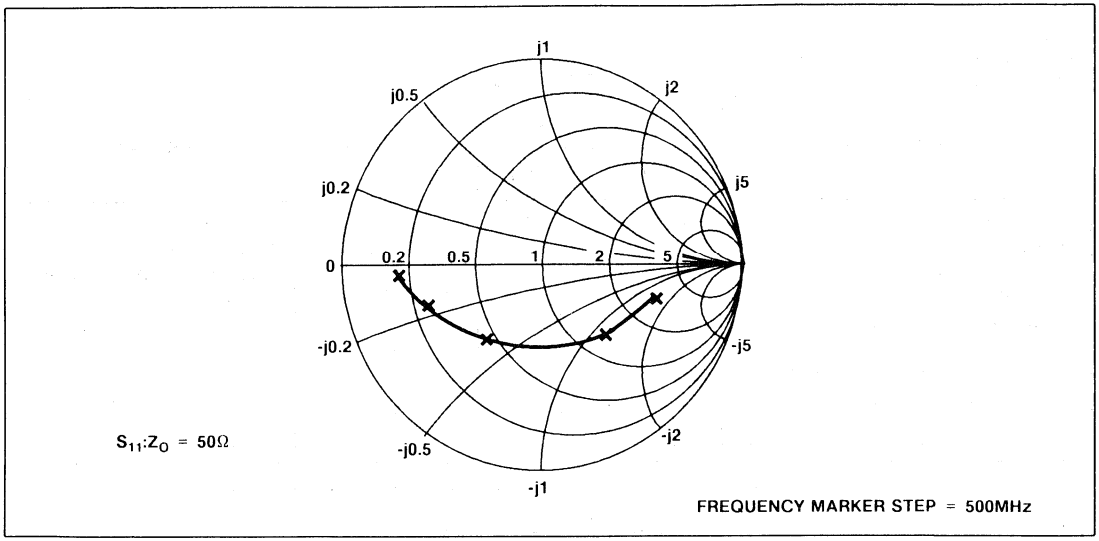


Fig.5 Typical input impedance

2276-1.0

SP4982

2.5GHz ÷ 8192 PRESCALER

The SP4982 is one of a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a CMOS compatible output stage.

FEATURES

- High Speed Operation 2.5GHz
- Silicon Technology for Low Phase Noise
- Very Low Power Dissipation 250mW
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Full ESD Protection

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

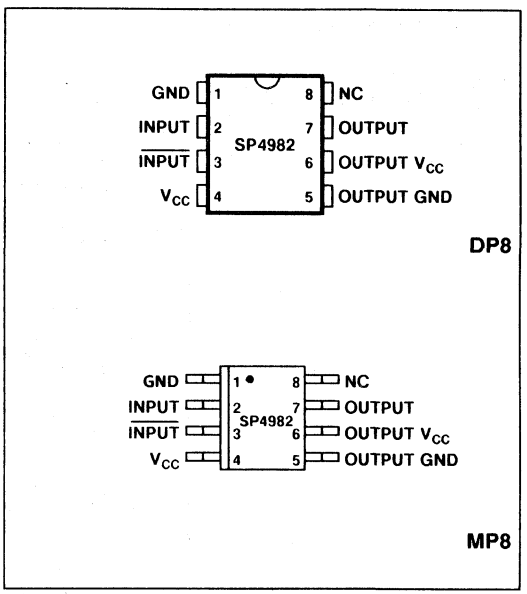


Fig 1 Pin Connections - top view

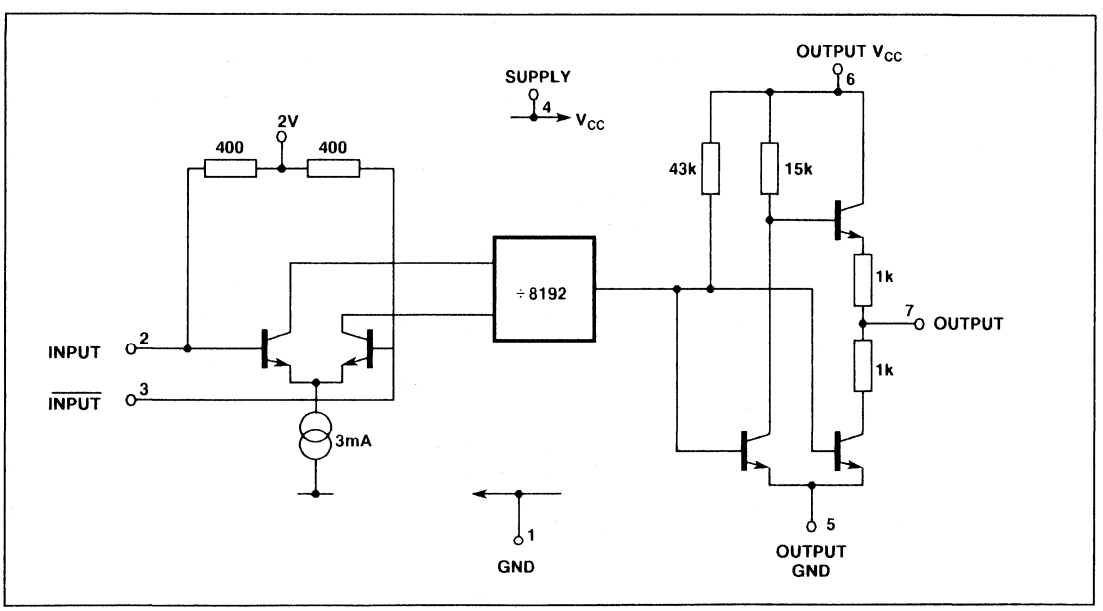


Fig 2 SP4982 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} = +4.75V to +5.25V Tamb = -10°C to +85°C

Characteristic	Pin.	Value			Units	Conditions
		Min.	Typ	Max.		
Supply current	4		44	65	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
500MHz to 1800MHz				50	mV	Measured in 50Ω system. see
2500MHz				100	mV	Figs.3&4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage high at f_{IN} = 2500MHz	7	V_{CC}–0.75			V	V_{CC} = 5V Load as Fig.4
Output voltage low at f_{IN} = 2500MHz	7			0.5	V	V_{CC} = 5V Load as Fig.4

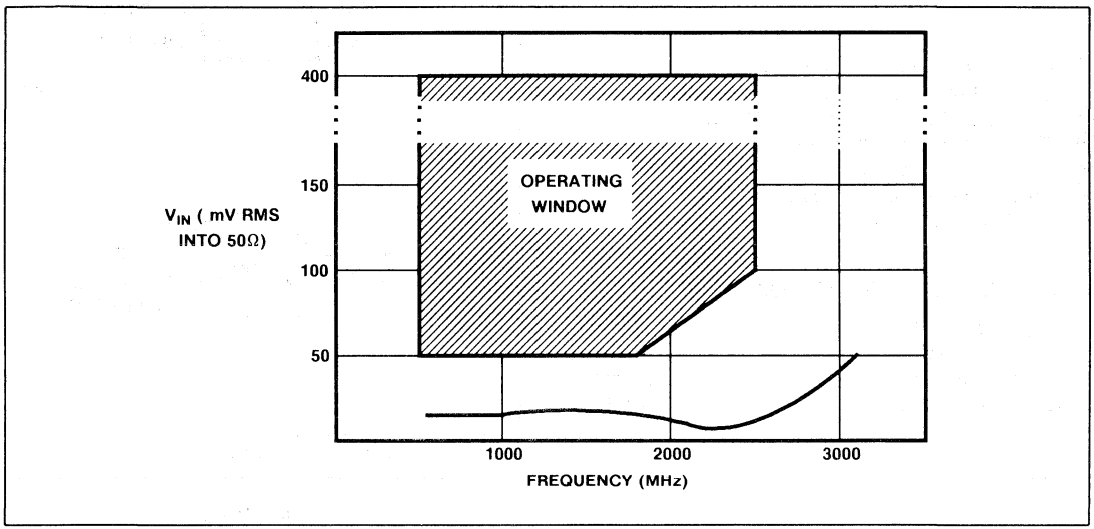


Fig.3 Typical input sensitivity

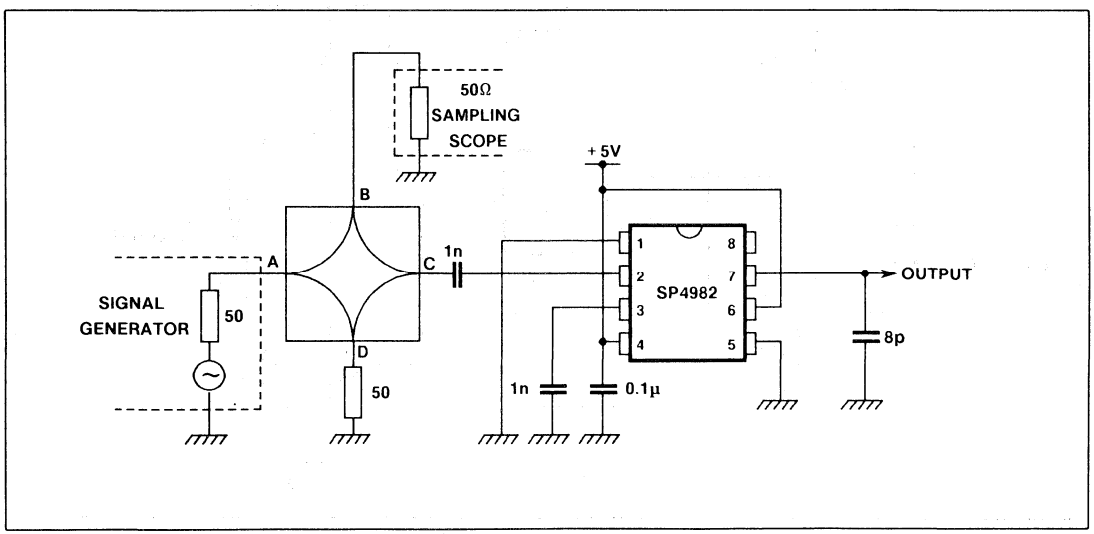


Fig.4 Test circuit

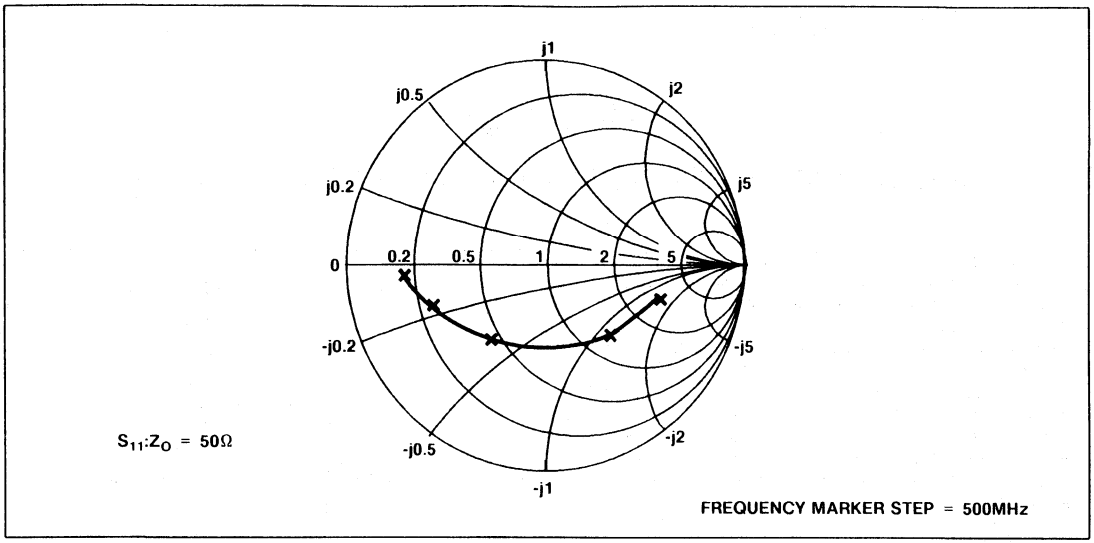


Fig.5 Typical input impedance

SP5000A

SINGLE CHIP FREQUENCY SYNTHESISER FOR TV TUNING

The SP5000A used with a TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide-by-16 prescaler with its own preamplifier and a 14 bit programmable divider controlled by a serially-loaded data register. Band selection lines are also included and give 4 switch output combinations on 3 lines. The frequency/phase comparator is fed with a 3.90625kHz reference, derived from the 4MHz crystal controlled on-chip oscillator. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

FEATURES

- Complete Single Chip System for Microprocessor Control
- Operating Supply 5V, 60mA
- Prescaler and Preamplifier Included
- Single Port 16-bit Serial Data Entry
- Frequencies up to 1024MHz in 62.5kHz Steps (with 4.0MHz Ref)
- High Comparator Frequency Simplifies Charge Pump Filter
- Frequency Band Select Outputs
- Charge Pump Amplifier with Feedback and Disable
- Crystal Controlled Output Clock at 62.5kHz

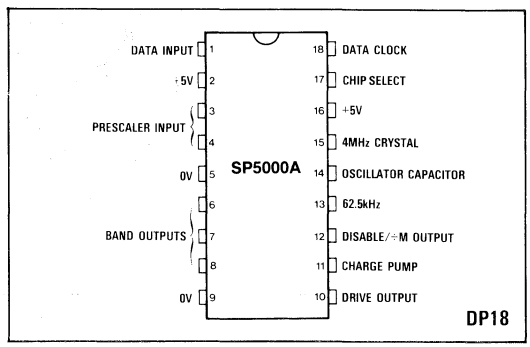


Fig.1 Pin connections - top view

Band select data		Band outputs Pin		
2^{15}	2^{14}	6	7	8
0	0	H	H	H
0	1	H	L	H
1	0	L	H	H
1	1	H	H	L

Table 1 Band select decoding

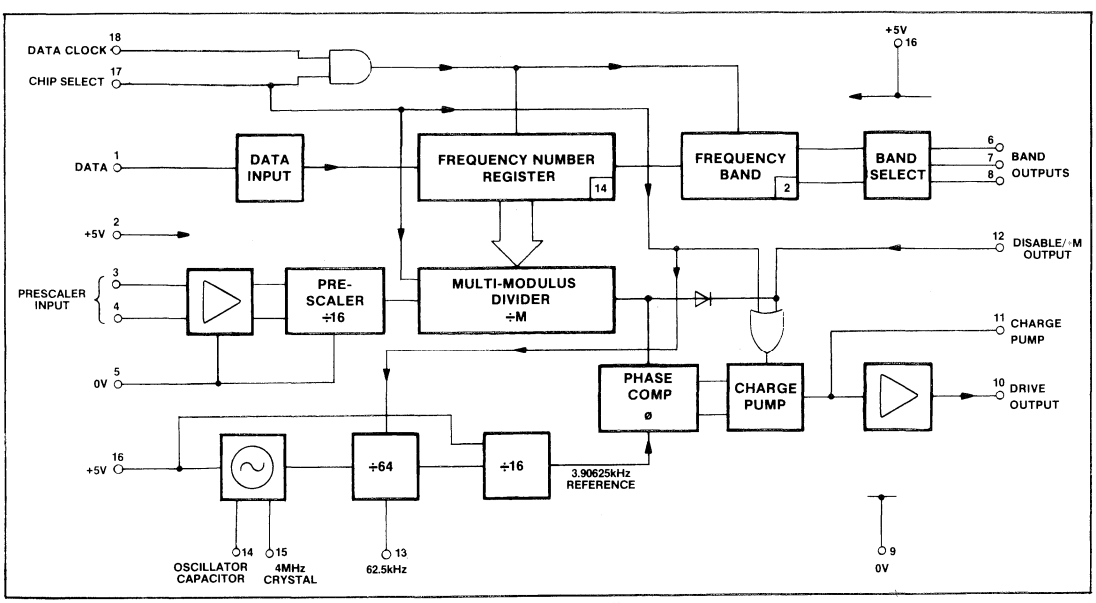


Fig.2 SP5000A block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{CC} = 5V, Frequency standard = 4MHz

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Operating voltage	V_{CC}	2,16	4.5		5.5	V	
Supply current	$I_{CC}(2)$	2		50	65	mA	
Supply current	$I_{CC}(16)$	16		1		mA	
Prescaler input voltage		3,4	17.5		200	mV	80MHz to 1GHz sinewave. See Fig.4
Prescaler input impedance		3,4		50		Ω	See Fig.5
High level input voltage		1,12,17,18	3.5		V_{CC}	V	
Low level input voltage		1,12,17,18	0		1.5	V	
High level input current		1,12,17			0.4	mA	V_{IN} = 5V
Input current		18			5	μA	V_{IN} = 3.5V
Multi-modulus divider		12		350		mV	6.8k to 0V. Provided for test purposes only.
Data clock input hysteresis		18		0.6		V	
Data clock rate		18			0.5	MHz	
Data setup time	t_{setup}	1,18	0.5			μs	See Fig.3
Chip select timing	csd(pos)	17,18	0		tc	μs	See Fig.3
Chip select timing	csd(neg)	17,18	0.5			μs	See Fig.3
External oscillator input		14,15		250		mV	AC coupled
Charge pump output current		11	±75	±100	±125	μA	V Pin 11 = 2.0V
Charge pump output leakage		11			±1	μA	V Pin 11 = 2.0V
Drift due to leakage					5	mV/s	At collector of external varicap drive transistor
Oscillator temperature stability		14,15		0.12		ppm/°C	Over 0°C to 65°C temperature range. IC variation only
Oscillator stability with supply voltage		14,15		0.25		ppm/V	V_{CC} = 4.5V to 5.5V
Charge pump drive output current	I_{OUT}	10	1			mA	V Pin 10 = 0.7V
Band output leakage current		6,7,8			5	μA	V Pins 6,7 and 8 = 13.5V
Band output current		6,7,8	1	1.3		mA	V_{OUT} = 12V
Clock output leakage current		13			5	μA	V Pin 13 = 5.5V
Clock output saturation voltage		13			0.5	V	I Pin 13 − 1mA

DESCRIPTION

The phase comparator reference frequency at 3.90625kHz is obtained by division of the 4MHz on chip crystal controlled oscillator frequency. An output at 62.5kHz for driving the SP5010 in cable TV applications is provided at Pin 13.

In order to achieve a high sensitivity at the tuner local oscillator pick off point, the divide-by-sixteen prescaler is preceded by a differential amplifier with inputs on Pins 3 and 4. A simple filter arrangement is necessary at the inputs to prevent loading by the unused oscillator output when operation at both UHF and VHF frequencies is required.

The divide-by-sixteen prescaler output drives the multi-modulus divider, which, when the loop is locked, produces an output, frequency and phase locked to the 3.90625kHz reference.

Synthesis of the complete range of frequencies required for both off air and cable TV reception is provided by varying the division ratio of the multi-modulus divider according to data applied from an external control system. The data, applied as a 16 bit serial word, is loaded using the data clock and select lines from the control system into a storage register with fourteen bits controlling the multi-modulus divider, and the remaining bits the band select outputs on Pins 6, 7 and 8.

Data from the serial input, Pin 1 is clocked into the storage register by the positive edge of the data clock waveform on Pin 18 when the chip select input on Pin 17 is high. The chip select input should be timed to go high during the low portion of the clock waveform otherwise a positive transition coincident with the select signal will be applied to the storage register clock possibly causing a misreading of the applied data.

Figure 3 and Table 1 show the data format and timing requirements.

A single external transistor driven from the charge pump output provides the 30V swing necessary on the tuner varicap input. To prevent unwanted frequency variations when data is being entered, the charge pump is disabled by chip select.

Pin 12 is a dual input/output pin, the normal function being to disable the charge pump when the input is taken high. The alternative output function is provided for test purposes only and allows the ÷M counter output to be monitored. This signal is available at low amplitude when Pin 12 is loaded to ground by a 6.8k resistor.

To improve stability the +5V and ground supplies to the chip are split and brought out to separate pins, it is therefore essential to connect all four supply pins for the device to operate.

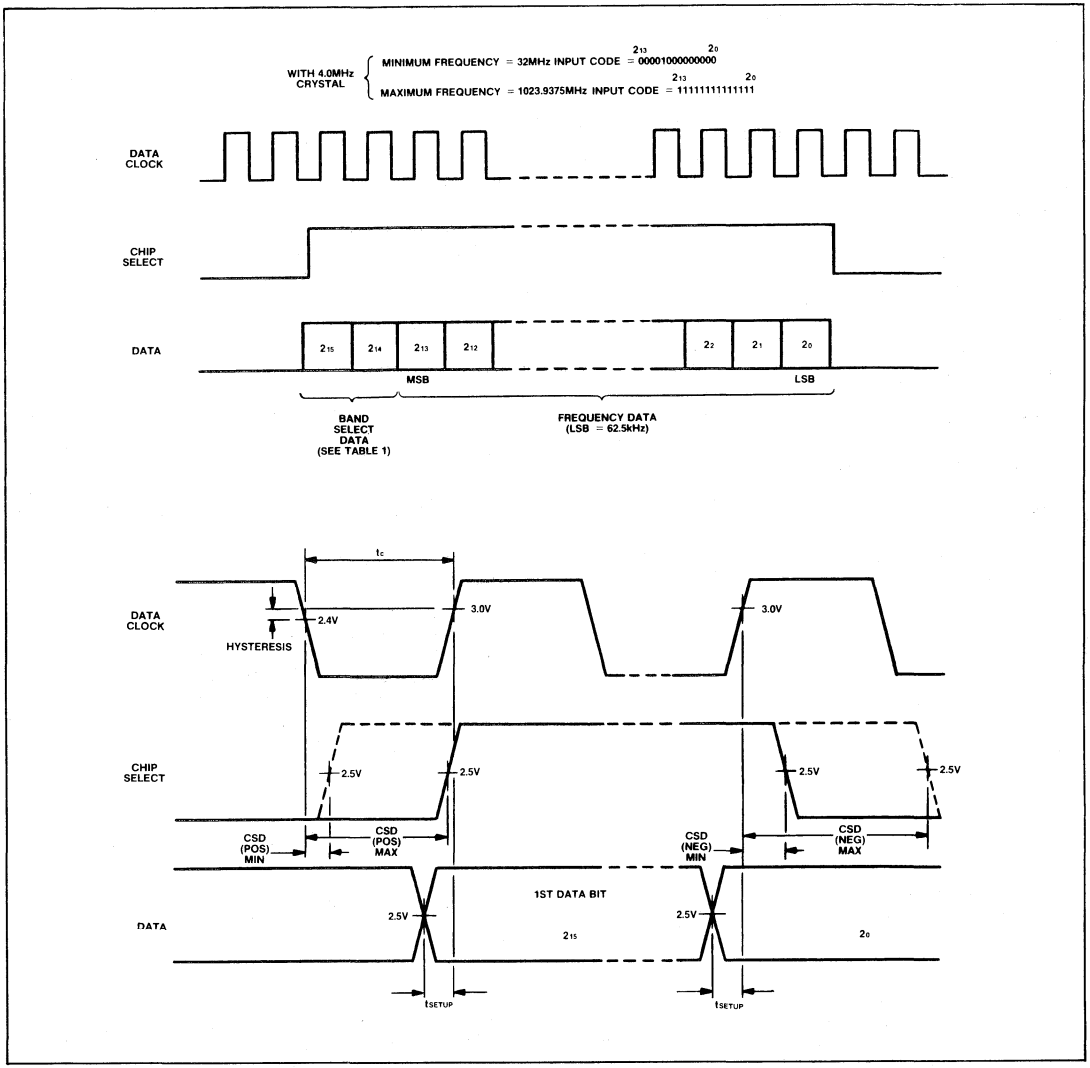


Fig.3 Data format and timing

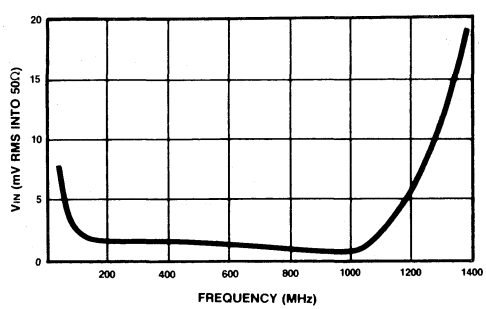


Fig.4 Typical input sensitivity of prescaler

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature: -10° C to +65° C
Storage temperature: -55° C to +125° C
Supply voltage Pin 2 and 16: 7V
Band select output voltage Pins 6,7,8: 14V
Prescaler input voltage: 2.5V p-p

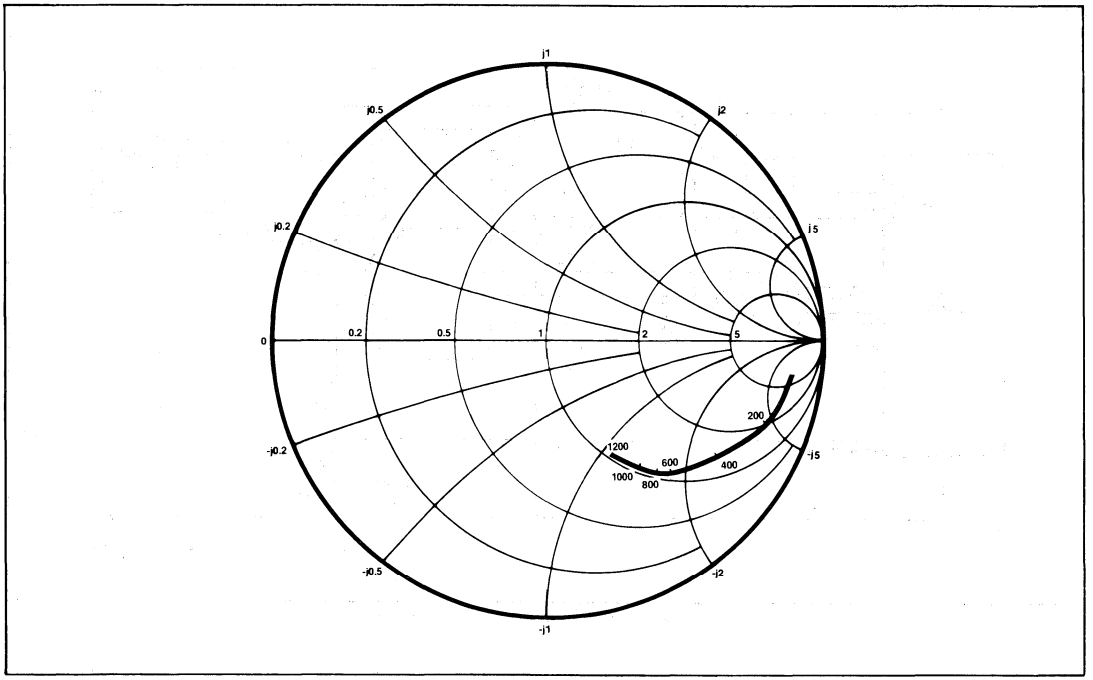


Fig.5 Typical input impedance frequencies in MHz. Normalised to 50 Ω

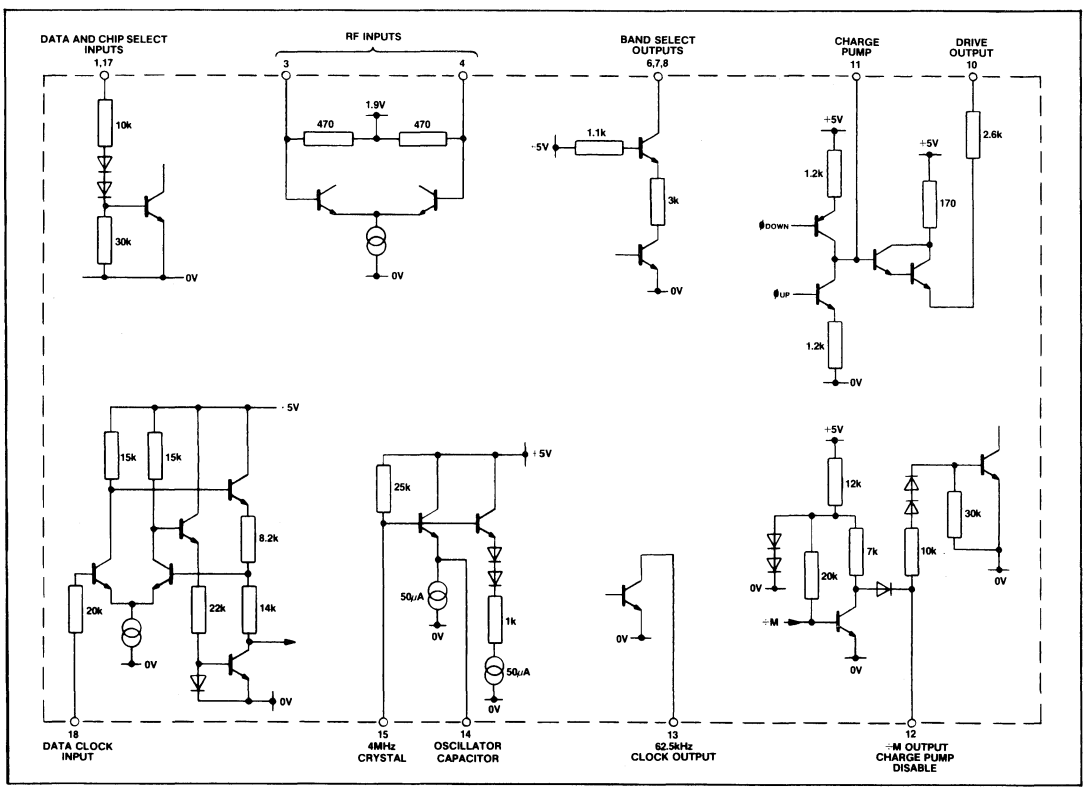


Fig.6 SP5000A input/output interface circuits

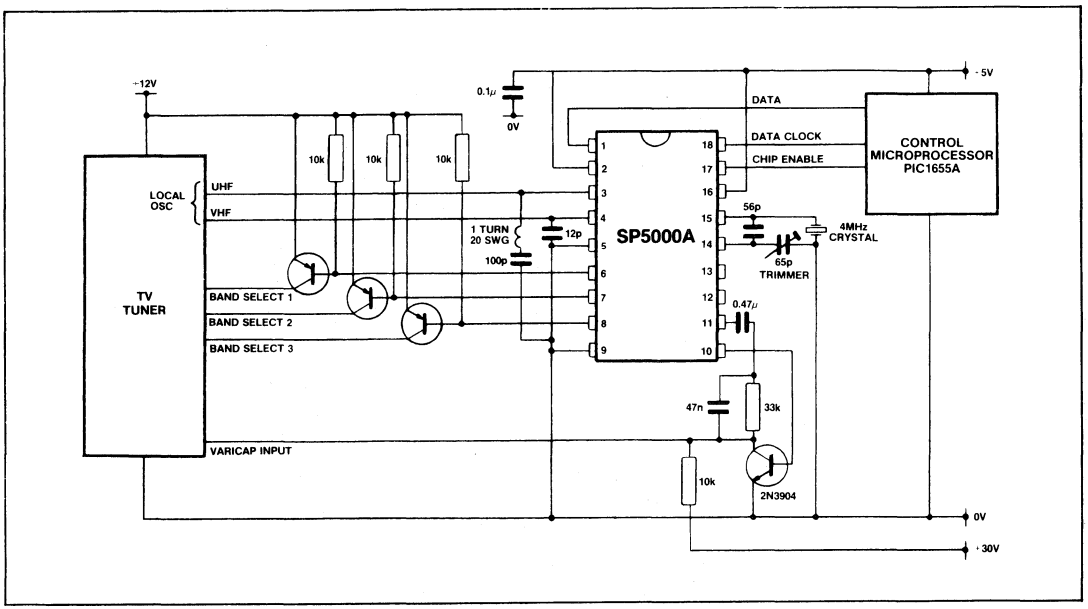


Fig.7 Typical TV application for 3 band reception

SP5011

CABLE TV PLL CONVERTER

The SP5011, together with an appropriate voltage controlled oscillator (VCO), forms a complete phase locked loop (PLL) synthesiser with 8-channel frequency selection. It consists of a prescaler with preamplifier and a divider which is programmable by means of link options on three pins. The frequency standard is derived from a 4MHz crystal controlled on-chip oscillator. A phase/frequency comparator operating at 3.90625kHz feeds a charge pump outout with an amplifier stage around which a feedback filter may be applied.

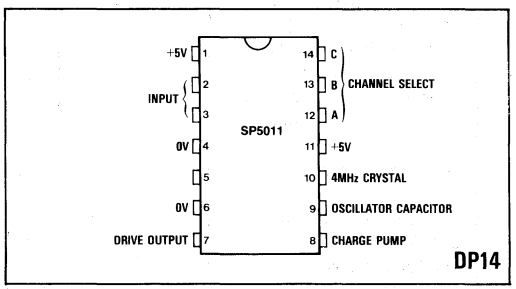


Fig.1 Pin connections - top view

FEATURES

- Complete 8-Channel System with Control
- +5V, 50mA Supply
- Prescaler and Preamplifier Included
- Frequencies Selected by Wire Links
- High Comparator Frequency for Easier Filtering
- Charge Pump Amplifier with Feedback Point
- 4MHz Crystal

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	-10° C to +65° C
Storage Temperature	-55° C to +125° C
Supply Voltage Pin 1 and Pin 12	7V
Prescaler Input Voltage	2.5V p-p

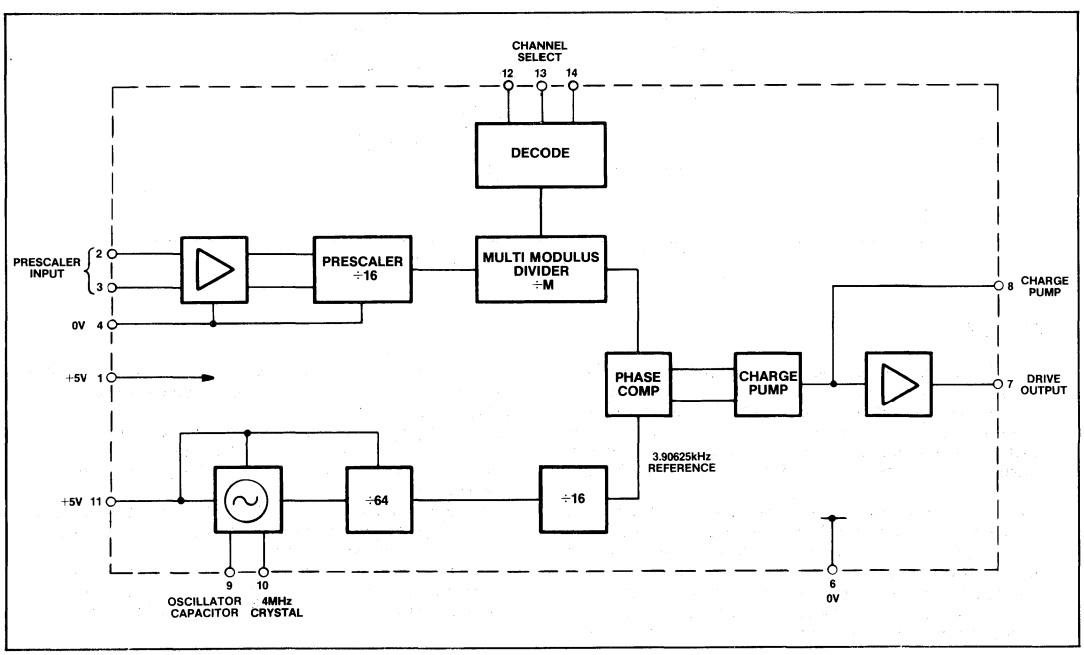


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)
T_{amb} = +25° C; V_{CC} = +5V

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Operating voltage	V_{CC}	1,11	4.5		5.5	V	
Supply current	I_{CC} (1)	1		50	60	mA	
Supply current	I_{CC} (11)	11		1		mA	
Prescaler input voltage		2,3	17.5		200	mV	RMS into 50Ω
Prescaler input impedance		2,3		50		Ohms	
High level input voltage		12,13,14	3.5V		V_{CC}	V	
Low level input voltage		12,13,14	0		1.5	V	
High level input current		12,13,14			0.4	mA	V_{in} = 5V
Charge pump output current		8	±75	±100	±125	μA	V pin 8 = 2.0V
Charge pump leakage current		8			±1	μA	V pin 8 = 2.0V
Charge pump drive output current		7	1			mA	V pin 7 = 0.7V
Drift due to leakage				5		mV/s	At collector of external varicap drive transistor
Oscillator temperature stability		9,10		0.12		PPM/° C	Over 0 to 65° C temperature range IC variation only
Oscillator stability with supply voltage		9,10		0.25		PPM/V	V_{CC} = 4.5V to 5.5V

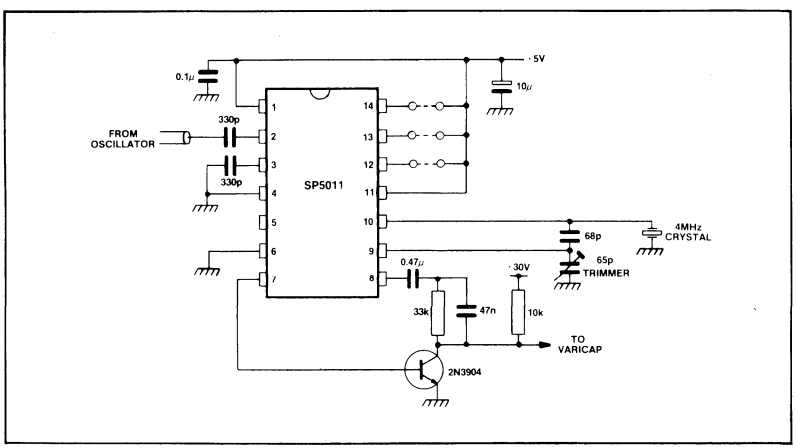


Fig.3 Typical application and test circuit

DESCRIPTION

The SP5011 when used with a voltage controlled oscillator form complete phase locked loop frequency synthesisers. Eight possible output frequencies are selectable by three wire links on each device. The SP5011 is intended to synthesise the 2nd LO frequency in American cable TV convertors using an IF frequency of 612.75MHz.

A phase comparator reference frequency of 3.90625kHz is obtained by division of a 4MHz reference frequency which may be generated on chip or applied externally from the SP5000 reference oscillator where this is used.

In order to achieve a high sensitivity at the local oscillator pick off point the divide by sixteen prescaler is preceded by a differential amplifier with inputs on pins 2 and 3. The prescaler output is further divided by the multi-modulus divider, producing an output which is phase locked to the 3.90625kHz reference.

By changing the code on the channel select inputs on pins 12, 13 and 14 the division ratio of the multi-modulus divider can be changed to allow synthesis of eight local oscillator frequencies.

A single external transistor driven from the charge pump output provides the output swing necessary for the local oscillator varicap control line.

To improve device stability the +5V and ground supplies to the chip are split and brought out to separate pins. It is therefore essential to connect all supply pins for the device to operate.

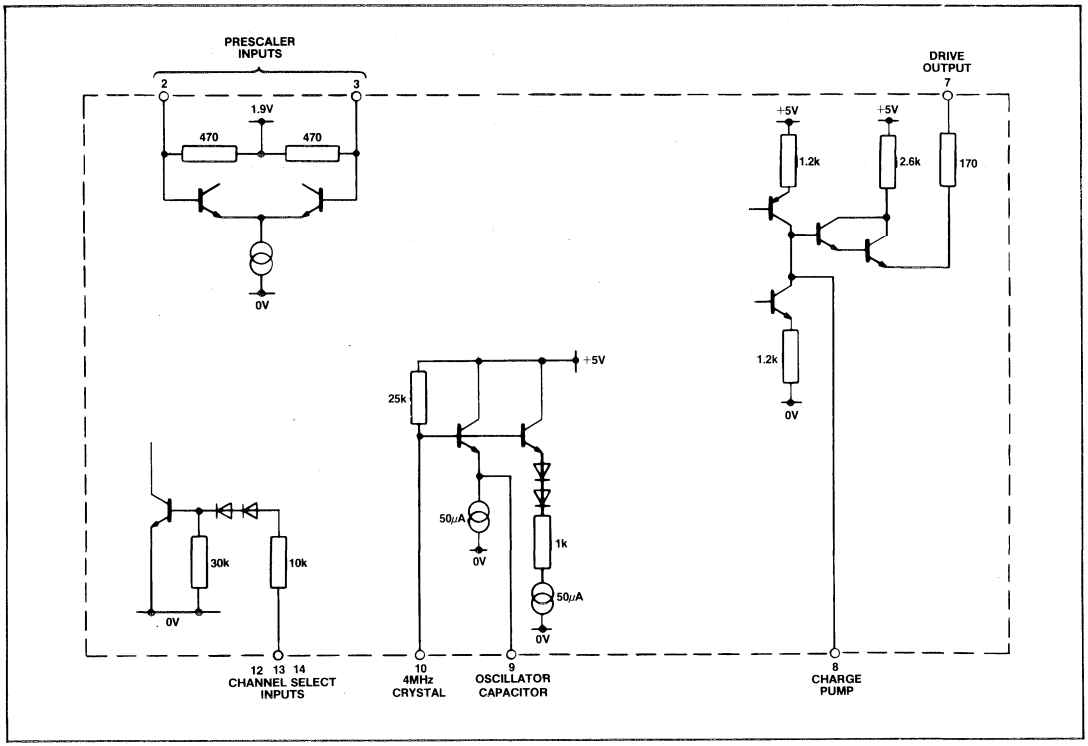


Fig.4 SP5011 input/output interface circuits

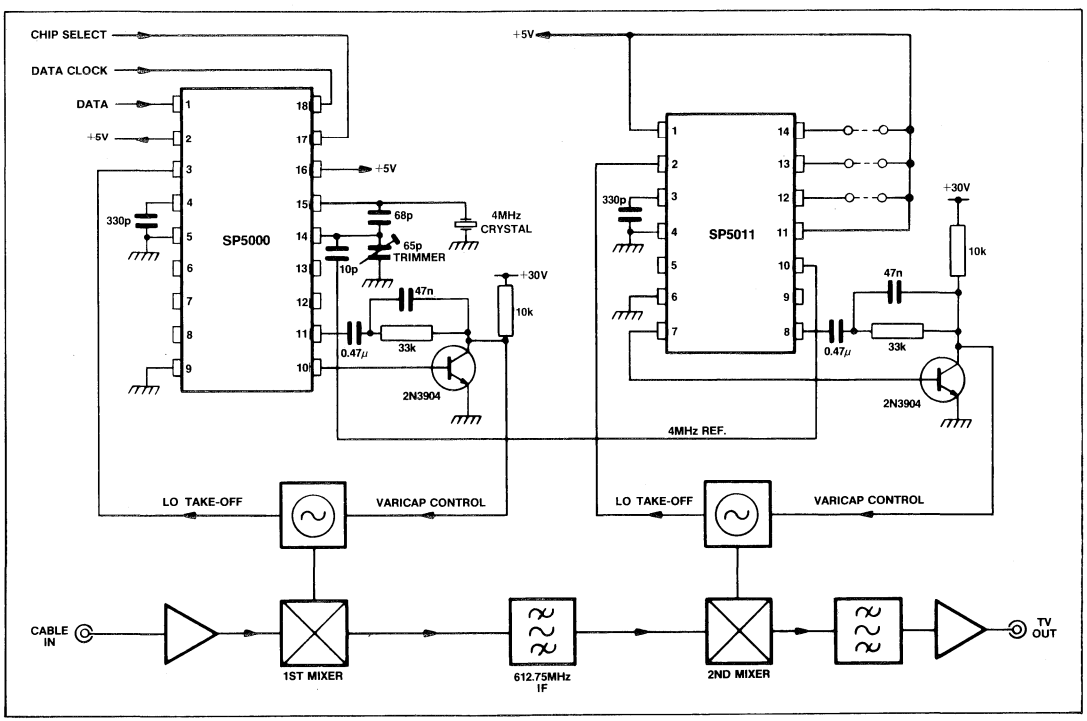


Fig.5 Cable TV set top converter

A Pin 12	B Pin 13	C Pin 14	SP5011 (2nd IF frequency = 612.75MHz)		
			USA channel	Synthesised frequency	Mixer output frequency
0	0	0	5	690MHz	77.25MHz
0	0	1	6	696MHz	83.25MHz
0	1	0	3 vision carrier	61.25MHz	-
0	1	1	4 vision carrier	67.25MHz	-
1	0	0	3	674MHz	61.25MHz
1	0	1	2	668MHz	55.25MHz
1	1	0	4	680MHz	67.25MHz
1	1	1	TV IF	567MHz	45.75MHz

Table 1 Channel selection coding for SP5011

SP5020

1.3GHz 3-WIRE BUS CONTROLLED SYNTHESISER

The SP5020, when used with a TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide-by-8 prescaler with its own preamplifier and a 15-bit programmable divider controlled by a serially-loaded data register. Four band selection lines, BS0-BS3, are included. The frequency/phase comparator is fed with a switchable 7.8125kHz or 3.90625kHz reference, derived from the 4MHz crystal controlled on - chip oscillator. The comparator has a charge pump output with an amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

FEATURES

- Complete 1.3GHz Single Chip System
- Switchable 7.8125kHz or 3.90625kHz Reference
- Low Power Consumption (5V 30mA)
- Low Radiation
- Phase Lock Indication
- Charge Pump Disable
- Single Port 19-Bit Serial Data Entry
- 4 Band Select Outputs
- Compatible with Toshiba TD6381, TD6382, TD6359, Mitsubishi M54965 and M54939 *
- Full ESD Protection †

* See notes on device compatibility, page 1-62

† Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV when combined with SP4902 2.5GHz Prescaler
- Cable tuning Systems
- VCRs

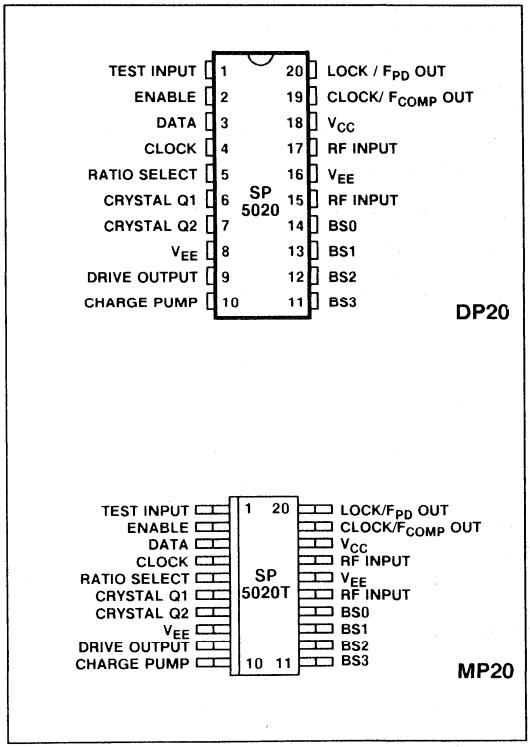


Fig.1 Pin connections - top view

ORDERING INFORMATION

SP5020 DP - (20 lead Plastic package)
SP5020T MP - (20 lead Miniature Plastic package)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = -10°C to +80°C, V_{CC} = +4.5V to +5.5V, Frequency Standard = 4MHz

These characteristics are guaranteed by production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	18		30	38	mA	
Prescaler input voltage		15, 17	10		300	mV_{RMS}	50MHz to 1GHz sinewave
Prescaler input voltage		15, 17	30		300	mV_{RMS}	1.3GHz, see Fig. 5
Prescaler input impedance Input capacitance		15, 16		50 2		Ω pF	
High level input voltage		1,2,3,4	2.7		V_{CC}	V	
High level input voltage		5	3.0		V_{CC}	V	
Low level input voltage		1,2,3,4			0.7	V	
Low level input voltage		5			1.5	V	
High level input current		1,3,4			1	μA	V_{IN} = 5.5V, V_{CC} = 5.5V
High level input current		2			+10	μA	V_{IN} = 5.5V, V_{CC} = 5.5V
Low level input current		1,3			-200	μA	V_{IN} = 0V, V_{CC} = 5.5V
Low level input current		2			-1.25	mA	V_{IN} = 0V, V_{CC} = 5.5V
Low level input current		5			-1	μA	V_{IN} = 0V, V_{CC} = 5.5V
High level input current		5			150	μA	V_{IN} = 5.5V, V_{CC} = 5.5V
Low level input current		4			-5	μA	V_{IN} = 0V, V_{CC} = 5.5V
Clock input hysteresis		4		300		mVp-p	
Clock rate		4			0.5	MHz	
Data setup time	t_2	3	0.5			μs	See Fig. 3
Enable setup time	t_1	2	0.5			μs	See Fig. 3
Clock-to-enable time	t_4	2,3	0.5			μs	See Fig. 3
Enable hold time	t_5	2	1.0			μs	See Fig. 3
Data hold time	t_3	3	0.5			μs	See Fig. 3
Charge pump output current		10		±150		μA	V pin 10 = 2.0V, V_{CC} = 5.0V
Charge pump output leakage current		10			±5	nA	V pin 10 = 2.0V
Charge pump drive output current		9	1			mA	V pin 9 = 0.7V
Charge pump amplifier gain				6400			Pin 9 current 100μA, V_{CC} = 5.0V
Oscillator temperature stability				0.1		ppm/°C	Excludes crystal effects
Oscillator stability with supply voltage				8		ppm/V	Excludes crystal effects

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Output ports							
Sink current		11-14	0.8		1.5	mA	V_{OUT} = 12.0V, V_{CC} = 5.0V
Port leakage current		11-14			10	μA	V_{OUT} = 13.2V, V_{CC} = 4.5V
Output sink current		19, 20			10	mA	V_{OUT} = 0.7V, V_{CC} = 5.5V
Output leakage current		19, 20			10	μA	V_{OUT} = 5.5V, V_{CC} = 5.5V

ABSOLUTE MAXIMUM RATINGS

(All voltages are referred to pins 16 and 8 at 0V)

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Supply voltage	18	-0.3	7	V	
RF input voltage	15, 17		2.5	Vp-p	
Port voltage	11-14	V_{CC}-0.3 V_{CC}-0.3	16 V_{CC} + 6	V V	Port in off state Port in on state
RF input DC offset	15, 17	-0.3	V_{CC} + 0.3	V	
Charge pump DC offset	10	-0.3	V_{CC} + 0.3	V	
Drive DC offset	9	-0.3	V_{CC} + 0.3	V	
Crystal oscillator DC offset	6, 7	-0.3	V_{CC} + 0.3	V	
Data bus input voltage	1-5	-0.3	V_{CC} + 0.3	V	With V_{CC} applied
Storage temperature		-55	+ 125	°C	
Junction temperature			+ 150	°C	
DP20 thermal resistance, chip-to-ambient DP20 thermal resistance, chip-to-case			78 24	°C/W °C/W	
MP20 thermal resistance, chip-to-ambient MP20 thermal resistance, chip-to-case			93 34	°C/W °C/W	
Power consumption at 5.5V			210	mW	All ports off

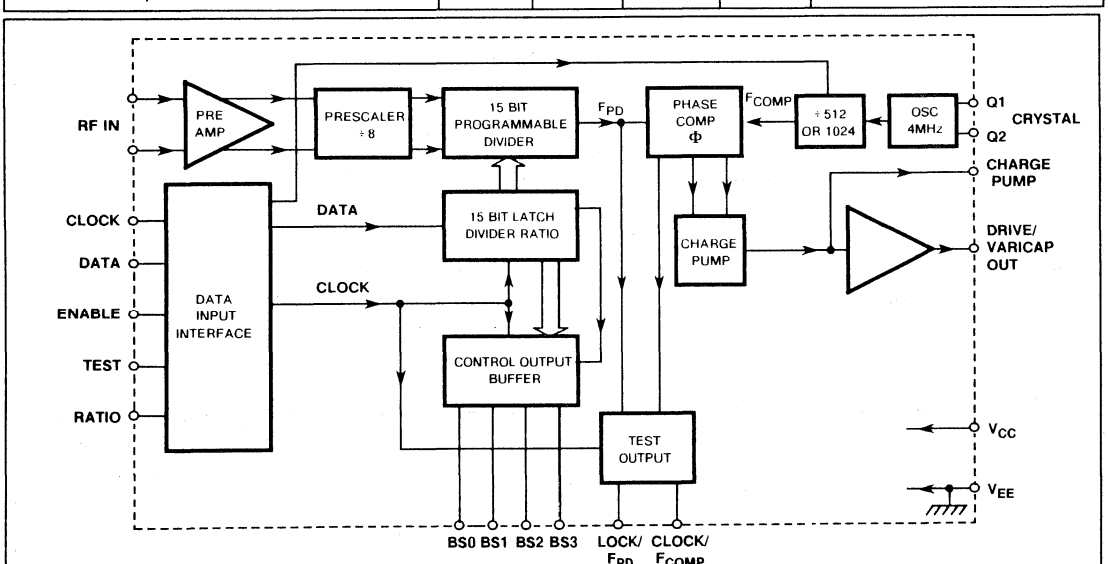


Fig.2 Block diagram os SP5020

FUNCTIONAL DESCRIPTION

The SP5020 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard data, clock, enable, three wire data bus. The data load normally consists of a single word, which contains the frequency and port information, and is only transferred to the internal data shift register during an enable high period, the clock input being disabled during enable low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable, so giving improved fine tune facility for digital AFC etc.

The data sequence and timing follows the format as displayed in Fig. 3.

The frequency is set by loading the programmable divider with the required 15 bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator where it is compared in phase and frequency domain to the internally generated comparison frequency, F_{COMP}.

The F_{COMP} is obtained by dividing the output of an on-chip crystal controlled frequency. The crystal frequency used is generally 4MHz, which gives an F_{COMP} of 3.90625/7.8125kHz and when multiplied back up to the synthesised LO gives a minimum step size of 31.25kHz/62.5kHz respectively depending on ratio selected.

The divide by 8 prescaler is preceeded by an RF preamplifier to achieve excellent sensitivity and overload performance over the full range of operation.

The prescaler then drives the 15-bit programmable multi modulus divider which, when the loop is locked produces an output which is frequency and phase matched to the output of the reference divider. The RF preamplifier input sensitivity and impedance are shown in Figs. 5 and 7, respectively.

The SP5020 contains 4 band switching outputs, ports BS0-BS3 which are capable of sinking 1mA. These outputs are set by the remaining four bits within the data word.

The device is switched between divide by 1024 and divide by 512 by applying a voltage to the ratio select pin pin 5. A"high" voltage puts the device into divide by 512 mode (62.5kHz step) and a 'low' or open circuit selects 1024 (31.25kHz).

DEVICE COMPATIBILITY

The SP5020 is pin compatible with the Toshiba TD6381 and Mitshubushi M54965 and M54939 with no modifications to their present application circuits. If pin 5 (ratio select) is left open circuit or taken to ground (divide by 1024 mode), the SP5020 is compatible with Toshiba TD6358 and TD6382.

TEST MODE

Taking pin 1 high disables the charge pump and makes F_{COMP} and F_{PD} available at pins 19 and 20 respectively.

In normal mode of operation pipelined data CLOCK and 'in-lock' flag, LOCK are available from these pins. The 'in-lock' detector is normally high impedance and pulses current depending on phase difference between F_{COMP} and F_{PD}.

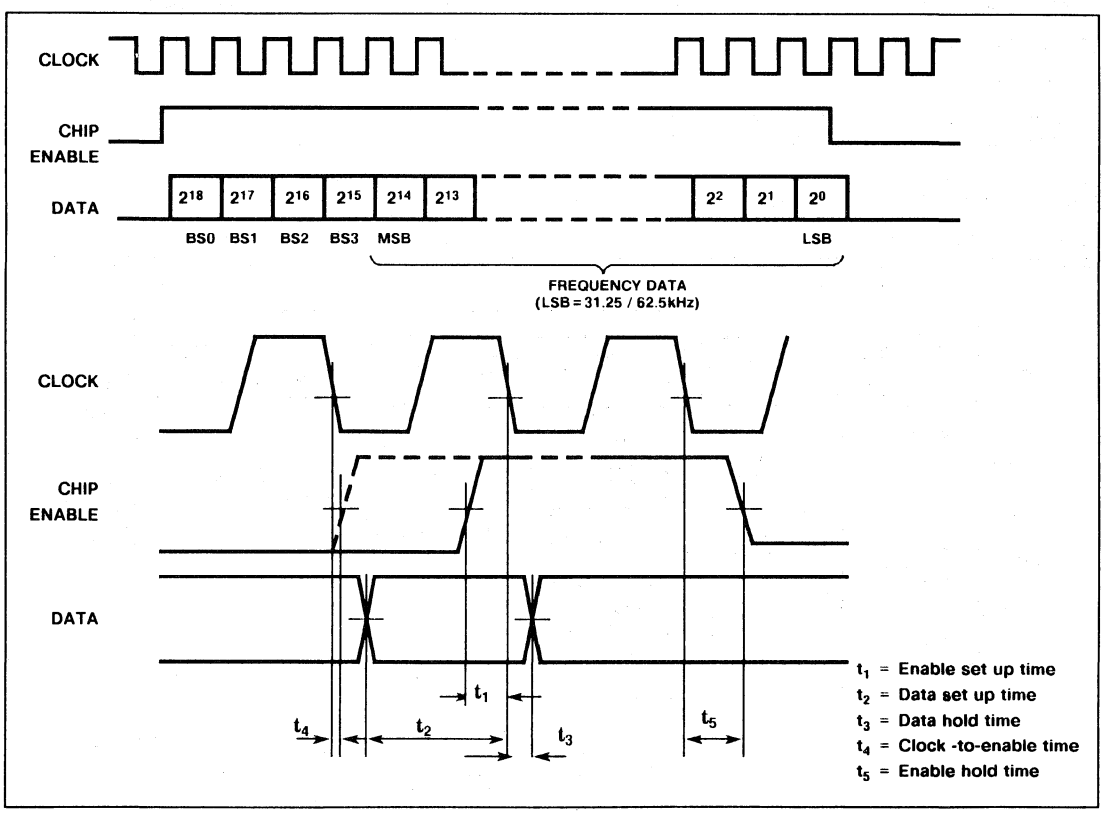


Fig.3. Data format and timing

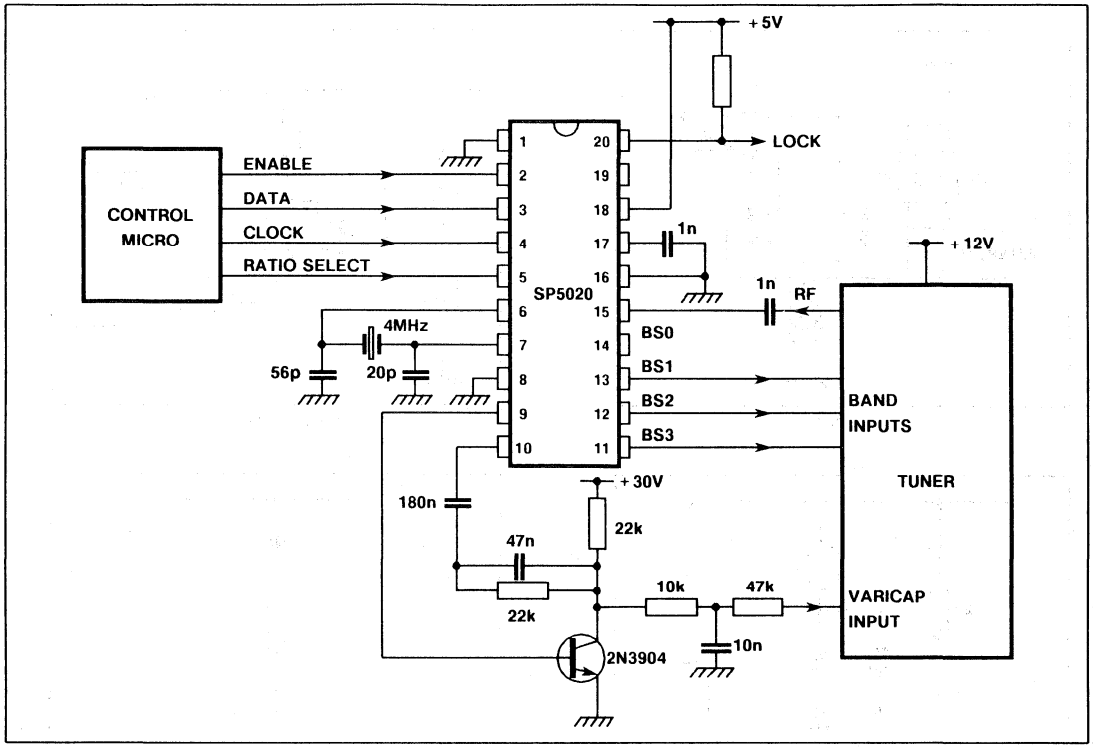


Fig. 4 Typical application

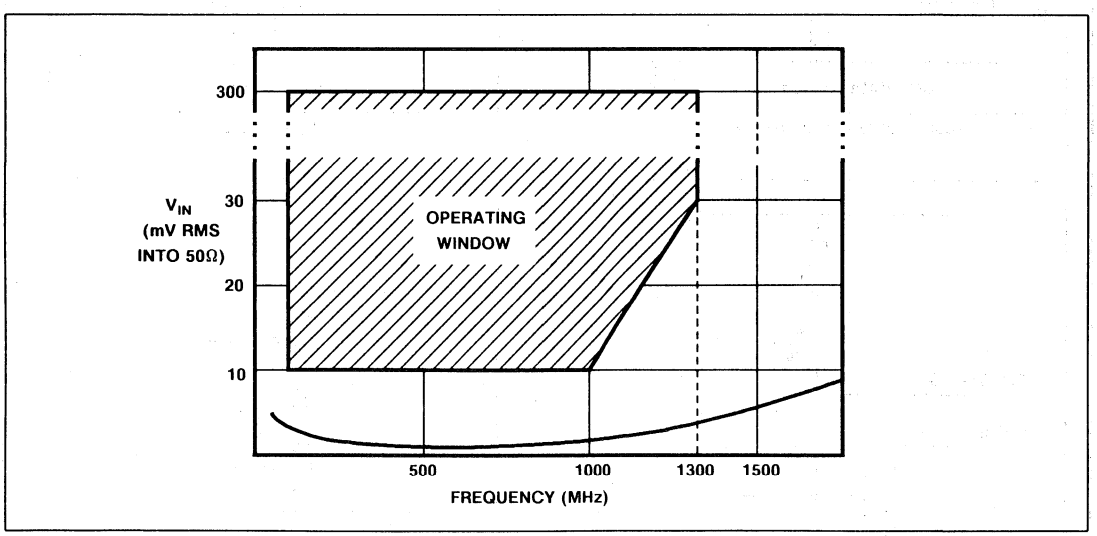
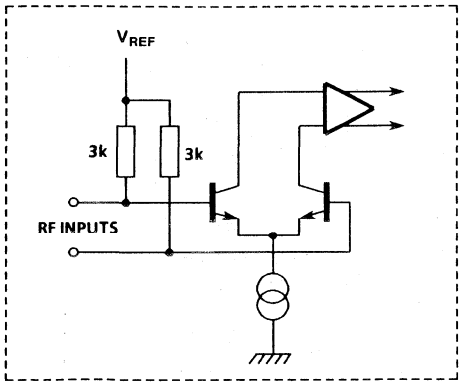
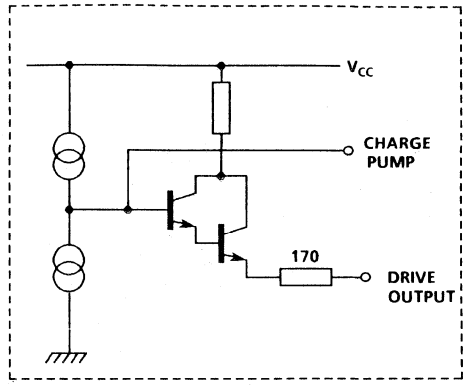


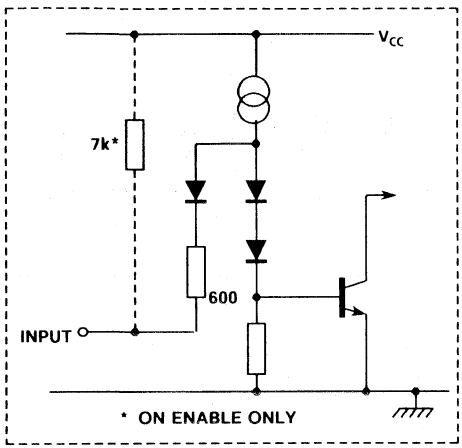
Fig.5. Typical input sensitivity



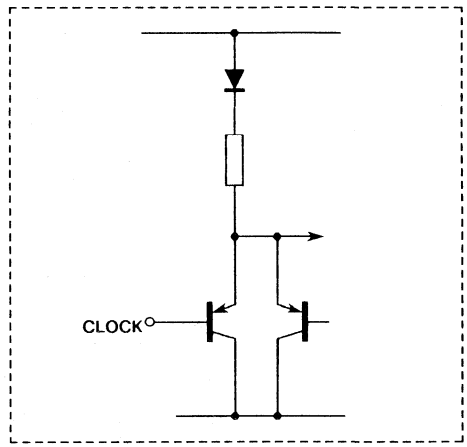
RF input



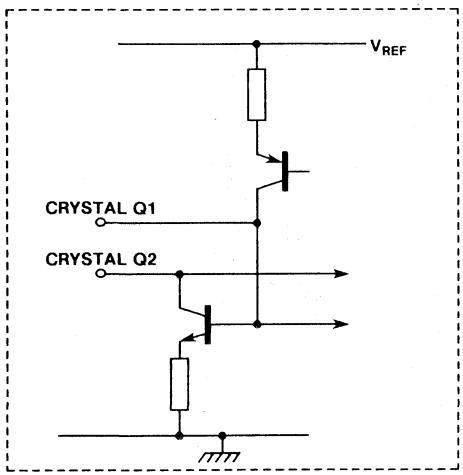
Loop amplifier



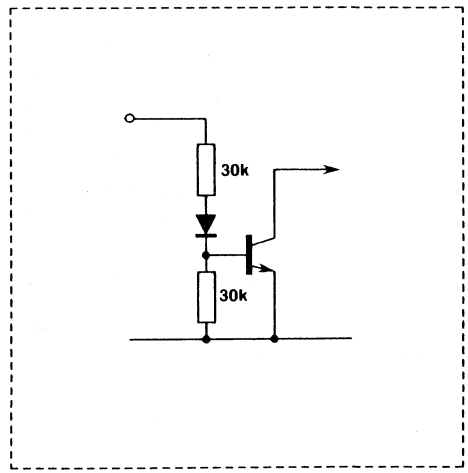
Test, enable and data inputs



Clock inputs



Oscillator



Reference ratio select

Fig.6a SP5020 input/output interface circuits

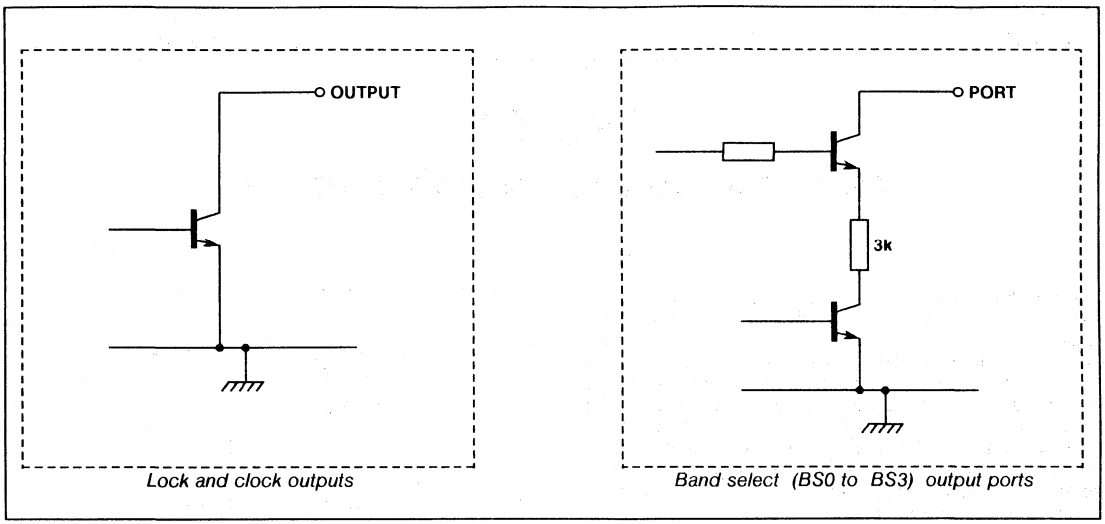


Fig.6b SP5020 input/output interface circuits (continued)

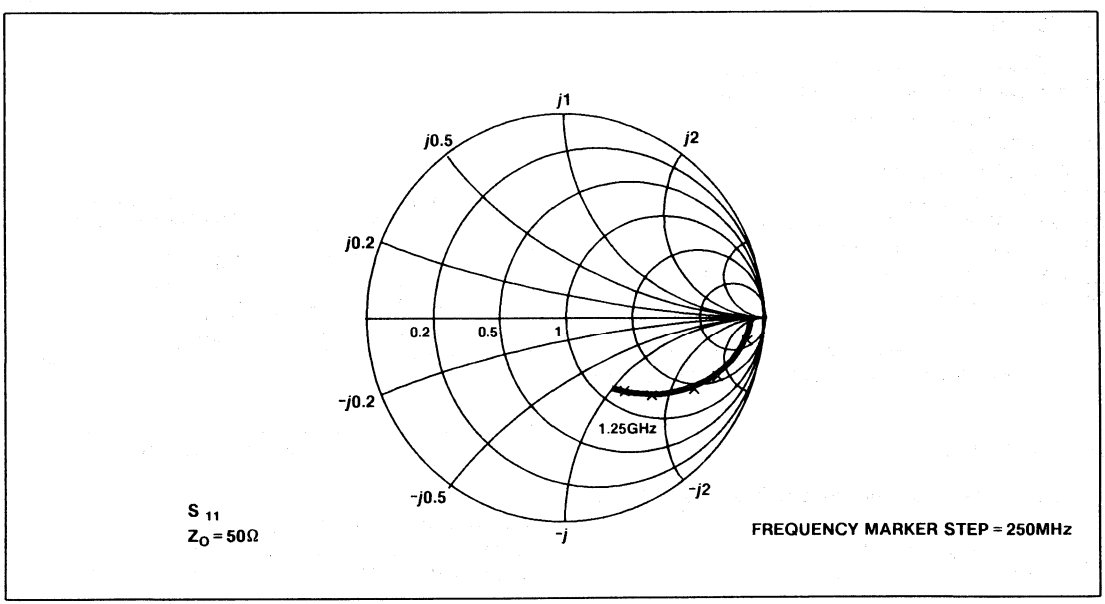


Fig. 7 Typical input impedance

SP5021

1GHz 3-WIRE BUS CONTROLLED SYNTHESISER

The SP5021, when used with a TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide-by-8 prescaler with its own preamplifier and a 14-bit programmable divider controlled by a serially-loaded data register. Four band selection lines, BS0-BS3, are included. The frequency/phase comparator is fed with a 7.8125kHz reference, derived from a 4MHz crystal controlled on - chip oscillator. The comparator has a charge pump output with an amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

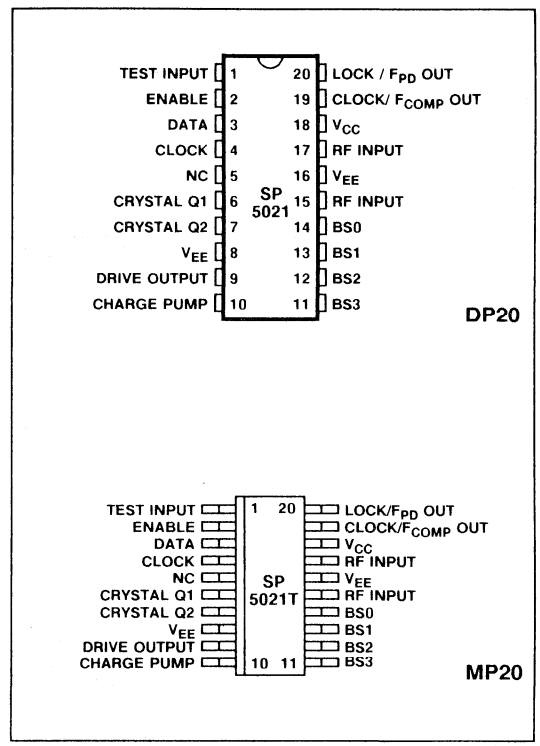


Fig.1 Pin connections - top view

FEATURES

- Complete 1GHz Single Chip System
- 7.8125kHz Reference/62.5kHz step size
- Low Power Consumption (5V 30mA)
- Low Radiation
- Phase Lock Indication
- Charge Pump Disable
- Single Port 18-Bit Serial Data Entry
- 4 Band Select Outputs
- Compatible with Toshiba TD6359, TD6380,*
- Full ESD Protection †

* See notes on device compatibility, page 1-69

† Normal ESD handling procedures should be observed

APPLICATIONS

- Satellite TV when combined with SP4902 2.5GHz Prescaler
- Cable tuning Systems
- VCRs

ORDERING INFORMATION

SP5021 DP - (20 lead plastic package)
SP5021T MP - (20 lead miniature plastic package)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = −10°C to +80°C, V_{CC} = +4.5V to 5.5V, Frequency Standard = 4MHz

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	18		30	38	mA	V_{CC} = 5V
Prescaler Input Voltage		15, 17	10		300	mV_{RMS}	50MHz to 1GHz sinewave
Prescaler Input Impedance Input Capacitance		15, 17		50 2		Ω pF	
High Level Input Voltage		1,2,3,4	2.7		V_{CC}	V	
Low Level Input Voltage		1,2,3,4			0.7	V	
High Level Input Current		1,3,4			1	μA	V_{IN} = 5.5V, V_{CC} = 5.5V
Low Level Input Current		1,3			-200	μA	V_{IN} = 0V, V_{CC} = 5.5V
Low Level Input Current		2			-1.25	mA	V_{IN} = 0V, V_{CC} = 5.5V
Low Level Input Current		4			-5	μA	V_{IN} = 0V, V_{CC} = 5.5V
HighLevel Input Current		2			± 10	μA	V_{IN} = 5.5V, V_{CC} = 5.5V
Clock Input Hysteresis		4		300		mVp-p	
Clock Rate		4			0. 5	MHz	
Data Setup Time	t_2	3	300			ns	See Fig 3
Enable SetupTime	t_1	2	300			ns	See Fig 3
Clock to Enable Time	t_4	2, 3	300			ns	See Fig 3
Enable Hold Time	t_5	2	600			ns	See Fig 3
Data Hold Time	t_3	3	600			ns	See Fig 3
Charge Pump Output Current		10		± 150		μA	V pin 10 = 2.0V
Charge Pump Output Leakage Current		10			± 5	nA	V pin 10 = 2.0V
Charge Pump Drive Output Current		9	1			mA	V pin 9 = 0.7V
Charge Pump Amplifier Gain				6400			Pin 9 current 100μA
Oscillator Temperature Stability				0.1		ppm/°C	Excludes crystal effects
Oscillator Stability with Supply Voltage				8		ppm/V	
Sink Current		11 to 14	0.8		1.5	mA	V_{OUT} = 12V, V_{CC} = 5.0V
Port Leakage Current		11 to 14			10	μA	V_{OUT} = 13.2V, V_{CC} = 4.5V
Output sink current		19, 20			10	mA	V_{OUT} = 0.7V, V_{CC} = 5.5V
Output leakage Current		19, 20			10	μA	V_{OUT} = 5.5V, V_{CC} = 5.5V

ABSOLUTE MAXIMUM RATINGS

(All voltages are referred to pins 16 and 8 at 0V)

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Supply voltage	18	-0.3	7	V	
RF input voltage	15, 17		2.5	Vp-p	
Port voltage	11-14	V_{CC}-0.3 V_{CC}-0.3	16 V_{CC} + 6	V V	Port in off state Port in on state
RF input DC offset	15, 17	-0.3	V_{CC} + 0.3	V	
Charge pump DC offset	10	-0.3	V_{CC} + 0.3	V	
Drive DC offset	9	-0.3	V_{CC} + 0.3	V	
Crystal oscillator DC offset	6, 7	-0.3	V_{CC} + 0.3	V	
Data bus input voltage	1-4	-0.3	V_{CC} + 0.3	V	With V_{CC} applied
Storage temperature		-55	+ 125	°C	
Junction temperature			+ 150	°C	
DP20 thermal resistance, chip-to-ambient DP20 thermal resistance, chip-to-case			78 24	°C/W °C/W	
MP20 thermal resistance, chip-to-ambient MP20 thermal resistance, chip-to-case			93 34	°C/W °C/W	
Power consumption at 5.5V			210	mW	All ports off

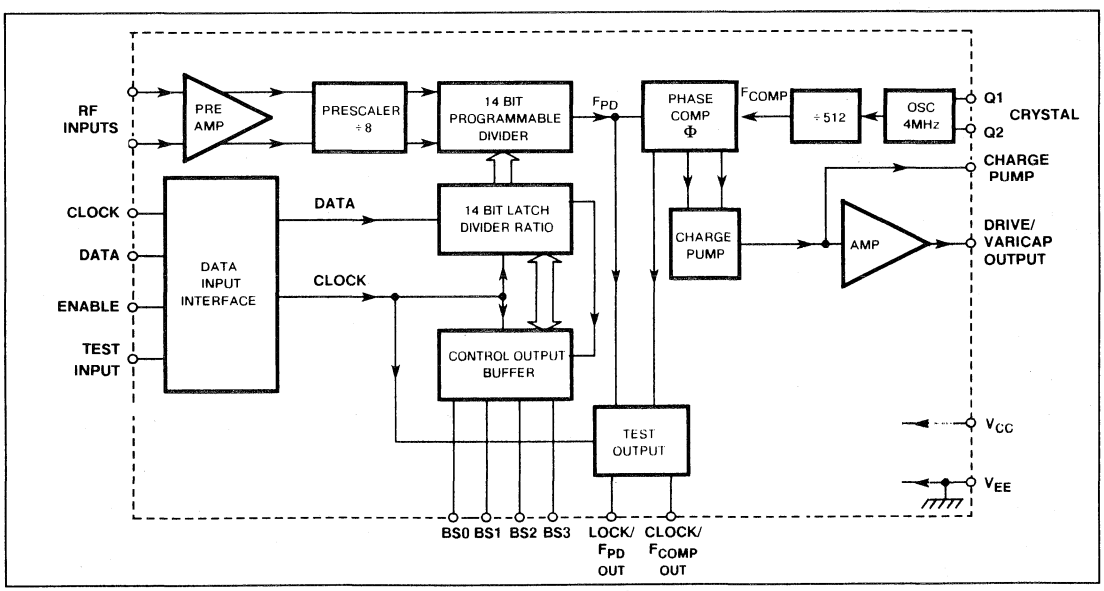


Fig.2. Block diagram of SP5021

FUNCTIONAL DESCRIPTION

The SP5021 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard data, clock and enable three-wire data bus. The data load normally consists of a single word, which contains the frequency and band information, and is only transferred to the internal data shift register during an enable high period. The clock input is disabled during enable low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable, so giving improved fine tune facility for digital AFC etc.

The data sequence and timing follows the format as displayed in Figure 3.

The frequency is set by loading the programmable divider with the required 14 bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator where it is compared in phase and frequency domain to the internally generated comparison frequency, F_{COMP}.

The F_{COMP} is obtained by dividing the output of an on-chip crystal controlled frequency. The crystal frequency used is generally 4MHz, which gives an F_{COMP} of 7.8125kHz and when multiplied back up to the synthesised LO gives a minimum step size of 62.5kHz.

The divide by 8 prescaler is preceded by an RF preamplifier to achieve excellent sensitivity and overload performance over the full range of operation. The prescaler then drives the 14 bit programmable multi modulus divider which, when the loop is locked produces an output which is frequency and phase matched to the output of the reference divider. Input sensitivity and impedance are shown in Figs. 7 and 7, respectively

The SP5021 contains 4 band switching outputs, BS0-BS3 which are capable of sinking up to 1.5mA. These outputs are set by the remaining four bits within the data word.

DEVICE COMPATIBILITY

The SP5021 is compatible with the Toshiba TD6359 and TD6380 with no modifications to their application circuits.

TEST MODE

Taking pin 1 high disables the charge pump and makes F_{COMP} and F_{PD} available at pins 19 and 20 respectively.

In normal mode of operation pipelined data CLOCK and phase lock flag LOCK are available from these pins. The 'inlock' detector pulses current depending on phase difference between F_{COMP} and F_{PD}. Phase lock is indicated by a logic low condition.

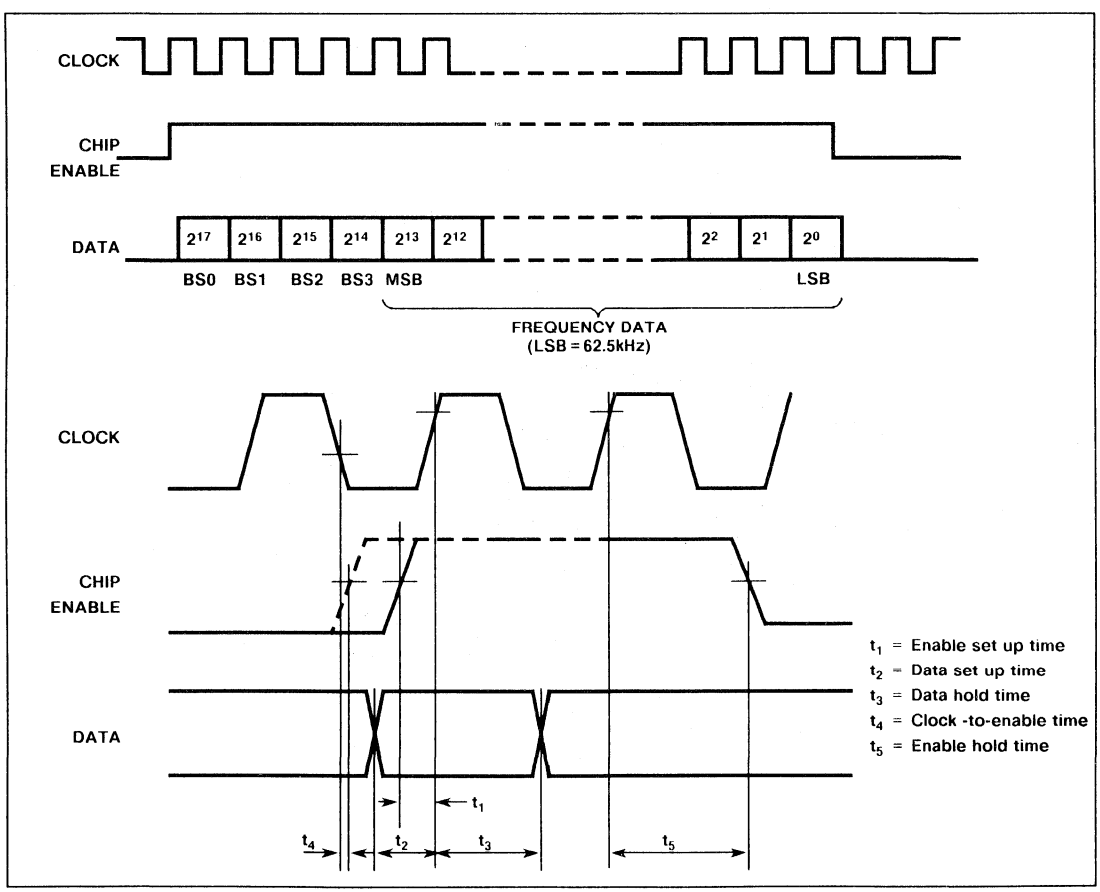


Fig.3 Data format and timing

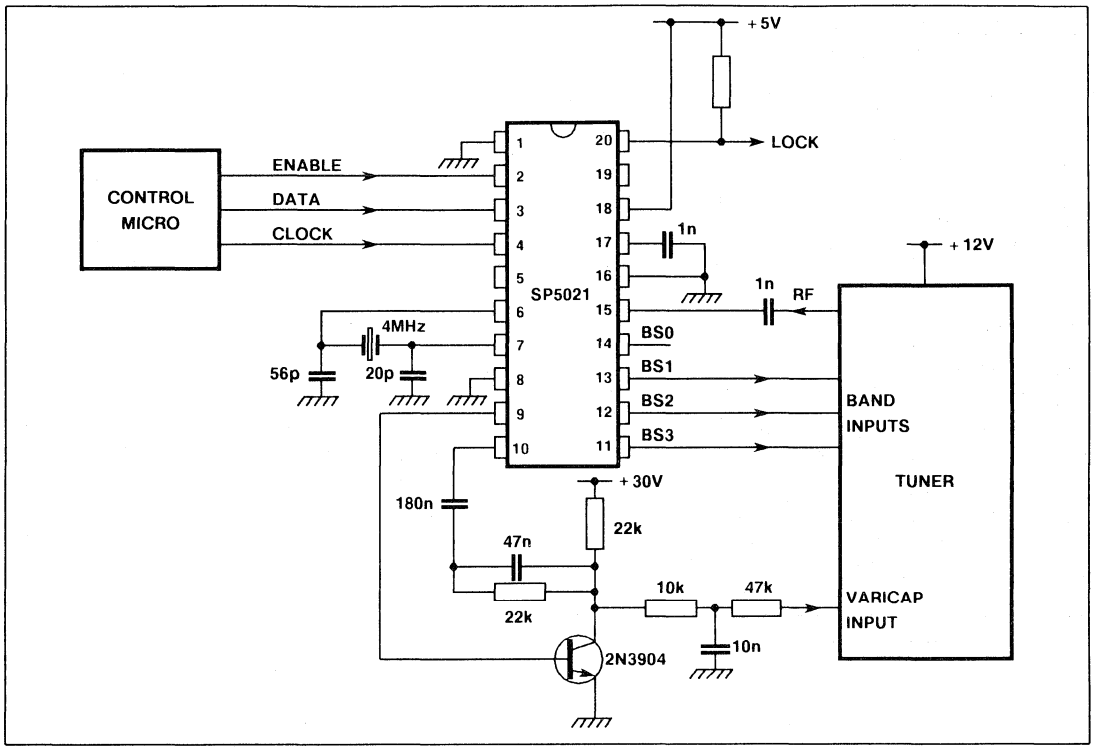


Fig. 4 Typical application

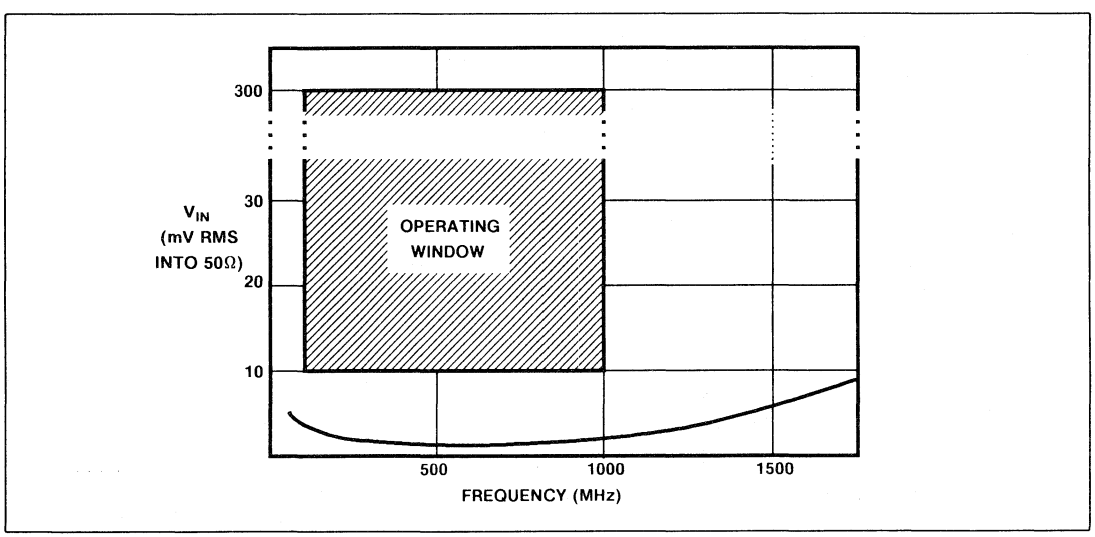
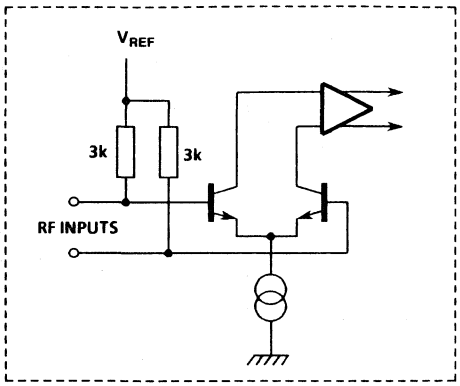
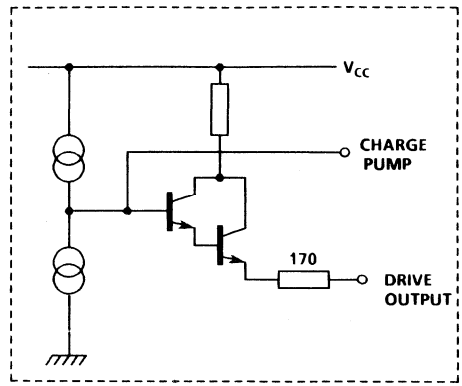


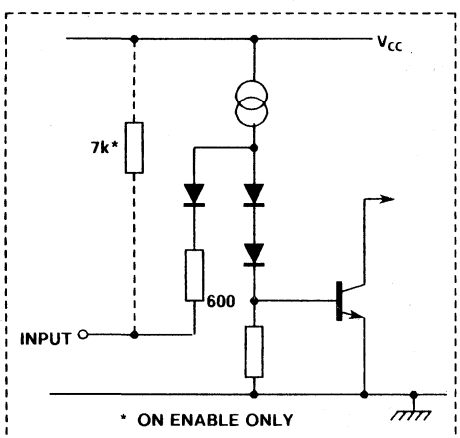
Fig.5 Typical Input sensitivity



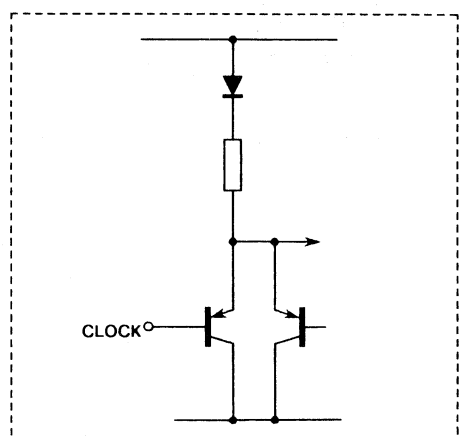
RF input



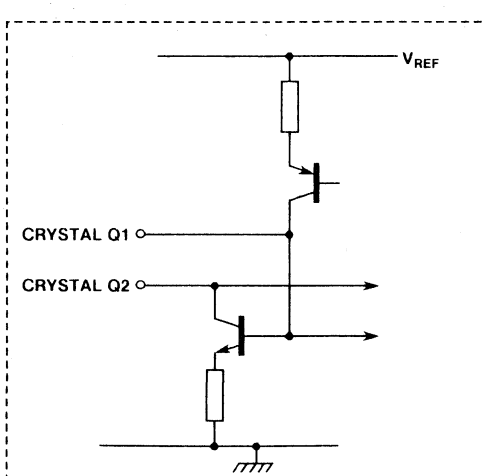
Loop amplifier



Test input, enable and data input



Clock input



Oscillator

Fig.6a SP5021 input/output interface circuits

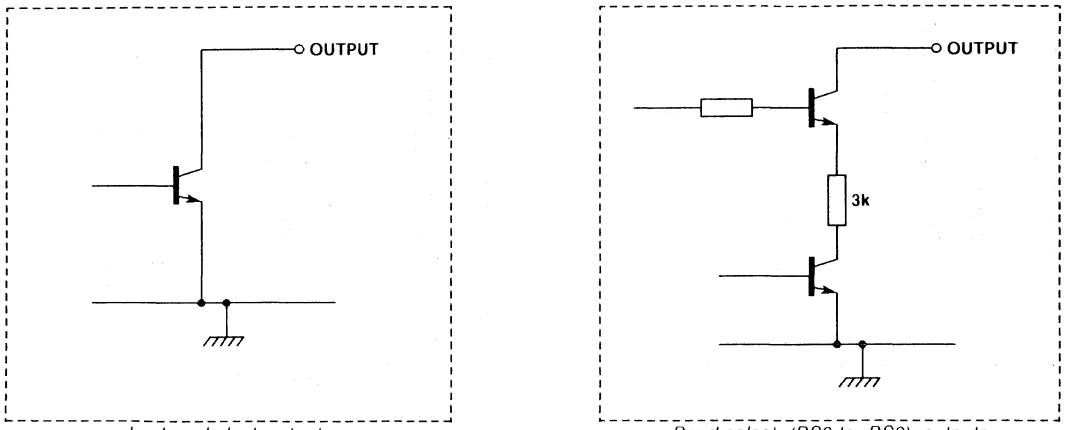


Fig.6b SP5021 input/output interface circuits (continued)

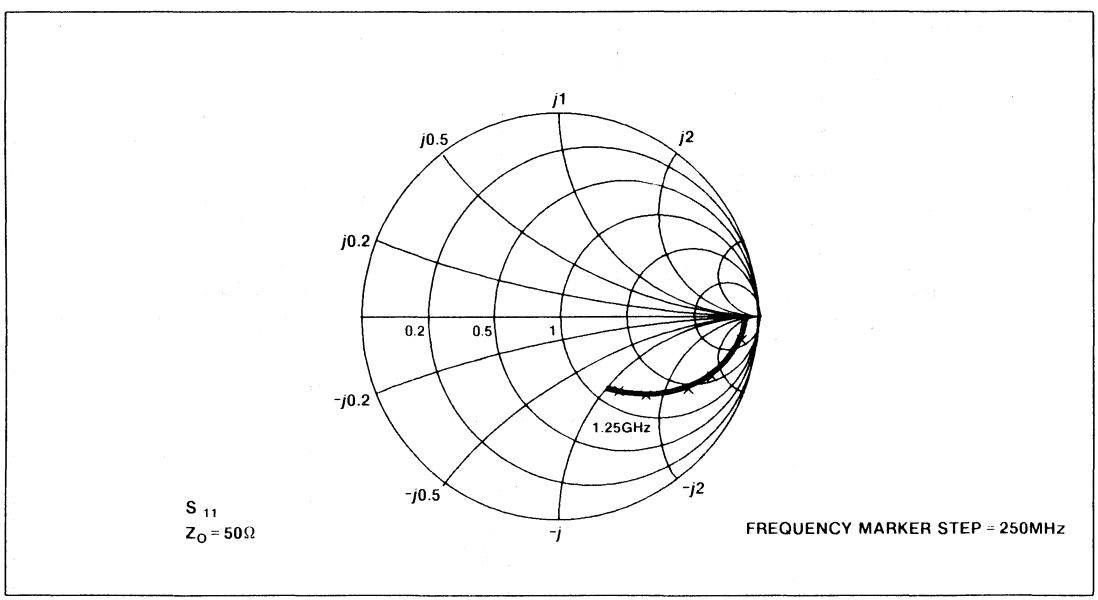


Fig. 7 Typical input impedance

SP5024

1.3GHz 3-WIRE BUS CONTROLLED SYNTHESISER

The SP5024 is a programming variant of the SP5510, allowing the design of one tuner with either I²C bus or 3-wire bus format depending on which device is inserted. The SP5024, when used with a TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide-by-8 prescaler with its own preamplifier and a 15-bit programmable divider controlled by a serially-loaded data register. Four open-collector outputs, each independently programmable, are included. The device has two modes of operation, selected by the 'mode select' input. In mode 1, the comparison frequency is 7.8125kHz and the programmable divider MSB is bypassed; mode 2 comparison frequency is 6.25 kHz. The comparison frequencies are both obtained from a 4MHz crystal controlled on-chip oscillator. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

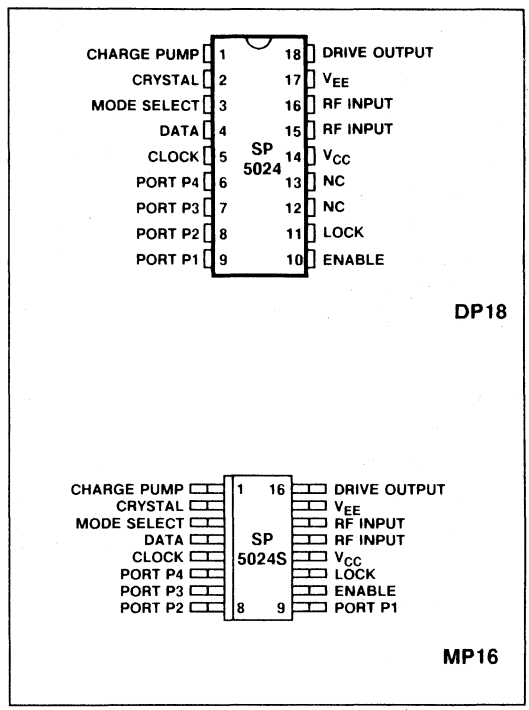


Fig.1 Pin connections - top view

FEATURES

- Complete 1.3GHz Single Chip System
- Dual Standard 50kHz or 62.5kHz Step Size
- Low Power Consumption (5V 40mA)
- Programming Compatible with Toshiba TD6380 and TD6381 *
- Pin Compatible with SP5510 *
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- Charge Pump Disable
- Single Port 18/19 Bit Serial Data Entry
- Four Controllable Outputs
- Full ESD Protection †

* See notes on pin compatibility, page 1-76.
† Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV when combined with SP4902 2.5GHz Prescaler
- Cable tuning Systems
- VCRs

ORDERING INFORMATION

SP5024 DP - (18 lead Plastic Package)
SP5024S MP - (16 lead Miniature Plastic Package)

ELECTRICAL CHARACTERISTICS

T_{amb} = -20°C to +80°C, V_{CC} = +4.5V to +5.5V Frequency Standard = 4MHz. Pin numbers refer to SP5024 (DP package) These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	14		40	55	mA	V_{CC} = 5V
Prescaler input voltage		15, 16	12.5		300	mV_{RMS}	50MHz to 1GHz sinewave
Prescaler input voltage		15, 16	30		300	mV_{RMS}	1.3GHz, see Fig. 5
Prescaler input impedance Input capacitance		15, 16		50 2		Ω pF	
High level input voltage		4,5,10	3		V_{CC}	V	
High level input voltage		3	4		V_{CC}	V	
Low level input voltage		3,4,5,10	0		0.6	V	
High level input current		4,5,10			1	μA	V_{IN} = 5.5V, V_{CC} = 5.5V
Low level input current		5			5	μA	V_{IN} = 0V, V_{CC} = 5.5V
Low level input current		4,10			-250	μA	V_{IN} = 0V, V_{CC} = 5.5V
High level input current		3			150	μA	V_{IN} = 5.5V, V_{CC} = 5.5V
Low level input current		3			-1	μA	V_{IN} = 0V, V_{CC} = 5.5V
Clock input hysteresis		5		0.4		V	
Clock rate		5			0. 5	MHz	
Data setup time	t_2	4	300			ns	See Fig. 3
Data hold time	t_3	4	600			ns	See Fig. 3
Enable setup time	t_1	10	300			ns	See Fig. 3
Enable hold time	t_5	10	600			ns	See Fig. 3
Clock-to-enable time	t_4	10	300			ns	See Fig. 3
Charge pump output current		1		±150		μA	V pin 1 = 2.0V
Charge pump output leakage current		1			±5	nA	V pin 1 = 2.0V
Drift due to leakage					5	mV/s	At collector of external varicap drive transistor
Charge pump drive output current		18	1			mA	V pin 18 = 0.7V
Charge pump amplifier gain				6400			Pin 18 current = 100μA
Oscillator temperature stability					2	ppm/°C	
Oscillator Stability with Supply Voltage					2	ppm/V	
Recommended crystal series resistance			10		200	Ω	
Crystal oscillator drive level		2		40		mV p-p	
Crystal oscillator source impedance		2		-400		Ω	Nominal spread ±15%

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Ports and Lock Output							
Sink current		6 - 9,11	10			mA	V_{OUT} = 0.7V
Port leakage current		6 - 9			10	µA	V_{OUT} = 13.2V
Varactor drive amp disable		10	-350			µA	V_{IN} < 0V
Charge pump disable		4	-350			µA	V_{IN} < 0V

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} = 0V

Parameter	Pin SP5024	Pin SP5024S	Value		Units	Conditions
			Min	Max		
Supply voltage	14	12	-0.3	7	V	
Prescaler inputs	15, 16	13, 14		2.5	Vp-p	
Output ports	6-9	6-9	-0.3 -0.3	14 6	V V	Port in off state Port in on state
Prescaler DC offset	15, 16	13, 14	-0.3	V_{CC} + 0.3	V	
Loop amplifier DC offset	1, 18	1, 16	-0.3	V_{CC} + 0.3	V	
Crystal oscillator DC offset	2	2	-0.3	V_{CC} + 0.3	V	
Data bus inputs	4, 5, 10	4, 5, 10	-0.7	V_{CC} + 0.3	V	With V_{CC} applied
Storage temperature			-55	+ 125	°C	
Junction temperature				+ 150	°C	
DP18 thermal resistance, chip-to-ambient DP18 thermal resistance, chip-to-case				78 24	°C/W °C/W	
MP16 thermal resistance, chip-to-ambient MP16 thermal resistance, chip-to-case				111 41	°C/W °C/W	
Power consumption at 5.5V				275	mW	All ports off

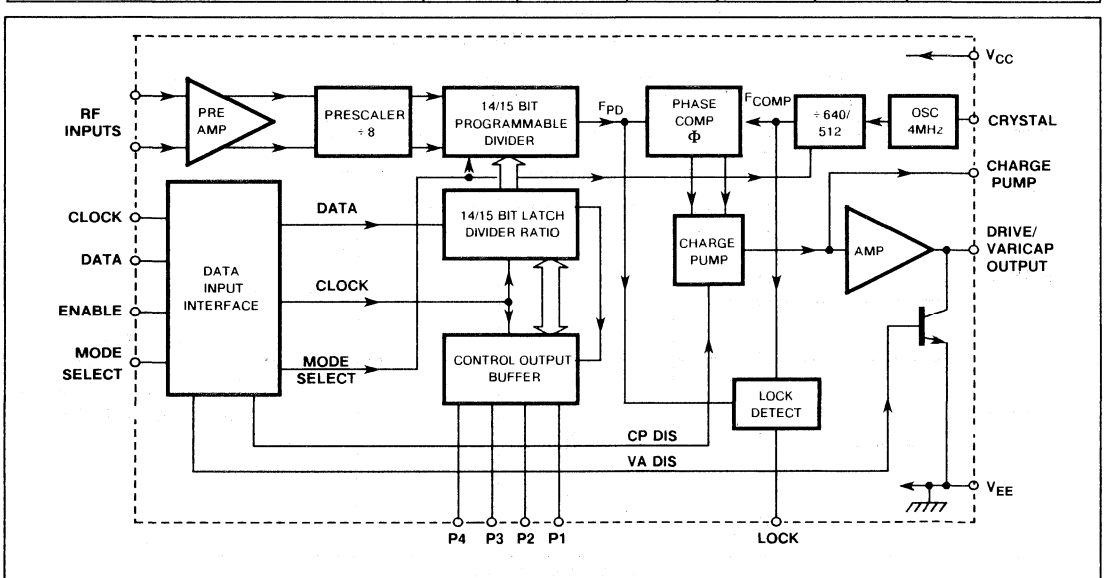


Fig.2. Block diagram of SP5024

FUNCTIONAL DESCRIPTION

The SP5024 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard data, clock, enable, three wire data bus. The data load normally consists of a single word, which contains the frequency and port information, and is only transferred to the internal data shift register during an enable high period. The clock input is disabled during enable low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable, so giving improved fine tune facility for digital AFC etc.

The data sequence and timing follows the format as displayed in Figure 3.

The frequency is set by loading the programmable divider with the required 14/15 bit divisor word. The output of this divider, F_{pd}, is fed to the phase comparator where it is compared in phase and frequency domain to the internally generated comparison frequency, F_{COMP}.

The F_{COMP} is obtained by dividing the output of an on-chip crystal controlled osciillator. The crystal frequency used is generally 4MHz, which gives an F_{COMP} of 6.25/7.8125kHz and when multiplied back up to the synthesised LO gives a minimum step size of 50kHz/62.5kHz respectively.

The programmable divider is preceded by an input RF preamplifier and high speed, low radiation prescaler. The preamplifier is arranged to be self oscillating so giving excellent input sensitivity. The input sensitivity and impedance are shown in Figs. 5 and 7, respectively.

The SP5024 contains an improved lock detect circuit which generates a flag when the loop has attained lock. 'In lock' is indicated by high impedance state.

The SP5024 contains 4 general purpose open collector outputs, ports P1-P4, which are capable of sinking up to 10mA. These outputs are set by the remaining four bits within the normal data word.

PIN COMPATIBILITY

The SP5024 may be used in SP5510 applications which require 3-wire bus as opposed to I²C bus data format. In SP5510 applications where the reference crystal is grounded to pin 3, a small modification is required to ground the crystal as shown in Fig. 4.

Appropriate connections to the mode select input (pin 3) must also be made.

With pin 3 'HIGH' the SP5024 is programming and step size compatible with the Toshiba TD6380, and with pin 3 'LOW' it is compatible with the TD6381. In both modes a 4MHz crystal is used to derive F_{COMP}, unlike the TD6381 which requires a 3.2MHz crystal.

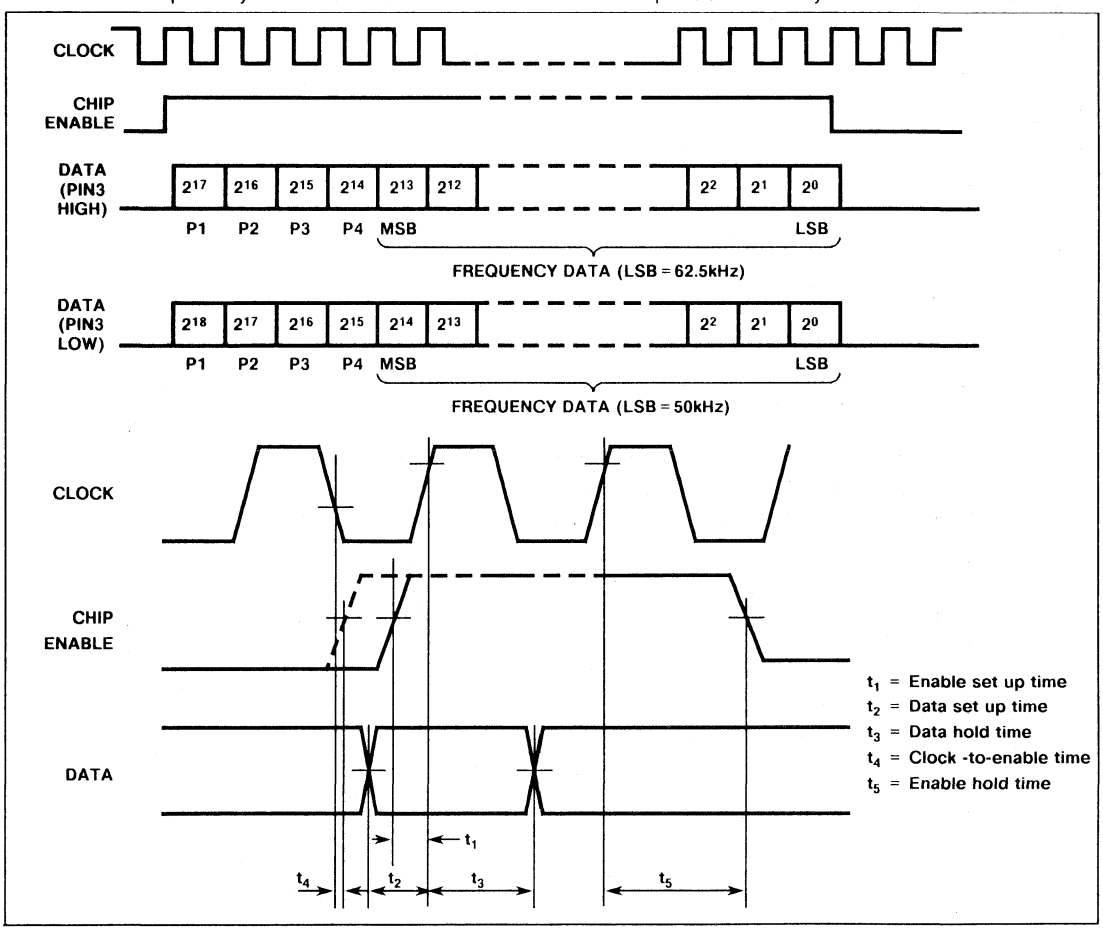


Fig.3 Data format and timing

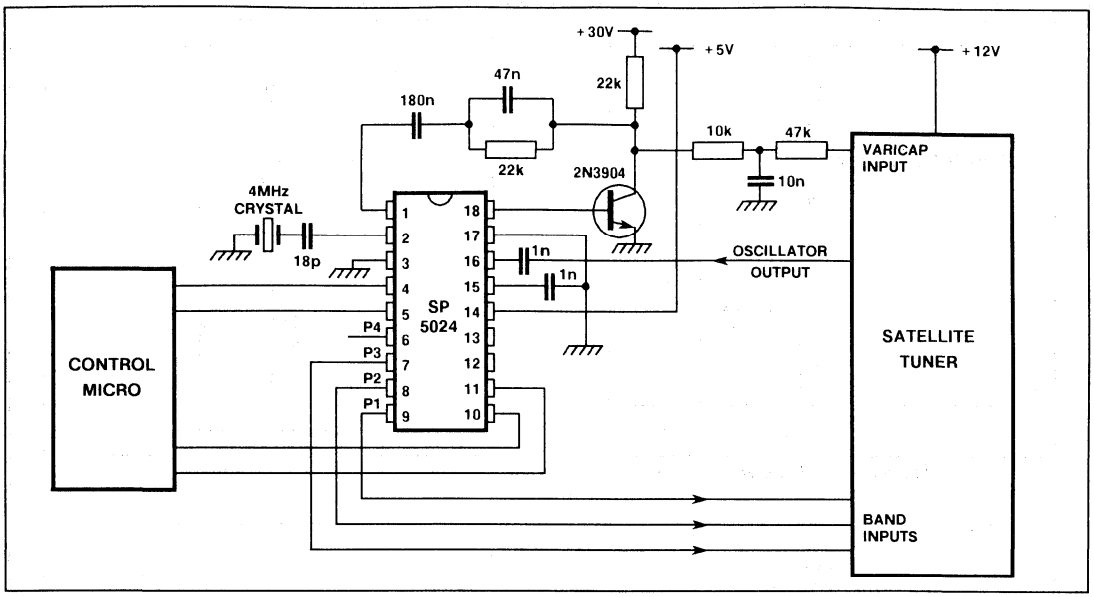


Fig.4 Typical application (F_{STEP} = 50kHz)

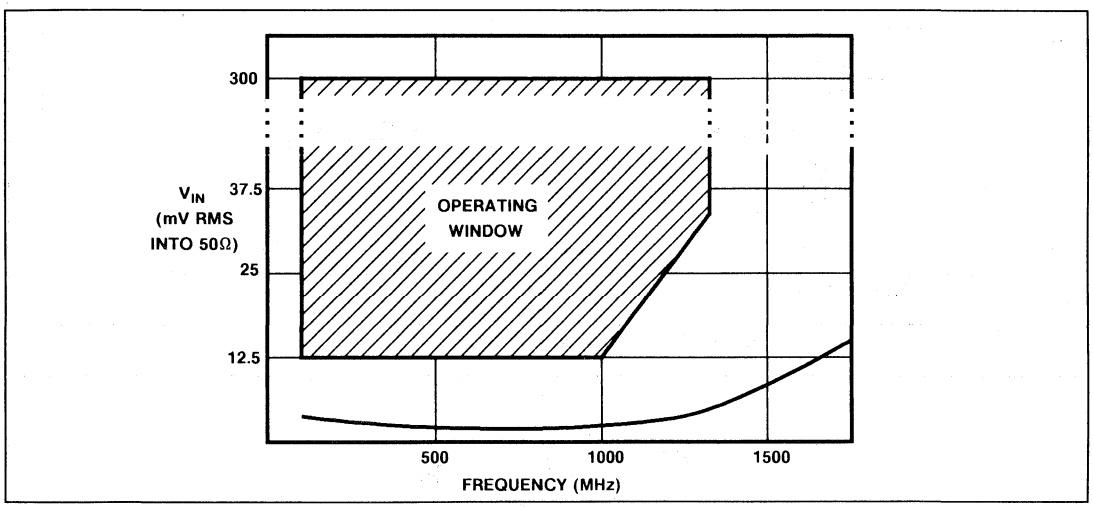


Fig.5 Typical input sensitivity

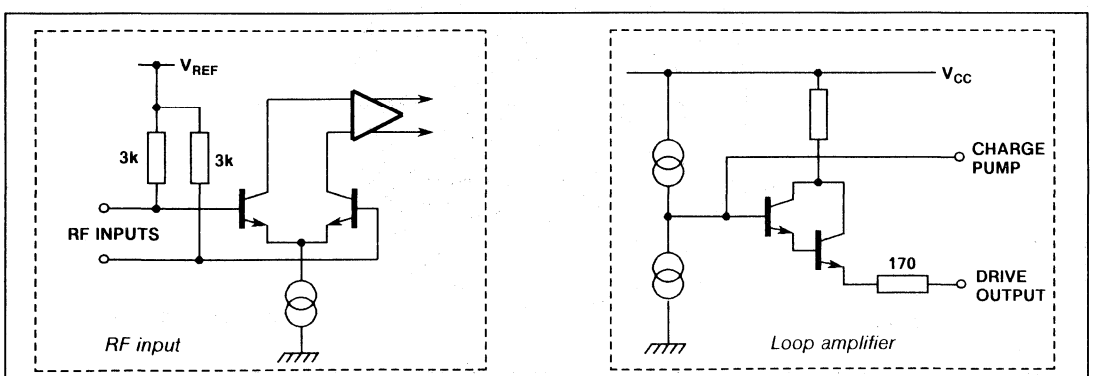


Fig.6a SP5024 input/output interface circuits

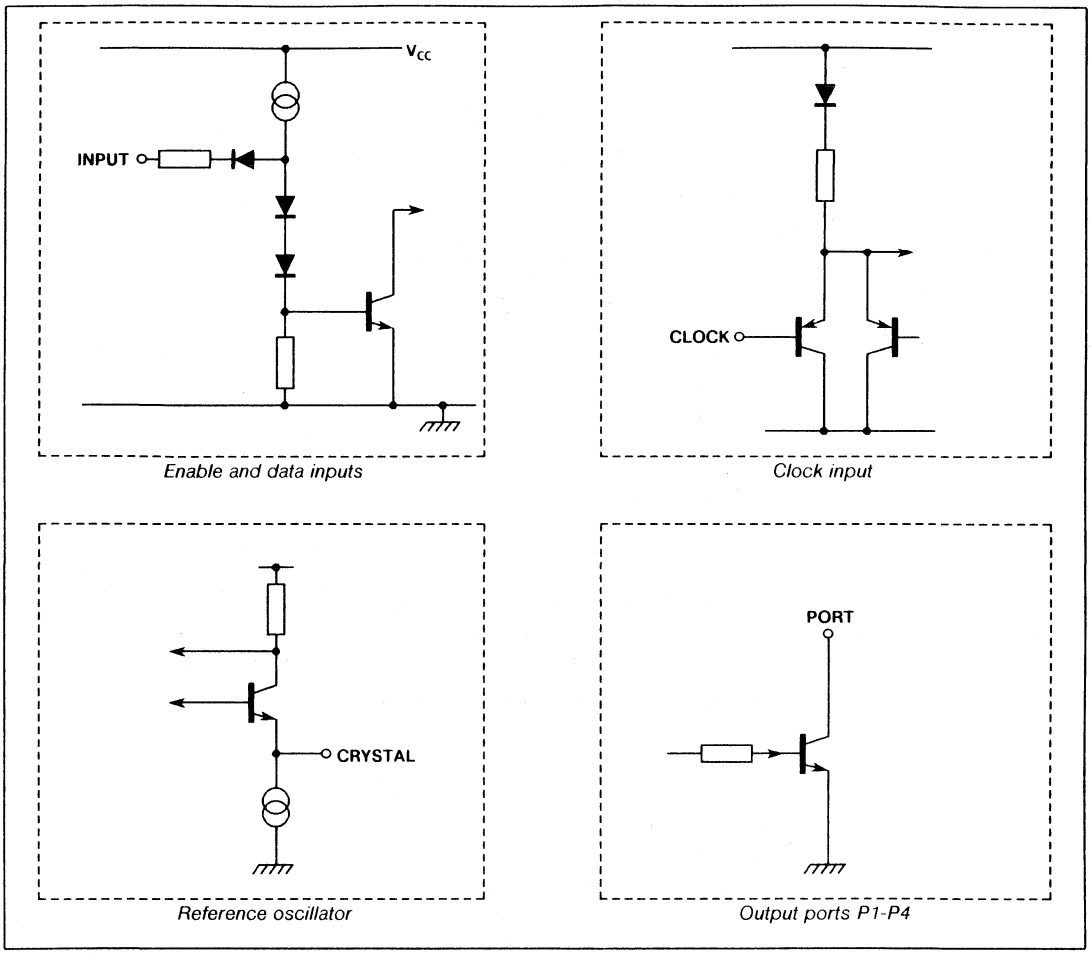


Fig.6b SP5024 input/output interface circuits (continued)

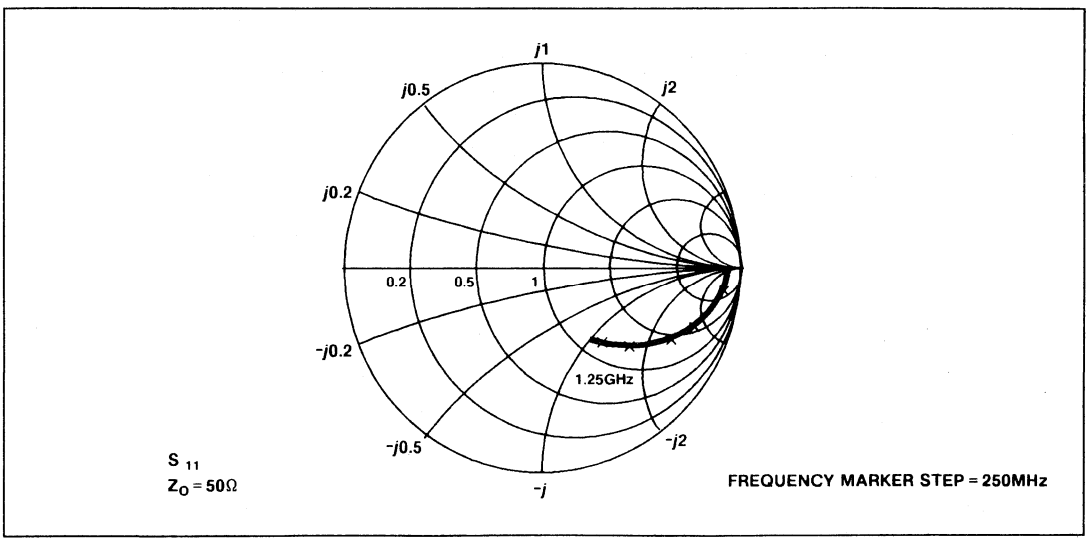


Fig. 7 Typical input impedance

SP5026

1.0GHz 3-WIRE BUS CONTROLLED SYNTHESISER

The SP5026 is a programming variant of the SP5510, allowing the design of one tuner with either I²C bus or 3-wire bus format depending on which device is inserted. The SP5026, when used with a TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide-by-8 prescaler with its own preamplifier and a 15-bit programmable divider controlled by a serially-loaded data register. Four open-collector outputs, each independently programmable, are included. The device has two modes of operation, selected by the 'mode select' input. In mode 1, the comparison frequency is 7.8125kHz and the programmable divider MSB is bypassed; mode 2 comparison frequency is 3.90625kHz. The comparison frequencies are both obtained from a 4MHz crystal controlled on-chip oscillator. The comparator has a charge pump output with an amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

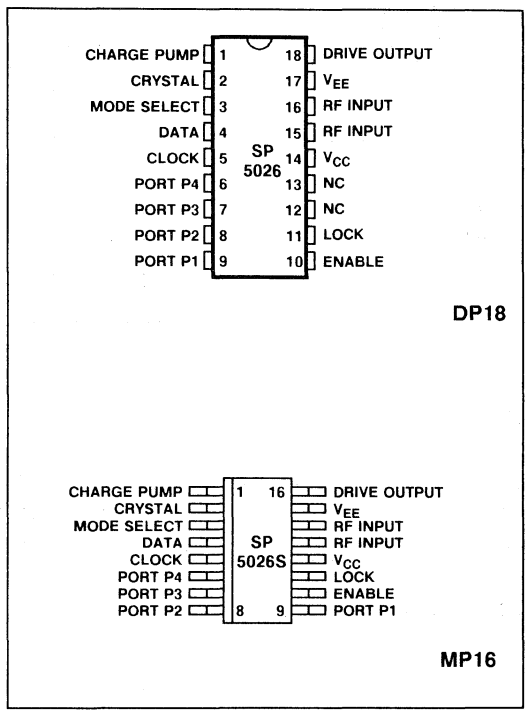


Fig.1 Pin connections - top view

FEATURES

- Complete 1.0GHz Single Chip System
- Dual Standard 62.5kHz or 31.25kHz Step Size
- Low Power Consumption (5V 40mA)
- Function Compatible with Toshiba TD6380 and TD6382 *
- Pin Compatible with SP5510 *
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- Charge Pump Disable
- Single Port 18/19 Bit Serial Data Entry
- Four Controllable Outputs
- Full ESD Protection †

* See notes on PIN compatibility, page 1-82.
† Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV when combined with SP4902 2.5GHz Prescaler
- Cable tuning Systems
- VCRs

ORDERING INFORMATION

SP5026 DP - (18 lead Plastic Package)
SP5026S MP - (16 lead Miniature Plastic Package)

ELECTRICAL CHARACTERISTICS

T_{amb} = -20°C to + 80°C, V_{CC} = + 4.5V to + 5.5V Frequency Standard = 4MHz. Pin numbers refer to SP5026 (DP package) These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	14		40	55	mA	V_{CC} = 5V
Prescaler input voltage		15, 16	12.5		300	mV_{RMS}	50MHz to 1GHz sinewave
Prescaler input impedance		15, 16		50		Ω	
Input capacitance				2		pF	
High level input voltage		4,5,10	3		V_{CC}	V	
High level input voltage		3	4		V_{CC}	V	
Low level input voltage		3,4,5,10	0		0.7	V	
High level input current		4,5,10			1	μA	V_{IN} = 5.5V, V_{CC} = 5.5V
Low level input current		5			5	μA	V_{IN} = 0V, V_{CC} = 5.5V
Low level input current		4,10			-250	μA	V_{IN} = 0V, V_{CC} = 5.5V
High level input current		3			150	μA	V_{IN} = 5.5V, V_{CC} = 5.5V
Low level input current		3			-1	μA	V_{IN} = 0V, V_{CC} = 5.5V
Clock input hysteresis		5		0.4		V	
Clock rate		5			0.5	MHz	
Data setup time	t_2	4	300			ns	See Fig. 3
Data hold time	t_3	4	600			ns	See Fig. 3
Enable setup time	t_1	10	300			ns	See Fig. 3
Enable hold time	t_5	10	600			ns	See Fig. 3
Clock-to-enable time	t_4	10	300			ns	See Fig. 3
Charge pump output current		1		±150		μA	V pin 1 = 2.0V
Charge pump output leakage current		1			±5	nA	V pin 1 = 2.0V
Drift due to leakage					5	mV/s	At collector of external varicap drive transistor
Charge pump drive output current		18	1			mA	V pin 18 = 0.7V
Charge pump amplifier gain				6400			Pin 18 current = 100μA
Oscillator temperature stability					2	ppm/°C	
Oscillator Stability with Supply Voltage					2	ppm/V	
Recommended crystal series resistance			10		200	Ω	
Crystal oscillator drive level		2		40		mV p-p	
Crystal oscillator source impedance		2		-400		Ω	Nominal spread ±15%

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Ports and Lock Output							
Sink current		6 - 9,11	10			mA	$V_{OUT} = 0.7V$
Port leakage current		6 - 9			10	µA	$V_{OUT} = 13.2V$
Varactor drive amp disable		10	-350			µA	$V_{IN} < 0V$
Charge pump disable		4	-350			µA	$V_{IN} < 0V$

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to $V_{EE} = 0V$

Parameter	Pin SP5026	Pin SP5026S	Value		Units	Conditions
			Min	Max		
Supply voltage	14	12	-0.3	7	V	
Prescaler inputs	15, 16	13, 14		2.5	Vp-p	
Output ports	6-9	6-9	-0.3 -0.3	14 6	V V	Port in off state Port in on state
Prescaler DC offset	15, 16	13, 14	-0.3	$V_{CC} + 0.3$	V	
Loop amplifier DC offset	1, 18	1, 16	-0.3	$V_{CC} + 0.3$	V	
Crystal oscillator DC offset	2	2	-0.3	$V_{CC} + 0.3$	V	
Data bus inputs	4, 5, 10	4, 5, 10	-0.7	$V_{CC} + 0.3$	V	With V_{CC} applied
Storage temperature			-55	+ 125	°C	
Junction temperature				+ 150	°C	
DP18 thermal resistance, chip-to-ambient DP18 thermal resistance, chip-to-case				78 24	°C/W °C/W	
MP16 thermal resistance, chip-to-ambient MP16 thermal resistance, chip-to-case				111 41	°C/W °C/W	
Power consumption at 5.5V				275	mW	All ports off

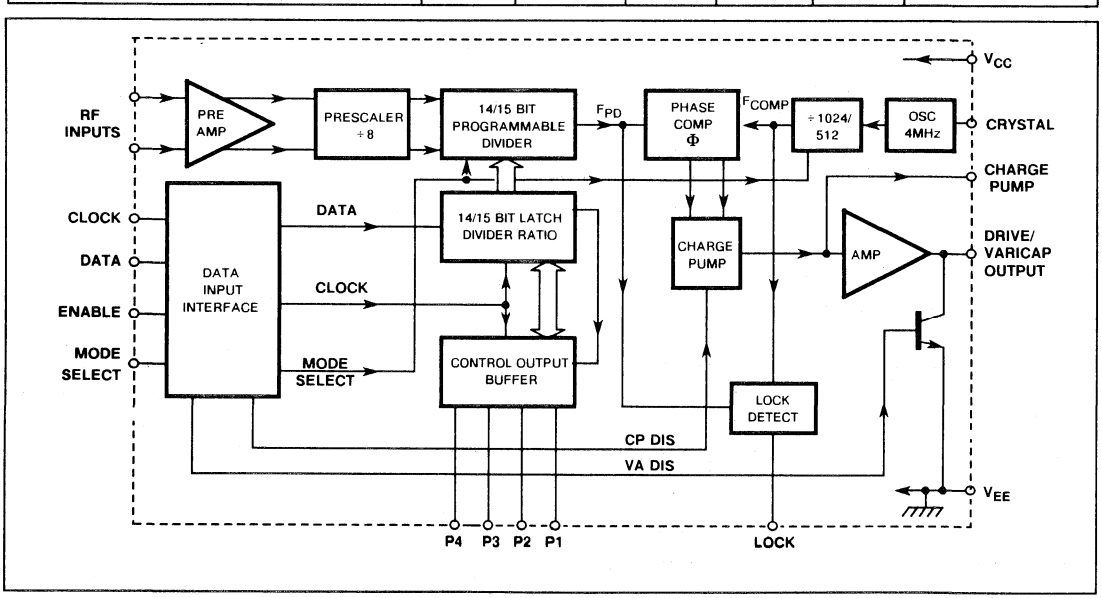


Fig.2. Block diagram of SP5026

FUNCTIONAL DESCRIPTION

The SP5026 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard data, clock, enable, three wire data bus. The data load normally consists of a single word, which contains the frequency and port information, and is only transferred to the internal data shift register during an enable high period. The clock input is disabled during enable low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable, so giving improved fine tune facility for digital AFC etc.

The data sequence and timing follows the format as displayed in Figure 3.

The frequency is set by loading the programmable divider with the required 14/15 bit divisor word. The output of this divider, F_{pd}, is fed to the phase comparator where it is compared in phase and frequency domain to the internally generated comparison frequency, F_{COMP}.

The F_{COMP} is obtained by dividing the output of an on-chip crystal controlled oscillator. The crystal frequency used is generally 4MHz, which gives an F_{COMP} of 3.90625/7.8125kHz and when multiplied back up to the synthesised LO gives a minimum step size of 31.25kHz/62.5kHz respectively.

The programmable divider is preceded by an input RF preamplifier and high speed, low radiation prescaler. The preamplifier is arranged to be self oscillating so giving excellent input sensitivity. The input sensitivity and impedance are shown in Figs. 5 and 7, respectively.

The SP5026 contains an improved lock detect circuit which generates a flag when the loop has attained lock. 'Out of lock' is indicated by high impedance state.

The SP5026 contains 4 general purpose open collector outputs, ports P1-P4, which are capable of sinking up to 10mA. These outputs are set by the remaining four bits within the data word.

PIN COMPATIBILITY

The SP5026 may be used in SP5510 applications which require 3-wire bus as opposed to I²C bus data format. In SP5510 applications where the reference crystal is grounded to pin 3, a small modification is required to ground the crystal as shown in Fig. 4.

Appropriate connections to the mode select input (pin 3) must also be made.

With pin 3 'HIGH' the SP5026 is function compatible with the Toshiba TD6380, and with pin 3 LOW' it is compatible with the TD6382.

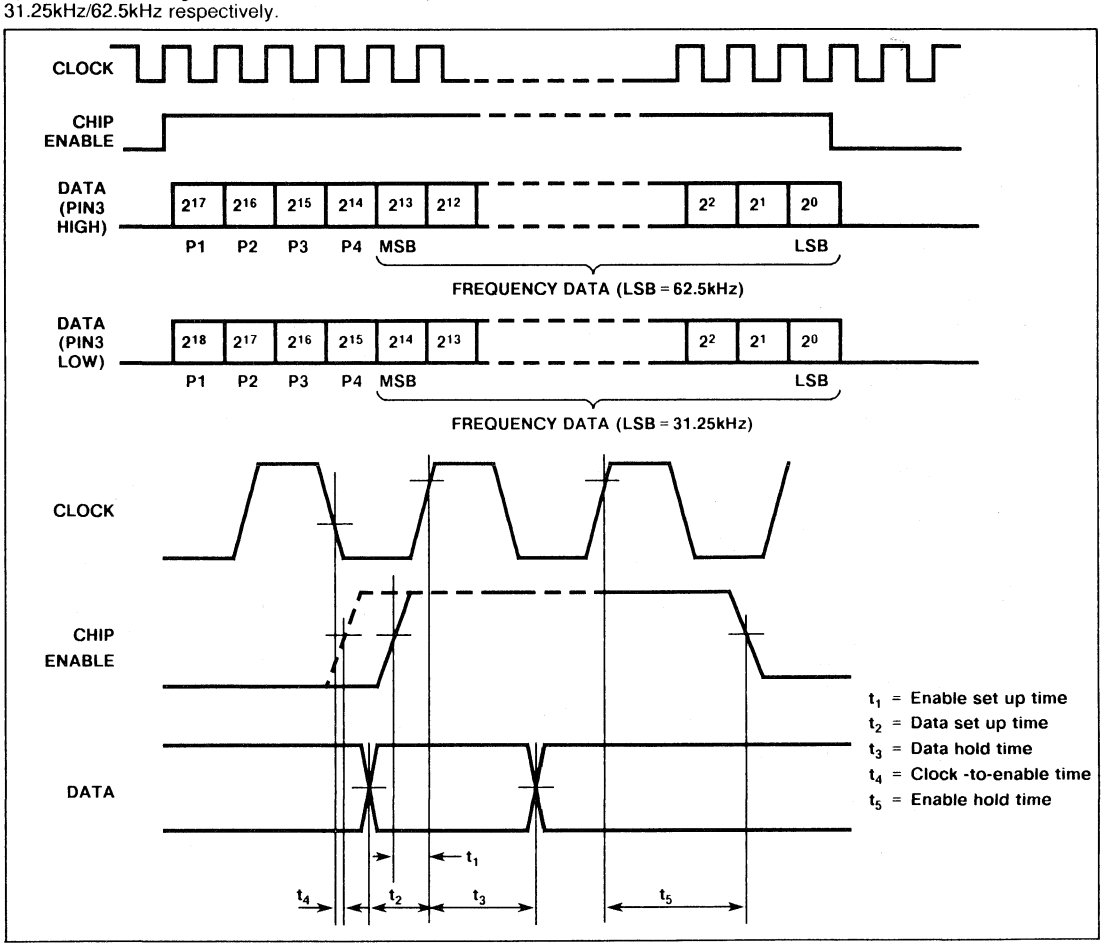


Fig.3 Data format and timing

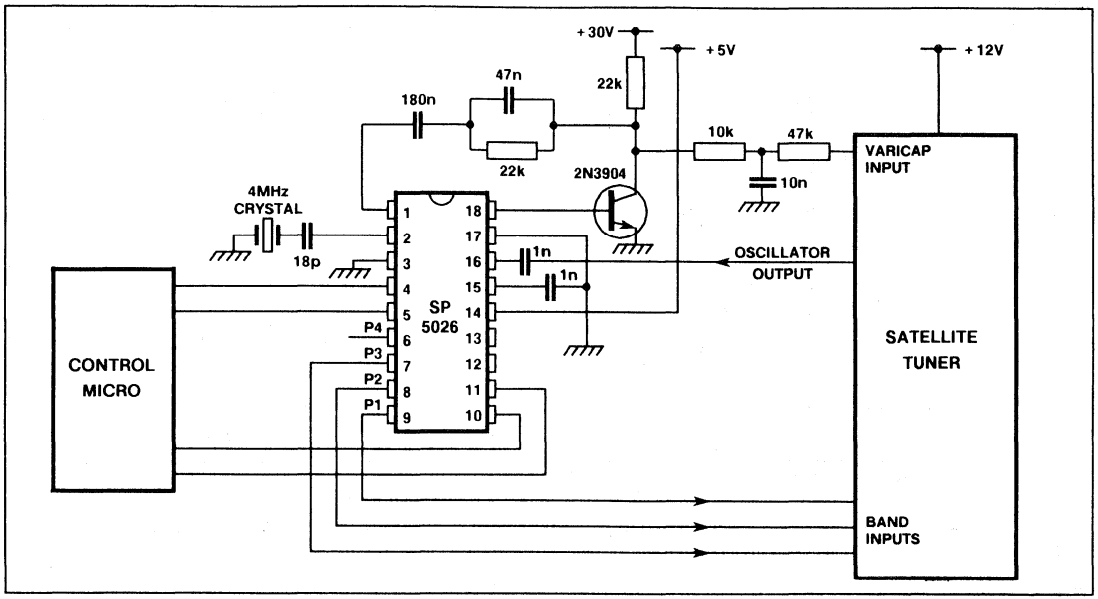


Fig.4 Typical application (F_{STEP} = 31.25kHz)

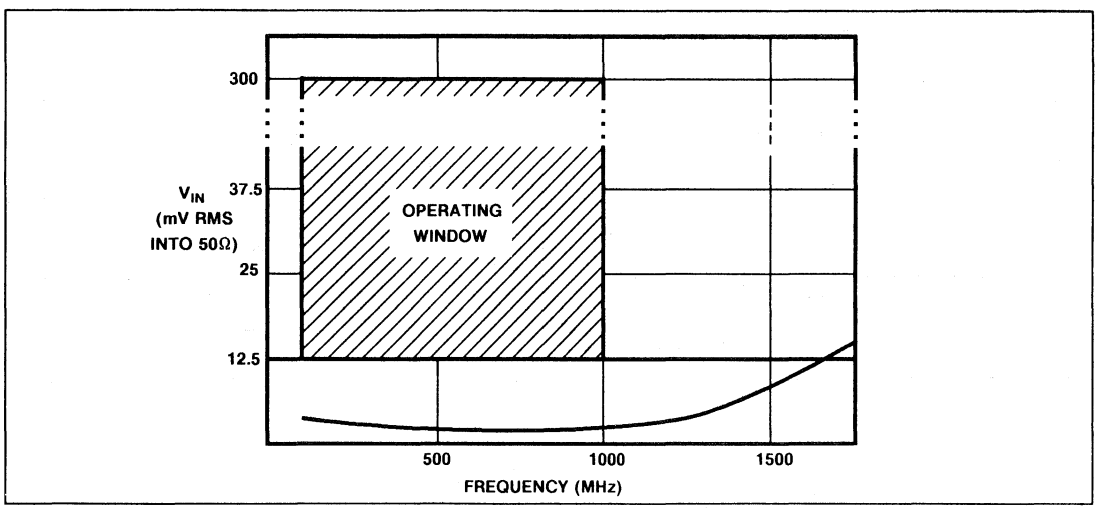


Fig.5 Typical input sensitivity

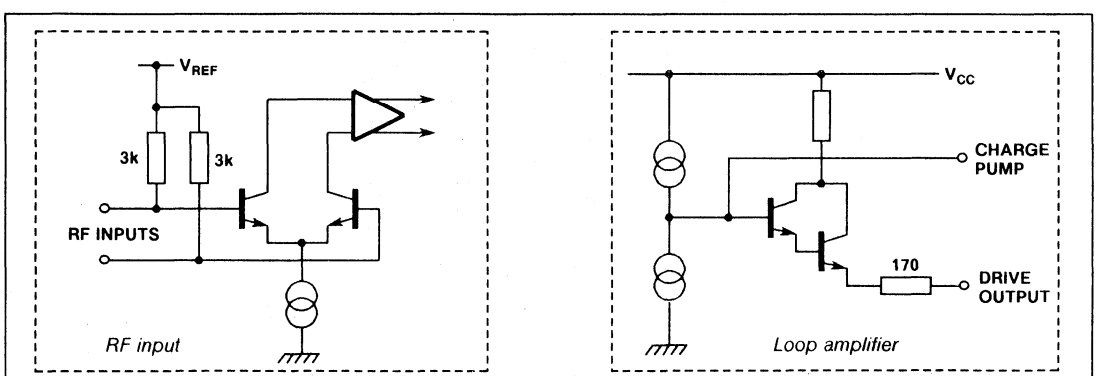


Fig.6a SP5026 input/output interface circuits

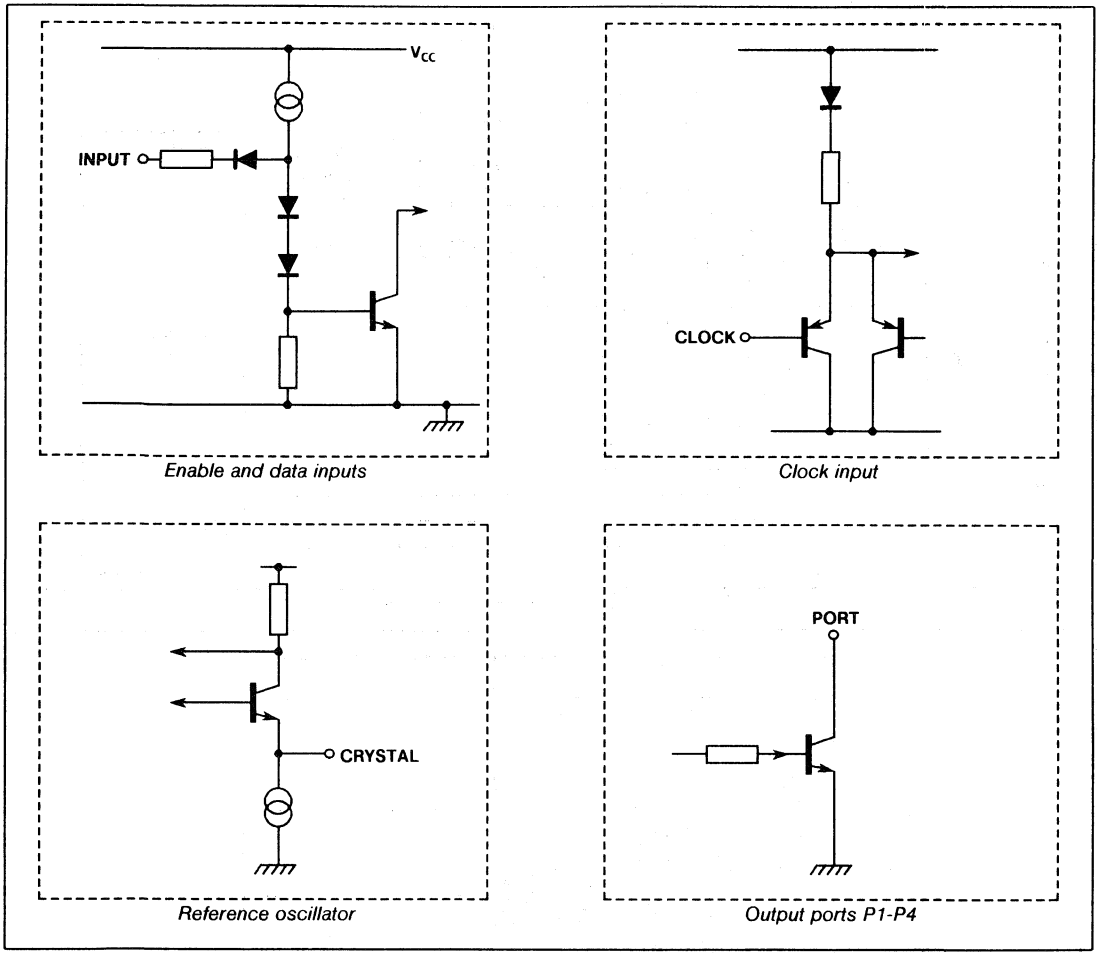


Fig.6b SP5026 input/output interface circuits (continued)

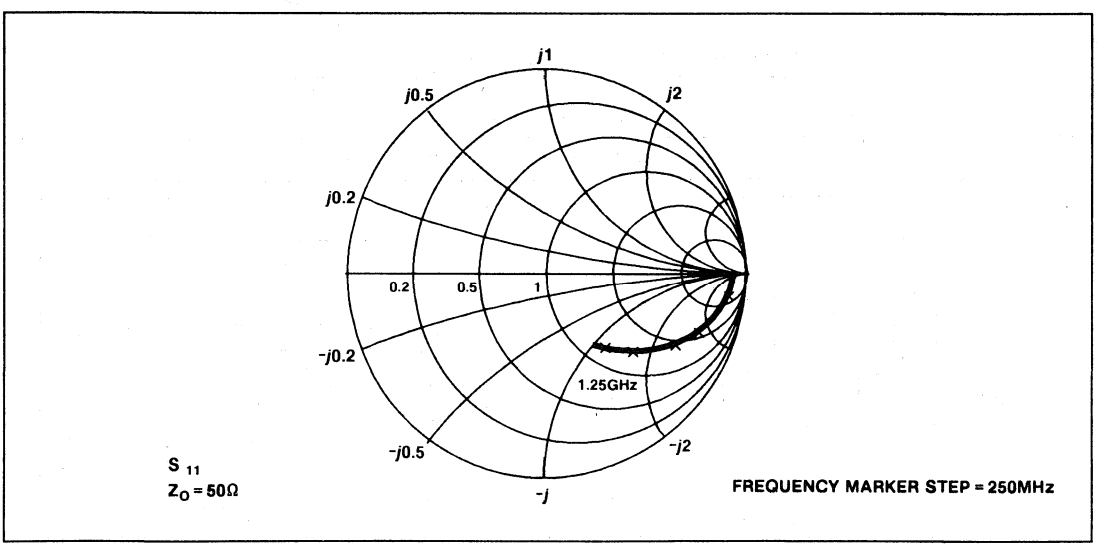


Fig. 7 Typical input impedance

2478-1.0

SP5029

1.0 GHz 3-WIRE BUS CONTROLLED SYNTHESISER

The SP5029 is a programming variant of the SP5510, allowing the design of one tuner with either I²C bus or 3-wire bus format depending on which device is inserted. The SP5029, when used with a TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide-by-8 prescaler with its own preamplifier and a 14-bit programmable divider controlled by a serially - loaded data register. Four open-collector outputs, each independently programmable, are included. The comparison frequency is 7.8125kHz and is derived from a 4MHz crystal controlled on-chip oscillator. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

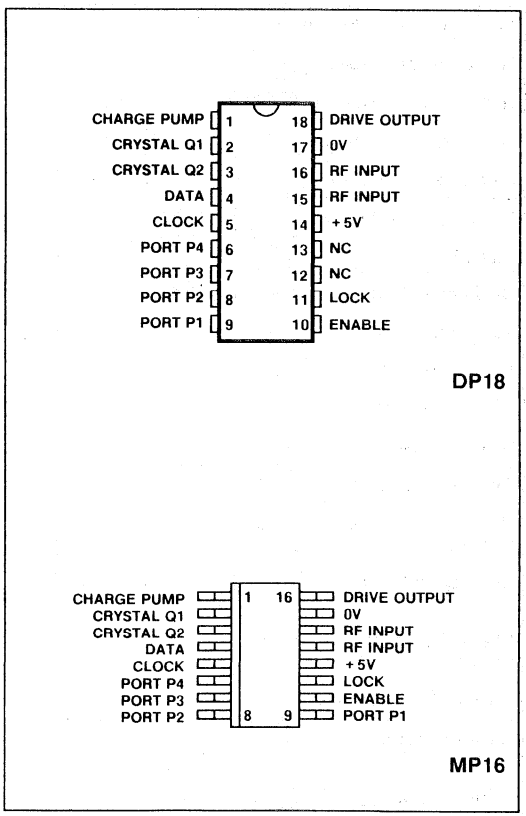


Fig.1 Pin connections - top view

FEATURES

- Complete 1.0GHz Single Chip System
- 62.5kHz Frequency Step Size
- Low Power Consumption (5V 40mA)
- Programming Compatible with Toshiba TD6380 †
- Pin Compatible with SP5510 †
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- Charge Pump Disable
- Single Port 18 Bit Serial Data Entry
- Four Controllable Outputs

† See notes on pin compatibility, page 4.

APPLICATIONS

- Satellite TV When Combined With SP4902 2.5 GHz Prescaler
- Cable Tuning Systems
- VCRs

ORDERING INFORMATION

SP5029 DP
SP5029S MP

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = -10°C to +80°C, V_{CC} = +4.5V to +5.5V Frequency Standard = 4MHz (All pin connections refer to DP package)

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	14		40	55	mA	V_{CC} = 5V
Prescaler Input Voltage		15, 16	12.5		300	mV_{RMS}	50MHz to 1GHz sinewave
Prescaler Input Impedance Input Capacitance		15, 16		50 2		Ω pF	
High Level Input Voltage		4,5,10	3		V_{CC}	V	
Low Level Input Voltage		4,5,10	0		0.7	V	
High Level Input Current		4,5,10			1	μA	V_{IN} = 5.5V V_{CC} = 5.5V
Low Level Input Current		5			5	μA	V_{IN} = 0V V_{CC} = 5.5V
Low Level Input Current		4,10			-250	μA	V_{IN} = 0V V_{CC} = 5.5V
Clock Input Hysteresis		5		0.4		V	
Clock Rate		5			0. 5	MHz	
Data Setup Time	t_2	4	300			ns	See Fig. 3
Data Hold Time	t_3	4	600			ns	See Fig. 3
Enable Setup Time	t_1	10	300			ns	See Fig. 3
Enable Hold Time	t_5	10	600			ns	See Fig. 3
Clock-to-Enable Time	t_4	10	300			ns	See Fig. 3
Charge Pump Output Current		1		±150		μA	V pin 1 = 2.0V
Charge Pump Output Leakage Current		1			±5	nA	V pin 1 = 2.0V
Drift Due to Leakage					5	mV/s	At Collector of External Varicap Drive Transistor
Charge Pump Drive Output Current		18	1			mA	V pin 18 = 0.7V
Charge Pump Amplifier Gain				6400			Pin 18 Current 100μA
Oscillator Temperature Stability *					2	ppm/°C	
Oscillator Stability with Supply Voltage *					2	ppm/V	
Recommended Crystal Series Resistance *			10		200	Ω	
Crystal Oscillator Drive Level *		2		40		mV p-p	
Crystal Oscillator Source Impedance *		2		-400		Ω	Nominal Spread ±15%

*Not tested in production

ELECTRICAL CHARACTERISTICS (continued)

Test conditions (unless otherwise stated)

T_{amb} = -10°C to + 80°C, V_{CC} = + 4.5V to + 5.5V, Frequency Standard = 4MHz (All pin connections refer to DP package)

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Ports and Lock output							
Sink Current		6 - 9,11	10			mA	V_{OUT} = 0.7V
Port Leakage Current		6 - 9			10	μA	V_{OUT} = 13.2V
Varactor Drive Amp Disable		10	-350			μA	V_{IN} < 0V
Charge Pump Disable		4	-350			μA	V_{IN} < 0V

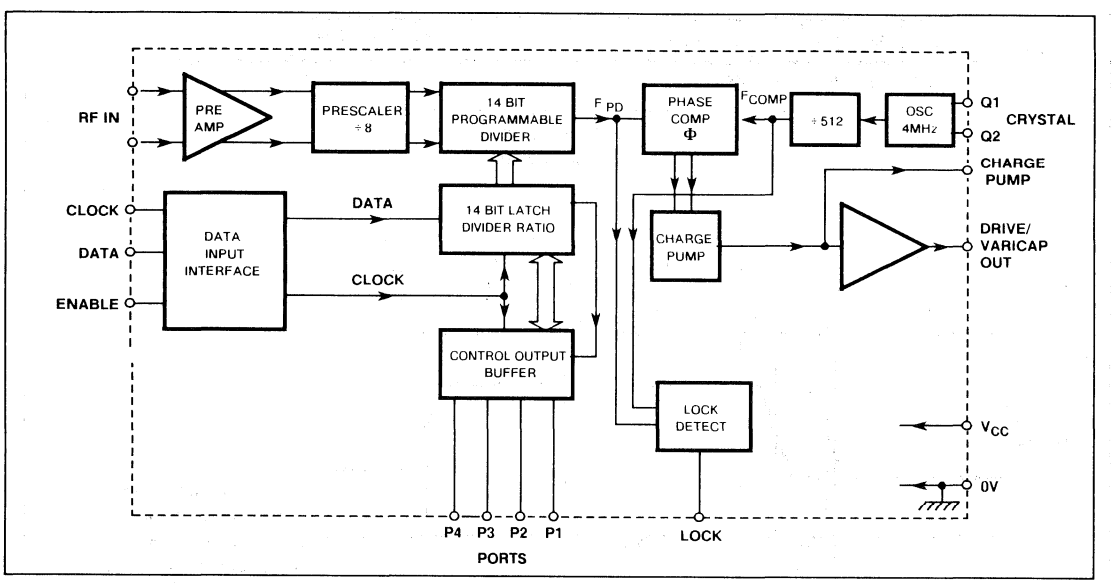


Fig.2. Block diagram of SP5029

FUNCTIONAL DESCRIPTION

The SP5029 contains all the elements necessary (with the exception of reference crystal, loop filter and external high voltage transistor) to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard data, clock and enable three-wire data bus. The data load normally consists of a single word, which contains the frequency and port information, and is only transferred to the internal data shift register during an enable high period. The clock input is disabled during enable low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable, so giving improved fine tune facility for digital AFC etc.

The data sequence and timing follows the format as shown in Fig. 3.

The frequency is set by loading the programmable divider with the required 14 bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator where it is compared in phase and frequency domain to the internally generated comparison frequency, F_{COMP}.

The F_{COMP} is obtained by dividing the output of an on-chip crystal controlled oscillator. The crystal frequency used is generally 4MHz, which gives an F_{COMP} of 7.8125kHz and, when multiplied back up to the synthesised LO, gives a minimum step size of 62.5kHz.

The programmable divider is preceded by an input RF preamplifier and high speed, low radiation prescaler. The preamplifier is arranged to be self oscillating so giving excellent input sensitivity.

The SP5029 contains an improved lock detect circuit which generates a flag when the loop has attained lock. In lock' is indicated by high impedance state.

The SP5029 contains 4 general purpose open collector outputs, ports P1-P4, which are capable of sinking at least 10mA. These outputs are set by the remaining four bits within the data word.

PIN COMPATIBILITY

The SP5029 may be used in SP5510 applications which require 3-wire bus as opposed to I²C bus data format. It is programming and step size compatible with the Toshiba TD6380.

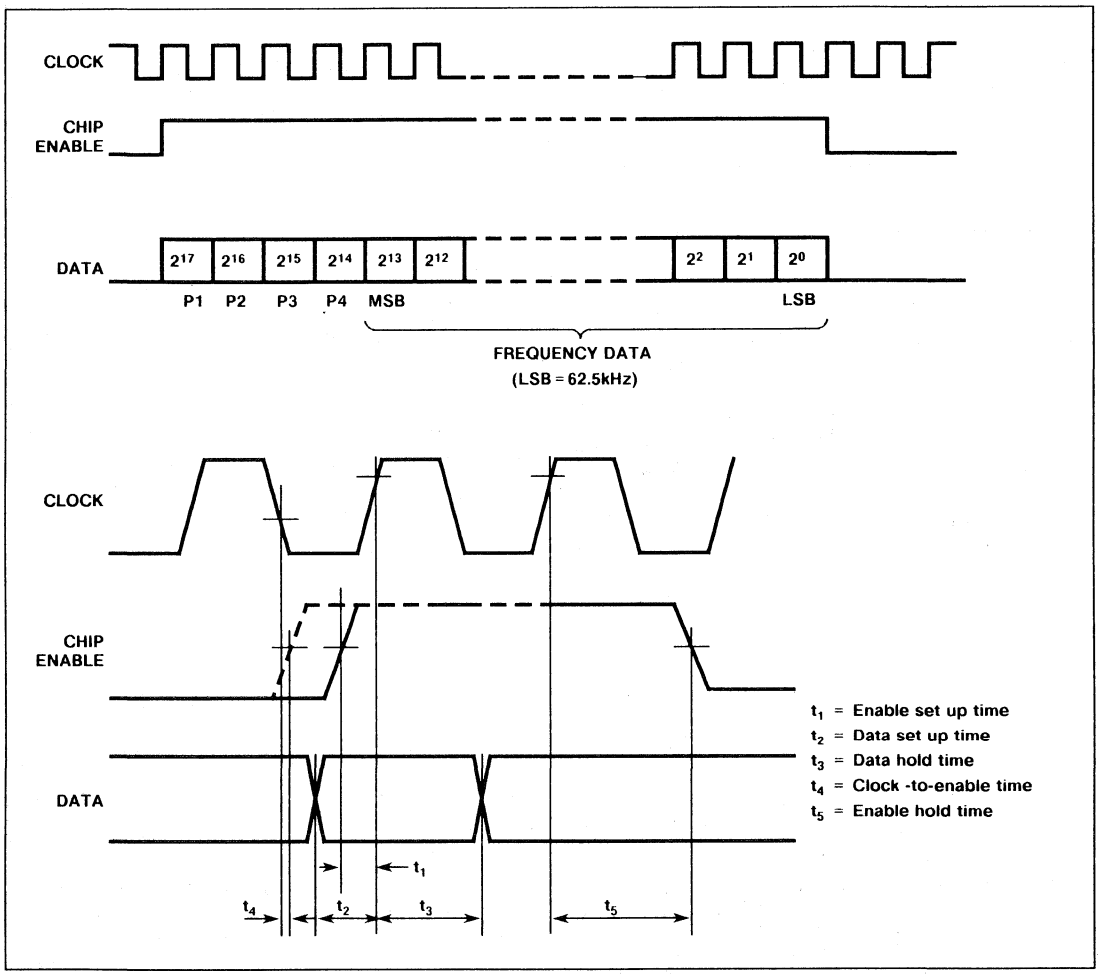


Fig.3. Data format and timing

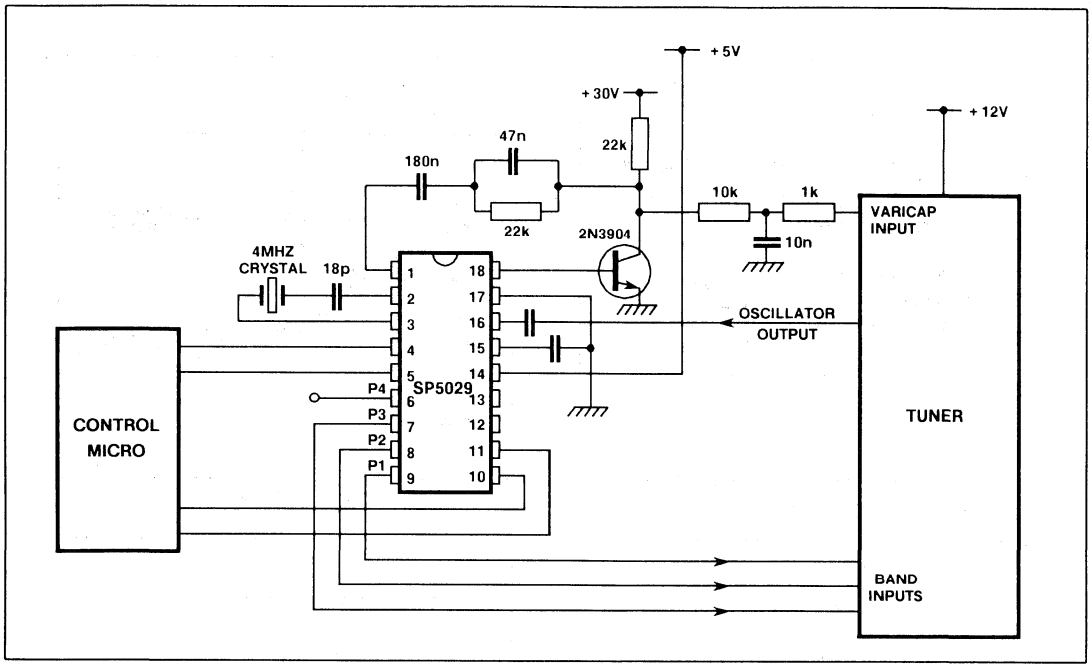


Fig.4. Typical application (F_{STEP} = 62.5kHz)

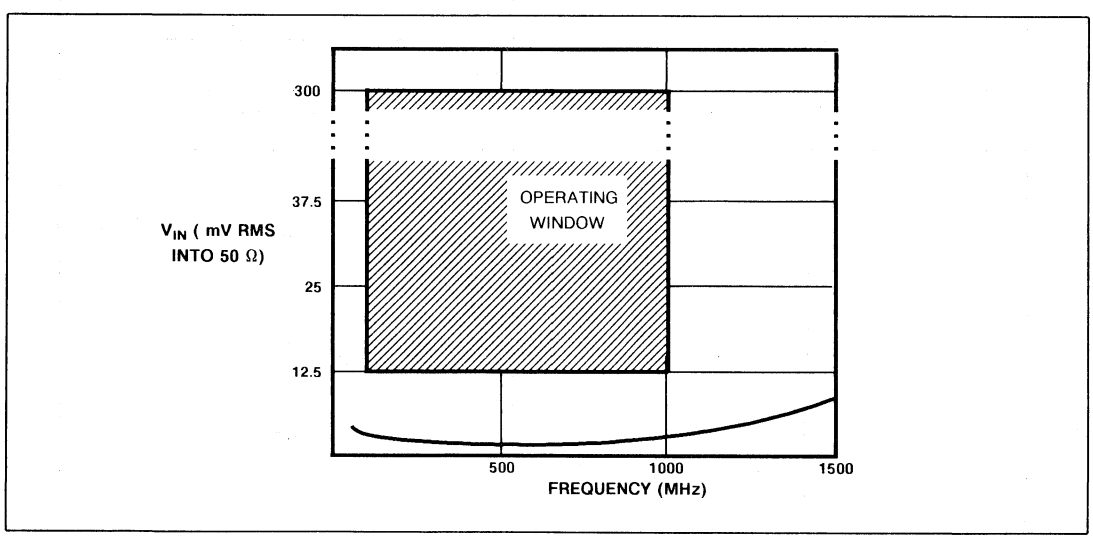
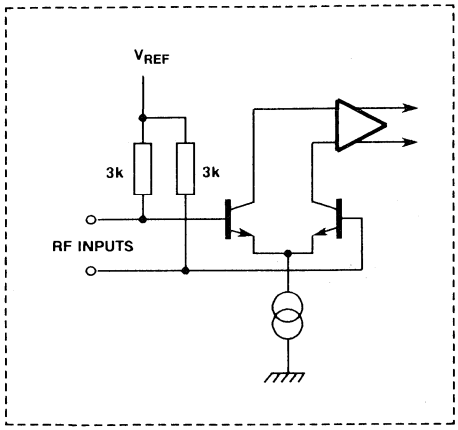
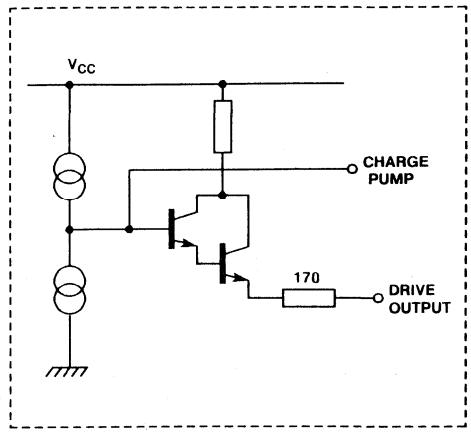


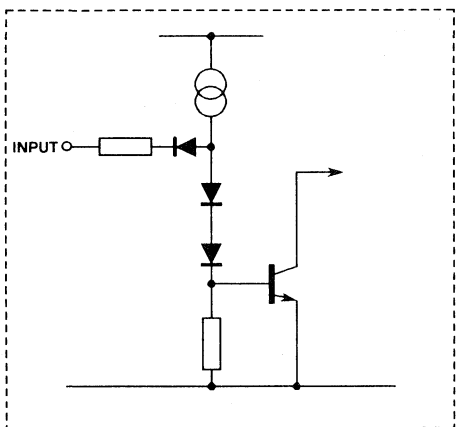
Fig.5. Typical input sensitivity



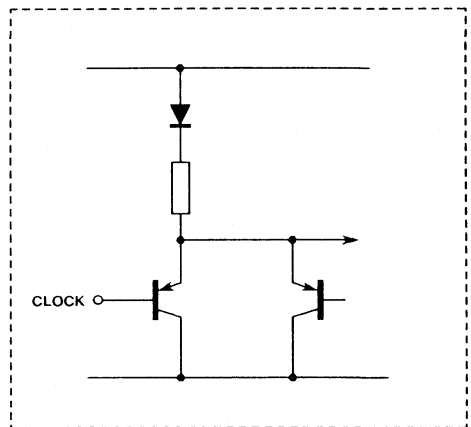
RF input



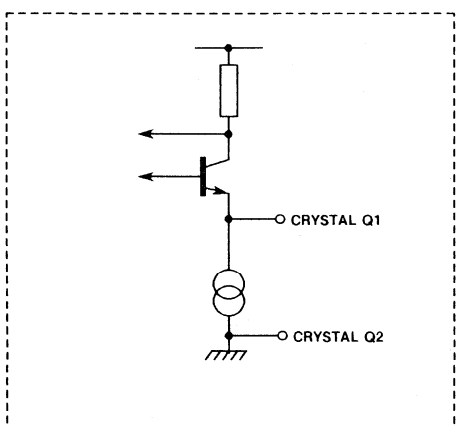
Loop amplifier



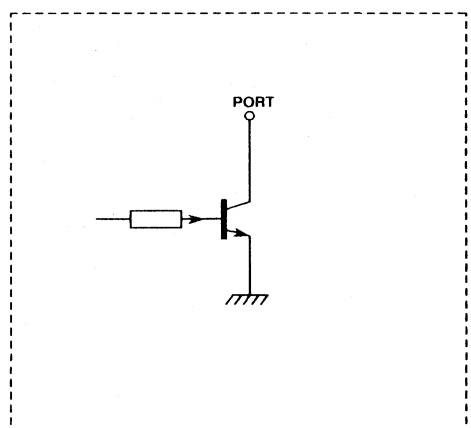
Enable and data inputs



Clock input



Reference oscillator



Output ports P1-P4

Fig.6 SP5029 Input/output interface circuits

SP5050/1

1.8/2GHz SINGLE CHIP FREQUENCY SYNTHESISER

The SP5050/1, used with a voltage controlled oscillator, forms a complete phase locked loop system. The circuit consists of a divide-by-32 prescaler with its own preamplifier and a 14 bit programmable divider controlled by a serially-loaded data register. Control selection lines are also included and give 4 switch output combinations on 3 lines. The frequency/phase comparator is fed with a 3.90625kHz reference, derived from the 4 MHz crystal controlled on-chip oscillator. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

FEATURES

- Complete Single Chip System for Microprocessor Control
- Operating Supply 5V, 90mA/70mA
- Prescaler and Preamplifier Included
- Single Port 16-Bit Serial Data Entry
- Frequencies up to 2048MHz in 125kHz Steps (with 4.0MHz Ref)
- High Comparator Frequency Simplifies Charge Pump Filter
- 3 Selectable Control Outputs Are Available
- Charge Pump Amplifier with Feedback and Disable
- Crystal Controlled Output Clock at 62.5kHz

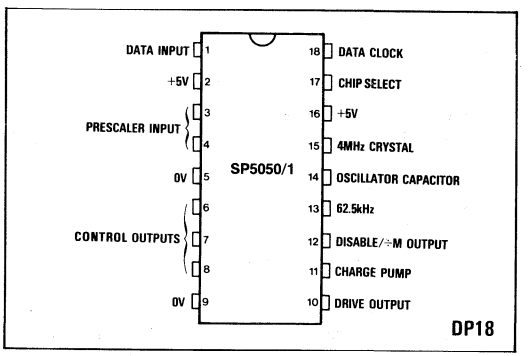


Fig.1 Pin connections - top view

Control select data		Control outputs Pin		
2^{15}	2^{14}	6	7	8
0	0	H	H	H
0	1	H	L	H
1	0	L	H	H
1	1	H	H	L

Table 1 Control select decoding

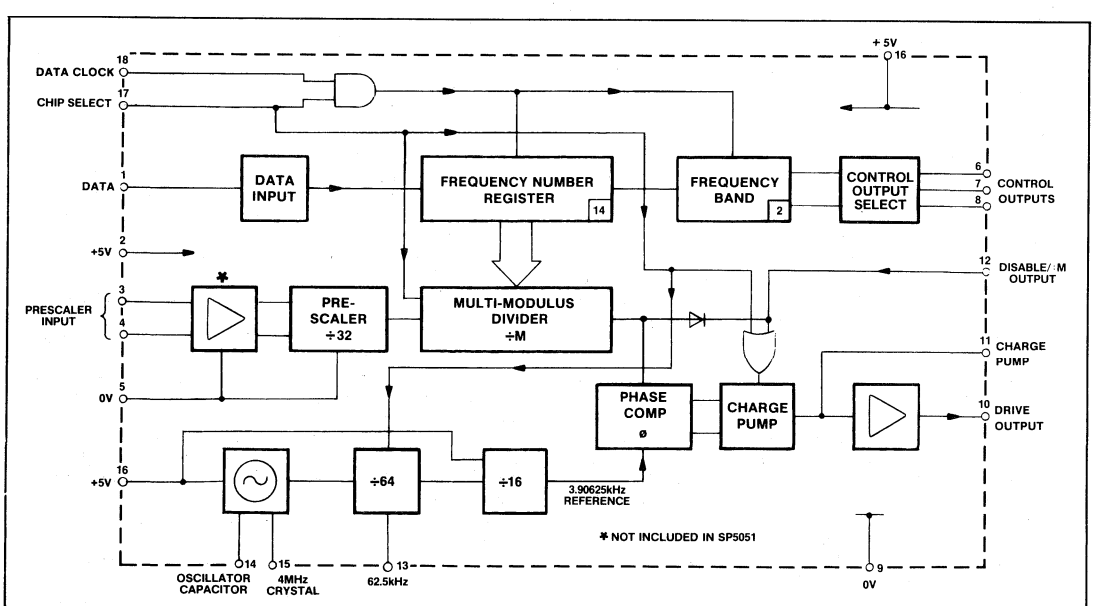


Fig.2 SP5050/1 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{CC} = 5V, Frequency standard = 4MHz

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Operating voltage	V_{CC}	2,16	4.5		5.5	V	
Supply current	I_{CC}	2		85		mA	SP5051
Supply current	I_{CC}	2		70		mA	SP5050
Prescaler input voltage		3,4		50		mV	300MHz to 1.8GHz sinewave - SP5050
		3,4	100			mV	See Fig.4,5 - SP5051
Prescaler input impedance		3,4	50			Ω	See Fig.6
High level input voltage		1,12,17,18	3.5		V_{CC}	V	
Low level input voltage		1,12,17,18	0		1.5	V	
High level input current		1,12,17			0.4	mA	V_{IN} = 5V
Input current		18			5	μA	V_{IN} = 3.5V
Multi-modulus divider output swing		12		350		mV	6.8k to 0V. Provided for test purposes only
Data clock input hysteresis		18		0.6		V	
Data clock rate		18			0.5	MHz	
Data setup time	t_{setup}	1,18	0.5			μs	See Fig.3
Chip select timing	csd(pos)	17,18	0		t_C	μs	See Fig.3
Chip select timing	csd(neg)	17,18	0.5			μs	See Fig.3
External oscillator input		14,15		250		mV	AC coupled
Charge pump output current		11	±75	±100	±125	μA	V Pin 11 = 2.0V
Charge pump output leakage		11			±1	μA	V Pin 11 = 2.0V
Drift due to leakage					5	mV/s	At collector of external varicap drive transistor
Oscillator temperature stability		14,15		0.12		ppm/°C	Over 0°C to 65°C temperature range. IC variation only.
Oscillator stability with supply voltage		14,15		0.25		ppm/V	V_{CC} = 4.5V to 5.5V
Charge pump drive output current	I_{OUT}	10	1			mA	V Pin 10 = 0.7V
Control output leakage current		6,7,8			5	μA	V Pins 6,7 and 8 = 13.5V
Control output current		6,7,8	1	1.3		mA	V_{OUT} = 12V
Clock output leakage current		13			5	μA	V Pin 13 = 5.5V
Clock output saturation voltage		13			0.5	V	I Pin 13 = 1mA

DESCRIPTION

The phase comparator reference frequency at 3.90625kHz is obtained by division of the 4MHz on chip crystal controlled oscillator frequency. An outpt at 62.5kHz is provided at Pin 13.

In order to achieve a high sensitivity at the tuner local oscillator pick off point, the divide-by-32 prescaler is preceded by a differential amplifier with inputs on Pins 3 and 4. The SP5051 does not contain this preamp as it limits the frequency range. But as a consequence the SP5051 is not as sensitive as the SP5050 in the lower frequency region.

The divide-by-32 prescaler output drives the multi-modulus divider, which, when the loop is locked, produces an output, frequency and phase locked to the 3.90625kHz reference.

Synthesis of the complete range of frequencies from 64 MHz to 2048MHz is provided by varying the division ratio of the multi-modulus divider according to data applied from an external control system. The data,applied as a 16-bit serial word,is loaded using the data clock and select lines from the control system into a storage register with fourteen bits controlling the multi-modulus divider,while the remaining bits determine the control outputs on Pins 6,7 and 8.

Data from the serial input, Pin 1 is clocked into the storage register by the positive edge of the data clock waveform on Pin 18 when the chip select input on Pin 17 is high. The chip select input should be timed to go high during the low portion of the clock waveform otherwise a positive transition coincident with the select signal will be applied to the storage register clock possibly causing a misreading of the applied data.

Figure 3 and Table 1 show the data format and timing requirements.

A single external transistor driven from the charge pump output provides the 30V swing necessary on the oscillator varicap input. To prevent unwanted frequency variations when data is being entered, the charge pump is disabled by chip select.

Pin 12 is a dual input/output pin, the normal function being to disable the charge pump when the input is taken high. The alternative output function is provided for test purposes only and allows the ÷M counter output to be monitored. This signal is available at low amplitude when Pin 12 is loaded to ground by a 6.8k resistor.

To improve stability the +5V and ground supplies to the chip are split and brought out to separate pins, it is therefore essential to connect all four supply pins for the device to operate.

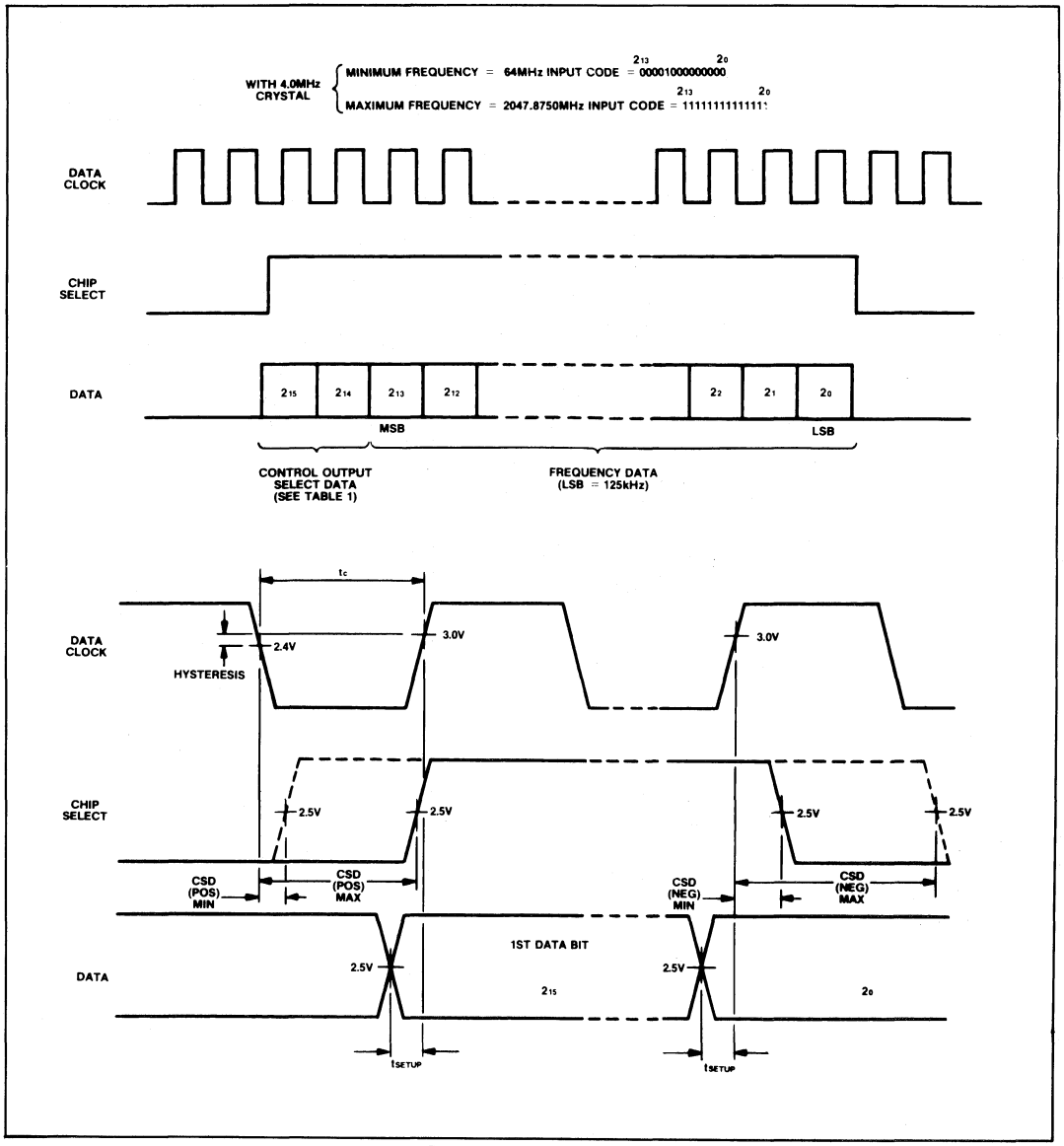


Fig.3 Data format and timing

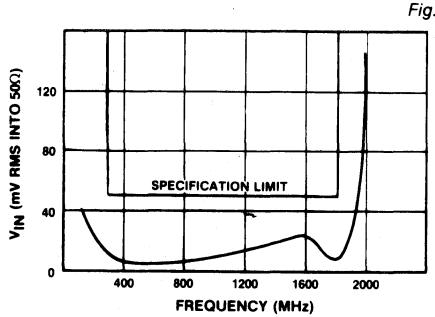


Fig.4 SP5050 typical input sensitivity

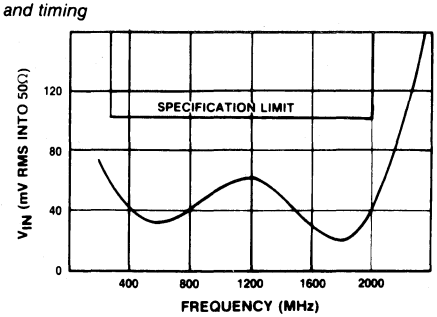


Fig.5 SP5051 typical input sensitivity

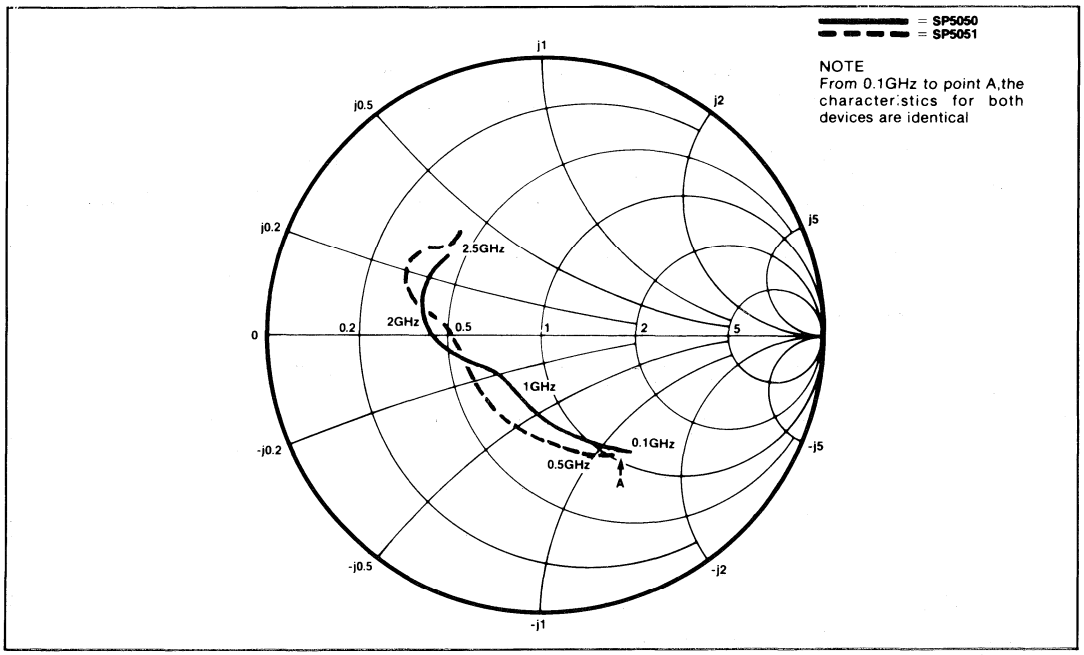


Fig.6 Typical input impedance frequencies in MHz. Normalised to 50Ω

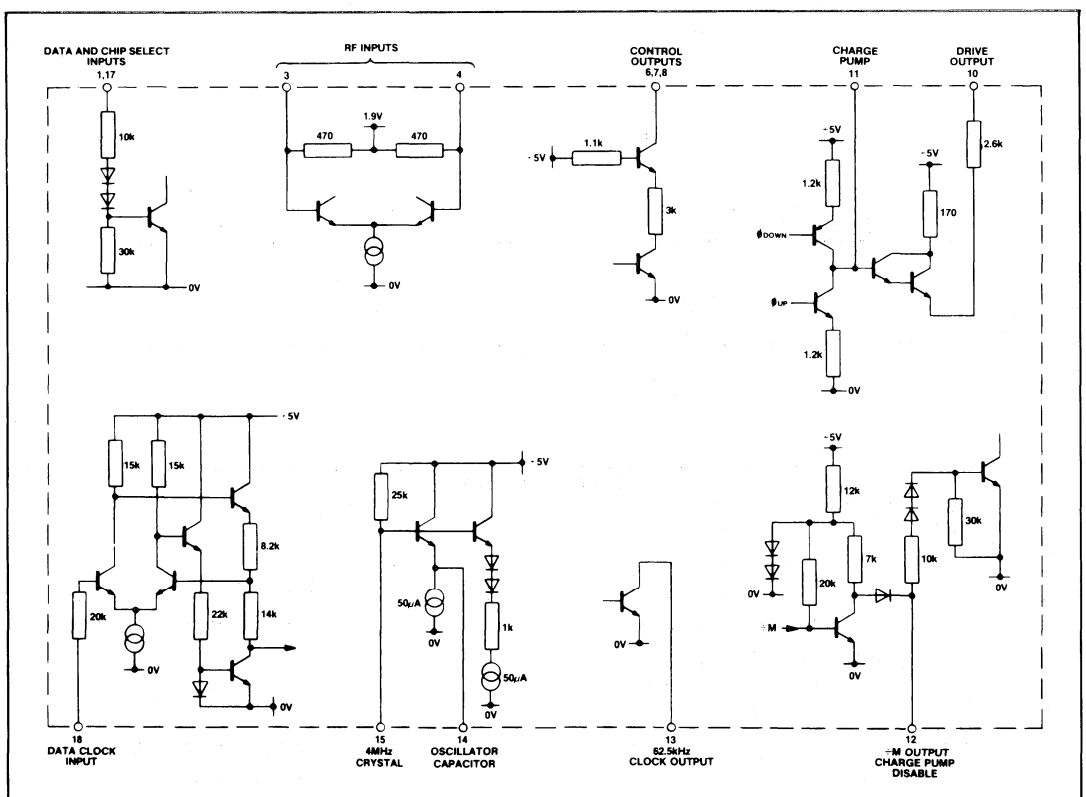


Fig.7 SP5050/1 input/output interface circuits

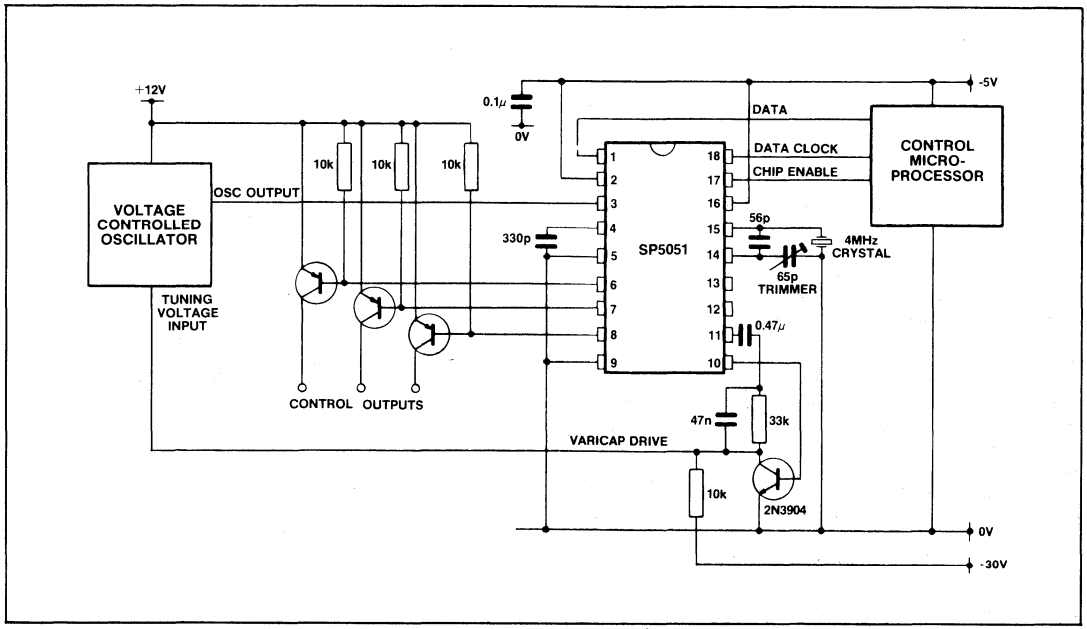


Fig.8 Application for controlling a 2GHz oscillator

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	-10° C to +65° C
Storage temperature	-55° C to +125° C
Supply voltage Pin 2 and 16	7V
Band select output voltage Pins 6,7,8	14V
Prescaler input voltage	2.5V p-p

SP5054

2.5 GHz 3-WIRE BUS CONTROLLED SYNTHESIZER

The SP5054 is a single chip frequency synthesizer designed for satellite TV tuning systems. It is a programming variant of the SP5055 allowing the design of one tuner with either I²C bus or 3-wire bus format depending on which device is inserted. The SP5054, when used with a satellite TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide-by-16 prescaler with its own preamplifier and a 14/15 bit programmable divider controlled by a serially - loaded data register. Four independently programmable open-collector outputs are included. The device has four modes of operation, selected by the 'mode select input.' These modes are summarised in Table 1.

The comparison frequencies are obtained from a 4MHz crystal controlled on-chip oscillator. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

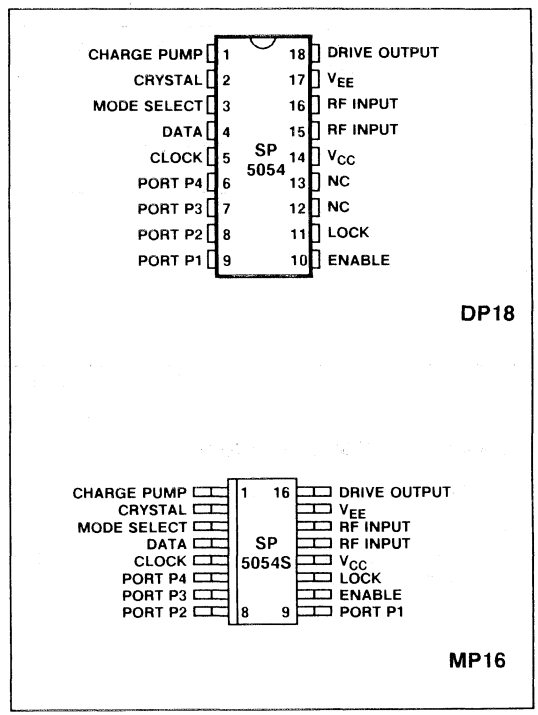


Fig.1 Pin connections - top view

FEATURES

- Complete 2.5GHz Single Chip System
- 62.5kHz, 100kHz and 125kHz Step Size
- Low Power Consumption (5V 65mA)
- Programming Compatible with Toshiba TD6380, TD6381 and TD6382 *
- Pin Compatible with SP5055 *
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- Charge Pump Disable
- Single Port 18/19 Bit Serial Data Entry
- Four Controllable Outputs
- Full ESD Protection †

* See notes on pin compatibility, page 1-100.
† Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

ORDERING INFORMATION

SP5054 DP - (18 lead Plastic Package)
SP5054S MP - (16 lead Miniature Plastic Package)

ELECTRICAL CHARACTERISTICS

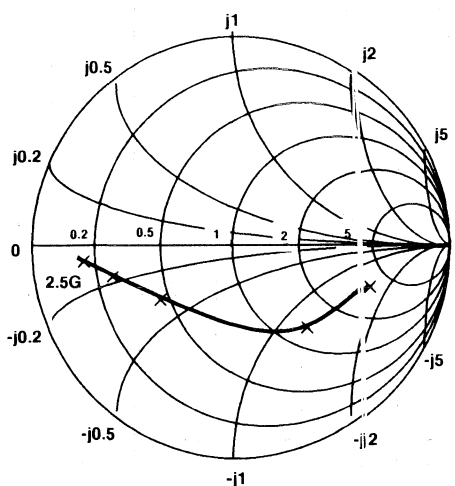
T_{amb} = -20°C to +80°C, V_{CC} = +4.5V to +5.5V Frequency Standard = 4MHz. All pin connections refer to SP5054 (DP package). These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	14		65	80	mA	V_{CC} = 5V
Prescaler input voltage		15, 16	50		400	mV_{RMS}	500MHz to 1.8GHz sinewave
Prescaler input voltage		15, 16	100		400	mV_{RMS}	2.5GHz, see Fig. 6
Prescaler input impedance Input capacitance		15, 16		50 2		Ω pF	
High level input voltage		4,5,10	3		V_{CC}	V	
Low level input voltage		4,5,10	0		0.7	V	
High level input current		4,5,10			1	μA	V_{IN} = 5.5V, V_{CC} = 5.5V
Low level input current		5			5	μA	V_{IN} = 0V, V_{CC} = 5.5V
Low level input current		4,10			-250	μA	V_{IN} = 0V, V_{CC} = 5.5V
High level input current		3			700	μA	V_{IN} = 5.5V, V_{CC} = 5.5V
Low level input current		3			-700	μA	V_{IN} = 0V, V_{CC} = 5.5V
Clock input hysteresis		5		0.4		V	
Clock rate		5			0.5	MHz	
Data setup time	t_2	4	300			ns	See Fig. 4
Data hold time	t_3	4	600			ns	See Fig. 4
Enable setup time	t_1	1,10	300			ns	See Fig. 4
Enable hold time	t_5	1,10	600			ns	See Fig. 4
Clock-to-enable time	t_4	1,10	300			ns	See Fig. 4
Charge pump output current		1		±150		μA	V pin 1 = 2.0V
Charge pump output leakage current		1			±5	nA	V pin 1 = 2.0V
Drift due to leakage					5	mV/s	At collector of external varicap drive transistor
Charge pump drive output current		18	1			mA	V pin 18 = 0.7V
Charge pump amplifier gain				6400			Pin 18 current = 100μA
Oscillator temperature stability					2	ppm/°C	
Oscillator Stability with Supply Voltage					2	ppm/V	
Recommended crystal series resistance			10		200	Ω	
Crystal oscillator drive level		2		40		mV p-p	
Crystal oscillator source impedance		2		-400		Ω	Nominal spread ±15%
Ports and lock output							
Sink Current		6 - 9,11	10			mA	V_{OUT} = 0.7V
Port leakage current		6 - 9			10	μA	V_{OUT} = 13.2V
Varactor drive amp disable		10	-350			μA	V_{IN} < 0V
Charge pump disable		4	-350			μA	V_{IN} < 0V

ABSOLUTE MAXIMUM RATINGS

(All voltages are referred to $V_{EE} = 0V$)

Parameter	Pin (DP)	Pin (MP)	Value Min	Value Max	Units	Conditions
Supply voltage	14	12	-0.3	7	V	
Prescaler inputs	15, 16	13, 14		2.5	Vp-p	
Output ports	6-9	6-9	-0.3 -0.3	14 6	V V	Port in off state Port in on state
Prescaler DC offset	15, 16	13, 14	-0.3	$V_{CC}+0.3$	V	
Loop amplifier DC offset	1, 18	1, 16	-0.3	$V_{CC}+0.3$	V	
Crystal oscillator DC offset	2	2	-0.3	$V_{CC}+0.3$	V	
Data bus inputs	4, 5, 10	4, 5, 10	-0.7	$V_{CC}+0.3$	V	With V_{CC} applied
Storage temperature			-55	+125	°C	
Junction temperature				+150	°C	
DP18 thermal resistance, chip-to-ambient DP18 thermal resistance, chip-to-case				78 24	°C/W °C/W	
MP16 thermal resistance, chip-to-ambient MP16 thermal resistance, chip-to-case				111 41	°C/W °C/W	
Power consumption at 5.5V				440	mW	All ports off



S_{11}:$Z_O = 50\Omega$

FREQUENCY MARKER STEP = 500MHz

Fig.2 Typical input impedance

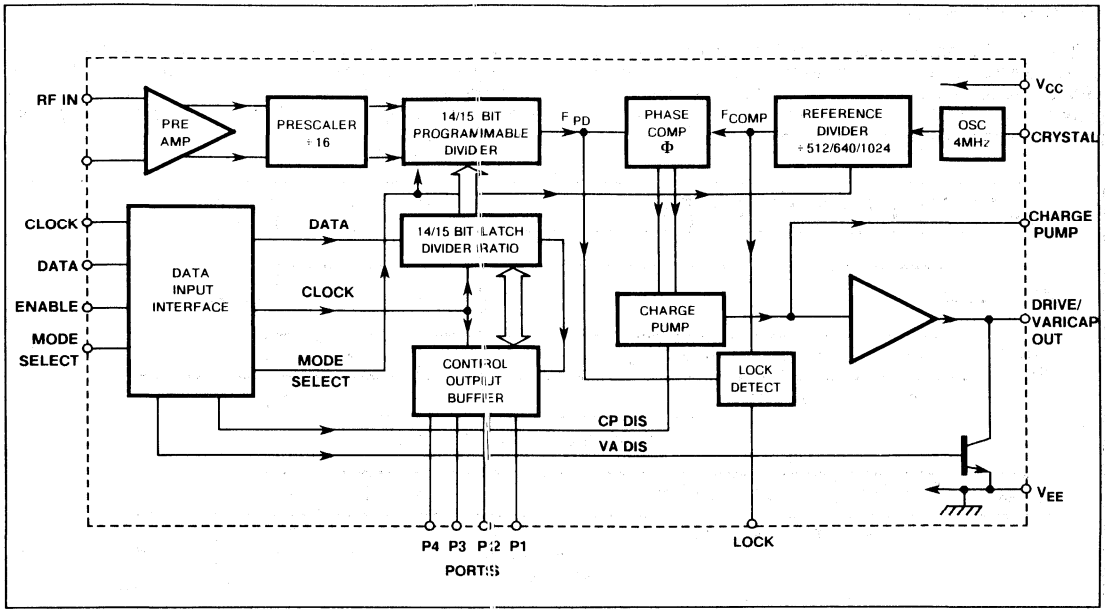


Fig.3. Block diagram of SP5054

Mode	'Mode Select' input voltage	Programmable divider bit length	Reference divider ratio	* Frequency step size (kHz)	* Maximum operating frequency (GHz)
3	0.925 V_{CC} - V_{CC}	14	512	125	2.0479
2	0.675 V_{CC} - 0.825 V_{CC}	15	512	125	2.5
1	Open Circuit	15	1024	62.5	2.0479
0	0 - 0.325 V_{CC}	15	640	100	2.5

Table1 SP5054 modes of operation

** Using a 4MHz crystal*

FUNCTIONAL DESCRIPTION

The SP5054 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor, to control a voltage controlled local oscillator, so forming a PLL frequency synthesized source.

The system is controlled by a microprocessor via a standard data, clock, enable, three-wire data bus. The data load normally consists of a single word, which contains the frequency and port information, and is only transferred to the internal data shift register during an enable high period. The clock input is disabled during enable low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable, so giving improved fine tune facility for digital AFC etc.

The data sequence and timing follows the format as shown in Fig. 4.

The frequency is set by loading the programmable divider with the required 14/15 bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator where it is compared in phase and frequency domain to the internally generated comparison frequency, F_{COMP}.

F_{COMP} is obtained by dividing the output of an on-chip crystal controlled oscillator. The crystal frequency used is generally 4MHz, which gives an F_{COMP} of 3.90625/6.25/7.8125kHz and, when multiplied back up to the synthesized LO, gives a minimum step size of 62.5/100/125kHz, respectively.

The programmable divider is preceded by an input RF preamplifier and high speed, low radiation prescaler. The preamplifier is arranged to be self oscillating so giving excellent input sensitivity.

The SP5054 contains an improved lock detect circuit which generates a flag when the loop has attained lock. 'In lock' is indicated by high impedance state.

The SP5054 contains 4 general purpose open collector outputs, ports P1-P4, which are capable of sinking at least 10mA. These outputs are set by the remaining four bits within the normal data word.

PIN COMPATIBILITY

The SP5054 may be used in SP5055 applications which require 3-wire bus as opposed to I²C bus data format. In SP5055 applications where the reference crystal is grounded to pin 3, a small modification is required to ground the crystal as shown in Fig. 5.

Appropriate connections must also be made to the mode select input (see Table 1). In mode 3, the SP5054 is programming compatible with the Toshiba TD6380, modes 0 and 2 are compatible with TD6381; mode 1 is compatible with TD6382.

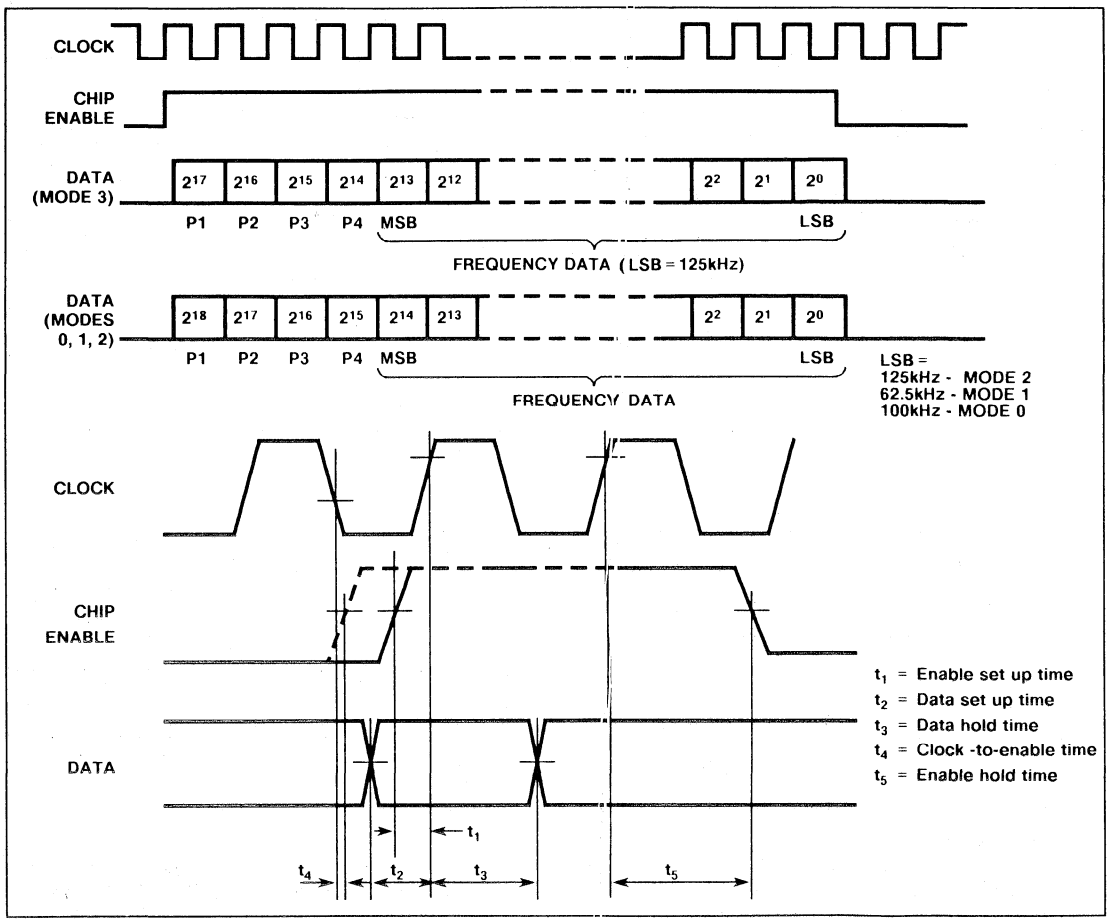


Fig.4 Data format and timing

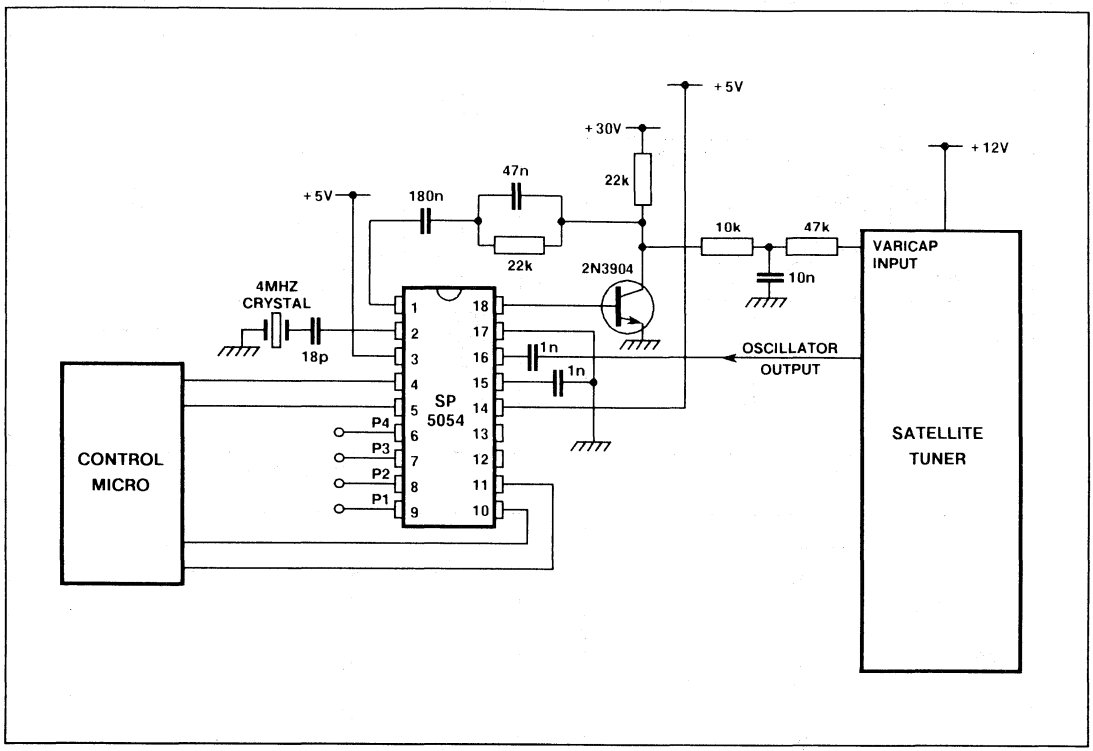


Fig.5. Typical application (F_{STEP} = 125kHz)

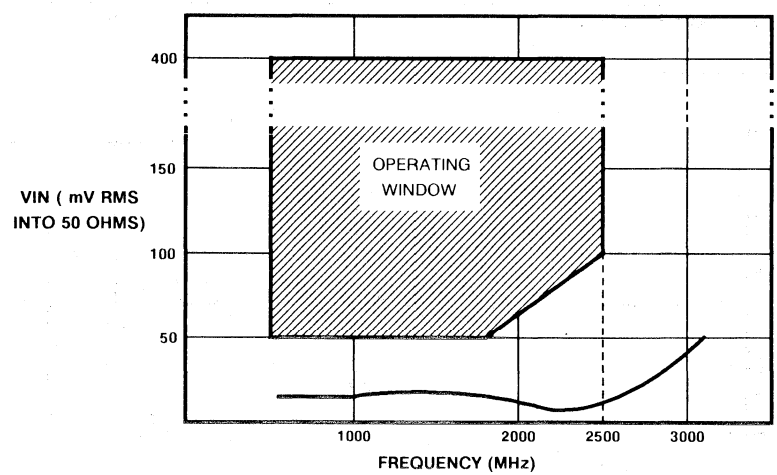


Fig.6. Typical input sensitivity

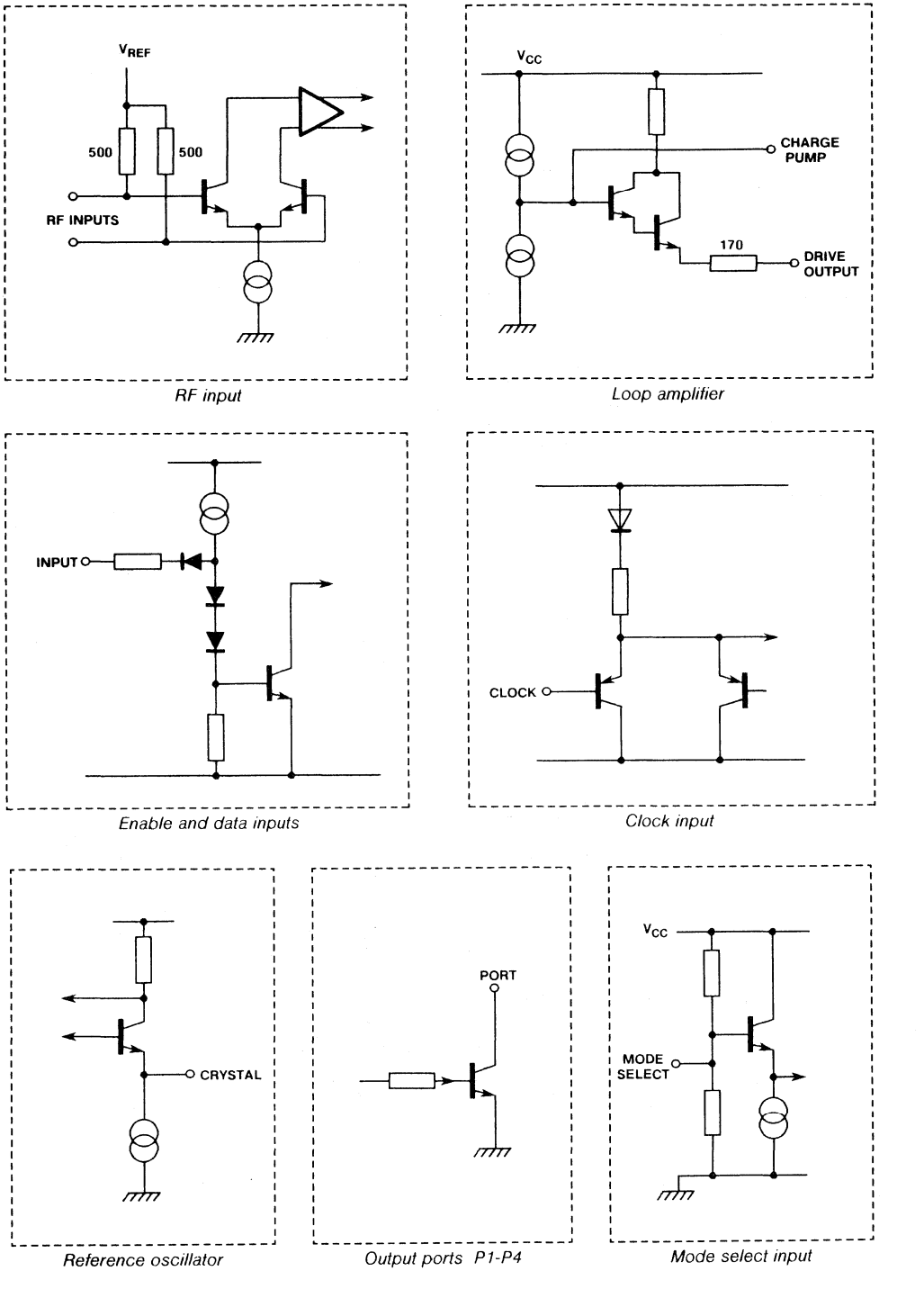


Fig.7 SP5054 Input/output interface circuits

SP5055

2.5 GHz BI-DIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

The SP5055 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 4 addressable current limited outputs and 4 addressable Bi-Directional open collector ports one of which is a 3 Bit ADC. The information on these ports can be read via the I²C BUS. The device has one fixed I²C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables 2 or more synthesisers to be used in a system.

The device is available in two variants: the SP5055 in 18-lead plastic DIL (DP18) and the SP5055S in 16-lead miniature plastic DIL (MP16). See Features below for functional differences between the devices.

FEATURES

- Complete 2.5GHz Single Chip System
- Programmable via I²C BUS
- Low power consumption (5V 65mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 8 Controllable Outputs, 4 Bi-Directional (SP5055)
- 6 Controllable Outputs, 4 Bi-Directional (SP5055S)
- 5 Level ADC
- Variable I²C BUS Address For Multi Tuner Applications
- Full ESD Protection *

* Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

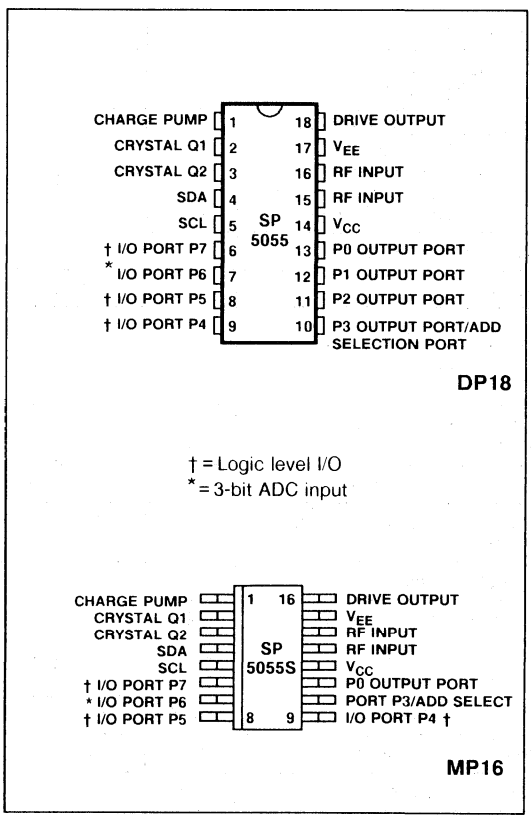


Fig.1 Pin connections - top view

ORDERING INFORMATION

SP5055 DP - (18 lead Plastic package)
SP5055S MP - (16 lead Miniature Plastic package)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = -10°C to 80°C, V_{CC} = +4.75V TO 5.25V

All pin connections refer to DP package.

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	14		65	80	mA	V_{CC} = 5V
Prescaler Input Voltage	15,16	50		300	mV_{RMS}	500MHz to 1.8GHz
Prescaler Input Voltage	15,16	100		300	mV_{RMS}	2.5GHz, see Fig. 5
Prescaler Input Impedance Input Capacitance	15,16		50 2		Ω pF	
SDA,SCL Input High Voltage Input Low Voltage Input High Current Input Low Current Leakage Current	4,5 4,5 4,5 4,5 4,5	3 0		5.5 1.5 10 -10 10	V V μA μA μA	 Input Voltage = V_{CC} Input Voltage = 0V When V_{CC} = 0V
SDA Output Voltage	4			0.4	V	I_{sink} = 3mA
Charge Pump Current Low	1		±50		μA	Byte 4 Bit 2 = 0, Pin 1 = 2V
Charge Pump Current High	1		±170		μA	Byte 4 Bit 2 = 1, Pin 1 = 2V
Charge Pump Output Leakage Current	1			±5	nA	Byte 4 Bit 4 = 1, Pin 1 = 2V
Charge Pump Drive Output Current	18	500			μA	$V_{pin\ 18}$ = 0.7V
Charge Pump Amplifier Gain			6400			
Recommended Crystal Series Resistance		10		200	Ω	
Crystal Oscillator Drive Level			40		mVp-p	
Crystal Oscillator Source Impedance	2		-400		Ω	Nominal Spread ± 15%
Output Ports						
P0-P3 Sink Current*	13-10	0.7	1	1.5	mA	V_{OUT} = 12V
P0-P3 Leakage Current*	13-10			10	μA	V_{OUT} = 13.2V
P4-P7 Sink Current	9-6	10			mA	V_{OUT} = 0.7V
P4-P7 Leakage Current	9-6			10	μA	V_{OUT} = 13.2V
Input Ports						
P3 Input Current High	10			+10	μA	V_{pin10} = 13.2V
P3 Input Current Low	10			-10	μA	V_{pin10} = 0V
P4,P5,P7 Input Voltage Low	9,8,6			0.8	V	
P4,P5,P7 Input Voltage High	9,8,6	2.7			V	
P6 Input Current High	7			+10	μA	See Table 3 for ADC Levels
P6 Input Current Low	7			-10	μA	

* Ports P1-P2 not present on the SP5055S.

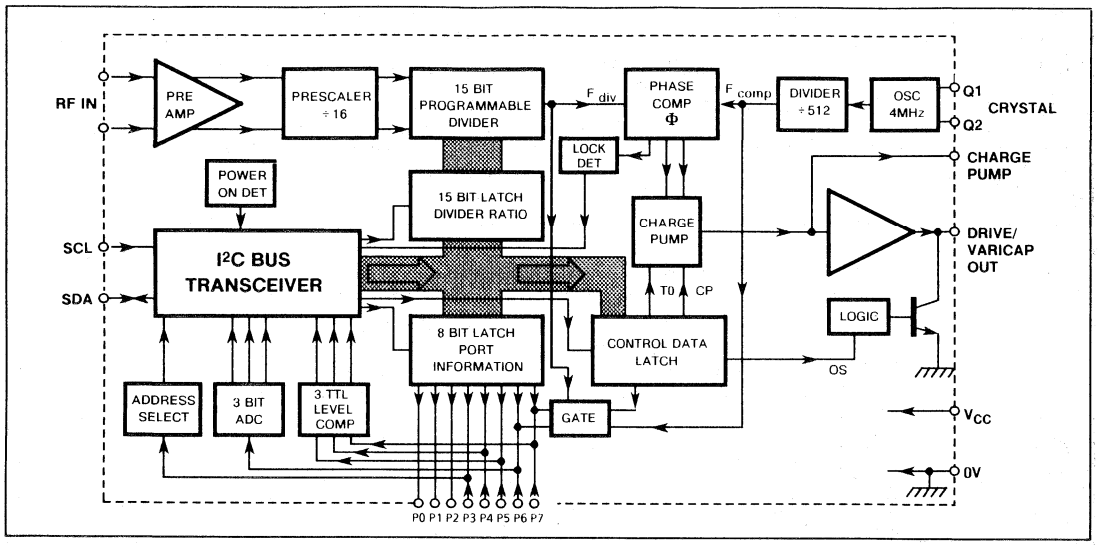


Fig.2 Block diagram of SP5055. (Ports P1-P2 not available on SP5055S)

FUNCTIONAL DESCRIPTION

The SP5055 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C BUS format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The last bit of the address byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5055 receives a correct address byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are programmed. When the SP5055 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode bytes 2 + 3 select the synthesised frequency while bytes 4 + 5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first bit of the next Byte determines whether that Byte is interpreted as byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (e.g. by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-16 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is shown in Fig 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 16 times the comparison frequency F_{comp}.

When frequency data is entered, the phase comparator, via the charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-board 4MHz crystal controlled oscillator.

Note - the comparison frequency is 7.8125KHz when a 4MHz reference is used.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for $\pm 170\mu A$ and a logic 0 for $\pm 50\mu A$ allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{comp} to P6 and F_{div} to P7.

Byte 5 programs the output ports P0 to P7; a logic 0 for a high impedance output and a logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power-on reset indicator and is set to a logic 1 if the power supply to the device has dropped below 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2,I1,I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5 level ADC.

The 5 level ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical Application is shown in Fig. 4. All input/ output interface circuits are shown in Fig. 6.

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	**BYTE 1**
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**BYTE 2**
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**BYTE 3**
CHARGE PUMP AND TEST BITS	1	CP	T1	T0	1	1	1	OS	A	**BYTE 4**
IO PORT CONTROL BITS	P7	P6	P5	P4	P3	P2*	P1*	P0	A	**BYTE 5**

Table 1 Write data format (MSB is transmitted first)

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	**BYTE 1**
STATUS BYTE	POR	FL	I2	I1	I0	A2	A1	A0	A	**BYTE 2**

Table 2 Read data format

A : Acknowledge Bit
MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select
T1 : Test mode selection
T0 : Charge pump disable
OS : Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P2*, P1*, P0 : control output states
POR : Power On Reset indicator
FL : Phase Lock detect Flag
I2, I1, I0 : Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0 : 5 Level ADC data from P6 (see Table 3)

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0.45V_{CC}$ to $0.6V_{CC}$
0	1	0	$0.3V_{CC}$ to $0.45\ V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.3\ V_{CC}$
0	0	0	0 to $0.15\ V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	$0 - 0.2\ V_{CC}$
0	1	ALWAYS VALID
1	0	$0.3 - 0.7\ V_{CC}$
1	1	$0.8\ V_{CC}$ - 13.2V

Table 4 Address selection

NOTE: * Don't care condition on SP5055S

Fig. 3 Data Formats

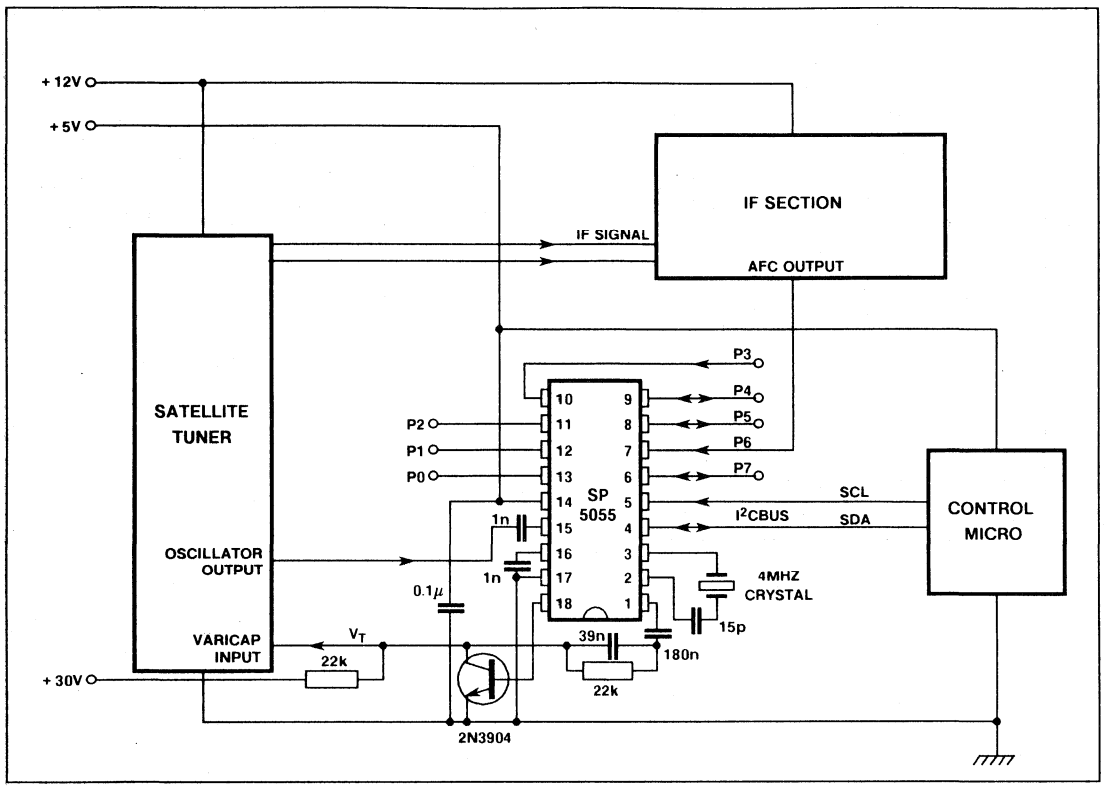


Fig.4 Typical SP5055 application

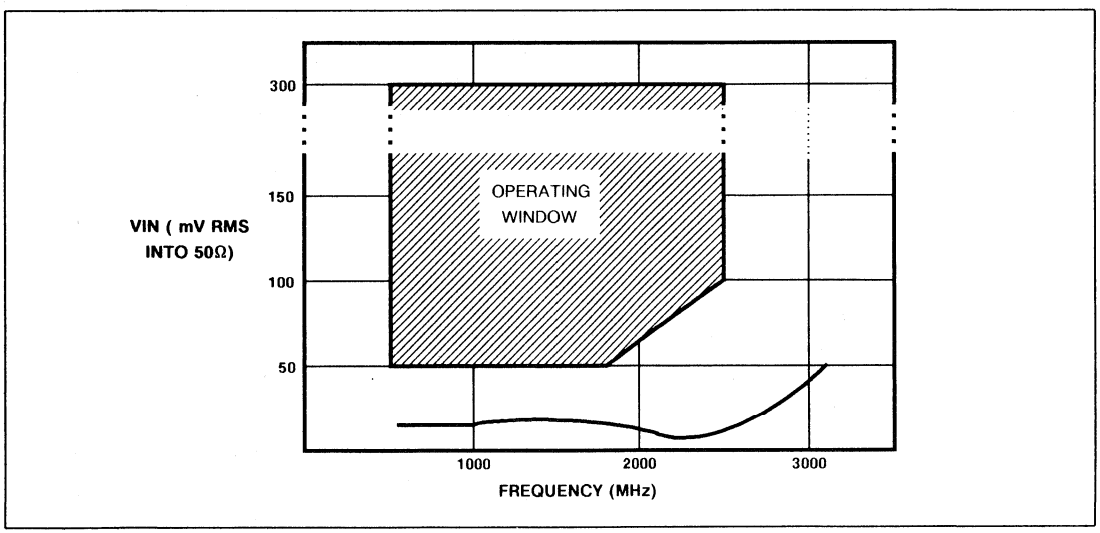
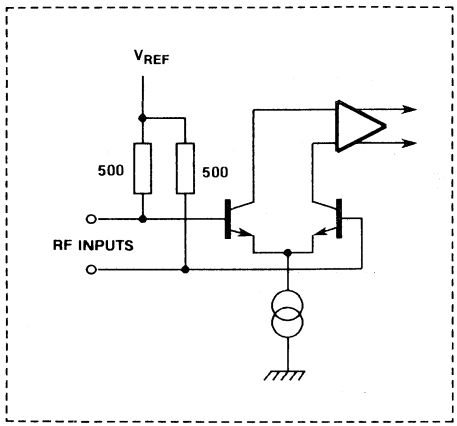
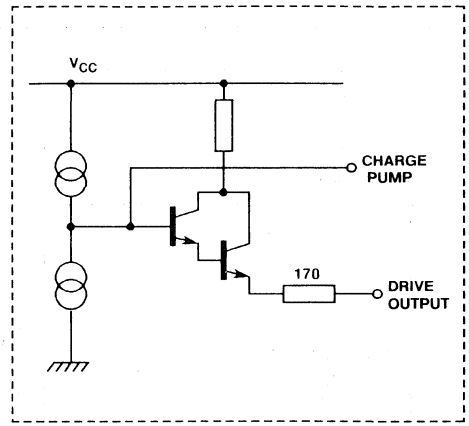


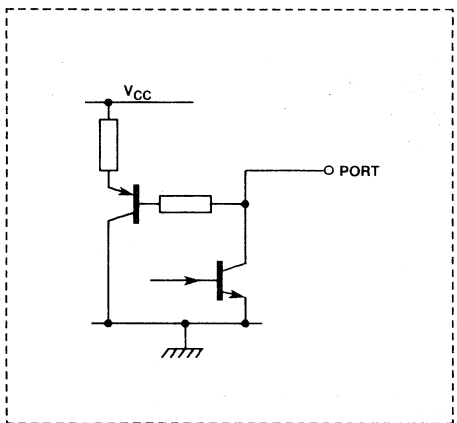
Fig.5 Typical input sensitivity



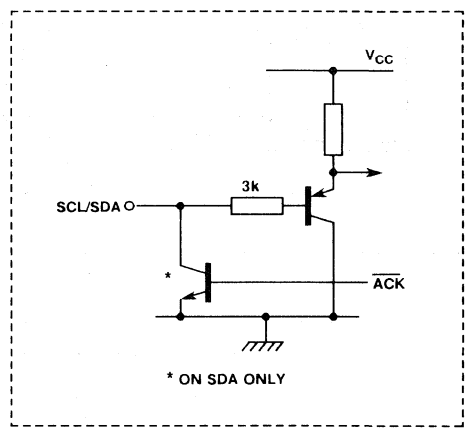
RF input



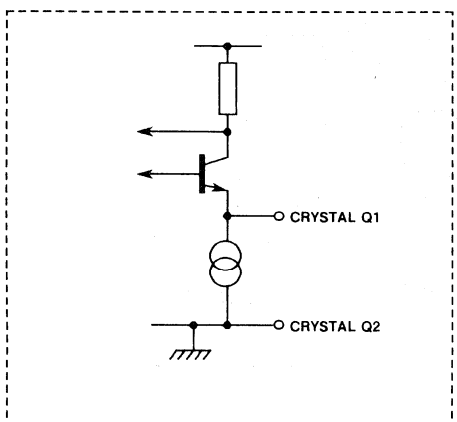
Loop amplifier



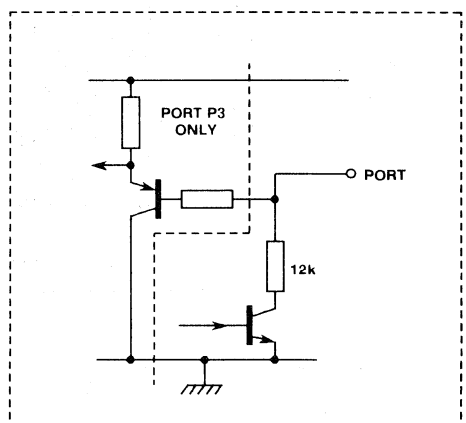
Ports P7 - P4



SCL and SDA input



Reference oscillator



Ports P0-P3 (SP5055), P0 and P3 only on SP5055S

Fig.6 SP5055 input/output interface circuits

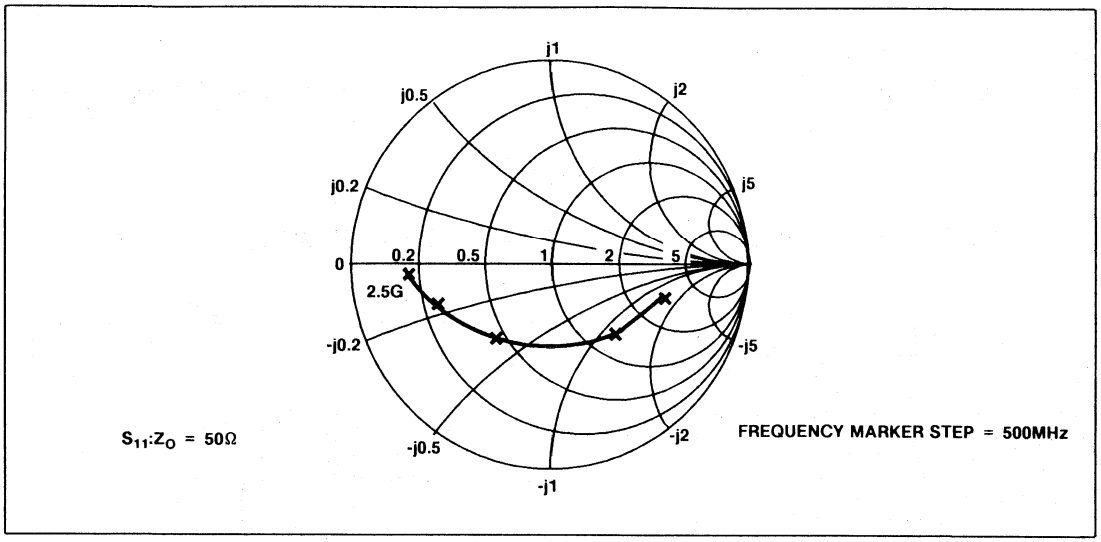


Fig.7 Typical input impedance

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V.

Parameter	Pin SP5055	Pin SP5055S	Value Min	Value Max	Units	Conditions
Supply voltage	14	12	-0.3	7	V	
RF input voltage	15, 16	13, 14		2.5	Vp-p	
Port voltage	6 - 13	6 - 11	-0.3	14	V	Port in off state
	6 - 9	6 - 9	-0.3	6	V	Port in on state
	10-13	10, 11	-0.3	14	V	Port in on state
Total port output current	6-13	6-11		50	mA	
RF input DC offset	15, 16	13, 14	-0.3	V_{CC} + 0.3	V	
Charge pump DC offset	1	1	-0.3	V_{CC} + 0.3	V	
Drive DC offset	18	16	-0.3	V_{CC} + 0.3	V	
Crystal oscillator DC offset	2	2	-0.3	V_{CC} + 0.3	V	
SDA, SCL input voltage	4, 5	4, 5	-0.3	V_{CC} + 0.3	V	With V_{CC} applied
			-0.3	5.5	V	V_{CC} not applied
Storage temperature			-55	+ 125	°C	
Junction temperature				+ 150	°C	
DP18 thermal resistance, chip-to-ambient				78	°C/W	
DP18 thermal resistance, chip-to-case				24	°C/W	
MP16 thermal resistance, chip-to-ambient				111	°C/W	
MP16 thermal resistance, chip-to-case				41	°C/W	
Power consumption at 5.5V				440	mW	All ports off

PRELIMINARY INFORMATION

2449-1.0

SP5056

2.5 GHz BI-DIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

The SP5056 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 3 addressable current limited outputs and 4 addressable Bi-Directional open-collector ports one of which is a 3-Bit ADC. The information on these ports can be read via the I²C BUS. The device has 4 programmable I²C BUS addresses, which enables 2 or more synthesisers to be used in a system.

The device is available in two variants: the SP5056 in 18-lead plastic DIL (DP18) and the SP5056S in 16-lead miniature plastic DIL (MP16). See Features below for functional differences between the devices.

FEATURES

- Complete 2.5GHz Single Chip System
- Programmable via I²C BUS
- Low power consumption (5V 65mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 7 Controllable Outputs, 4 Bi-Directional (SP5056)
- 4 Bi-Directional Controllable Outputs (SP5056S)
- 5 Level ADC
- Variable I²C BUS Address For Multi Tuner Applications
- Full ESD Protection *

* Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

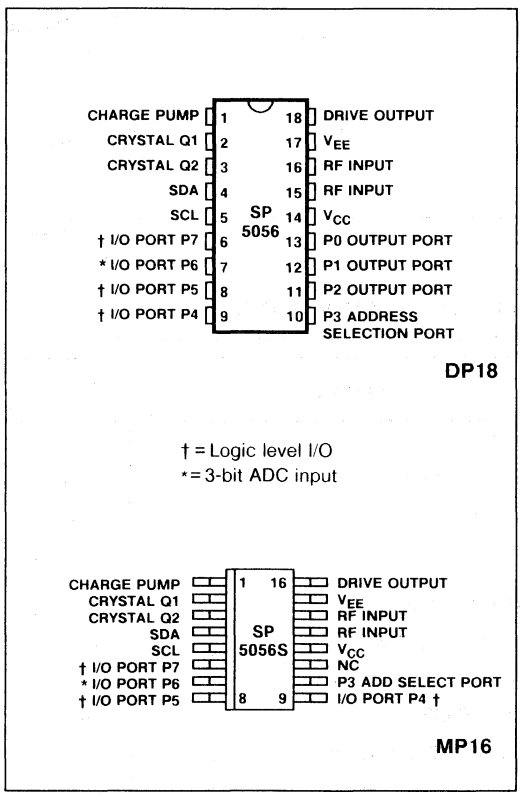


Fig.1 Pin connections - top view

ORDERING INFORMATION

SP5056 DP - (18 lead Plastic package)
SP5056S MP- (16 lead Miniature Plastic package)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = -10°C to 80°C, V_{CC} = +4.75V TO 5.25V
All pin connections refer to DP package.
These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	14		65	80	mA	V_{CC} = 5V
Prescaler Input Voltage	15,16	50		300	mV_{RMS}	500MHz to 1.8GHz
Prescaler Input Voltage	15,16	100		300	mV_{RMS}	2.5GHz, see Fig. 5
Prescaler Input Impedance Input Capacitance	15,16		50 2		Ω pF	
SDA,SCL Input High Voltage Input Low Voltage Input High Current Input Low Current Leakage Current	4,5 4,5 4,5 4,5 4,5	3 0		5.5 1.5 10 -10 10	V V µA µA µA	 Input Voltage = V_{CC} Input Voltage = 0V When V_{CC} = 0V
SDA Output Voltage	4			0.4	V	I_{sink} = 3mA
Charge Pump Current Low	1		±50		µA	Byte 4 Bit 2 = 0, Pin 1 = 2V
Charge Pump Current High	1		±170		µA	Byte 4 Bit 2 = 1, Pin 1 = 2V
Charge Pump Output Leakage Current	1			±5	nA	Byte 4 Bit 4 = 1, Pin 1 = 2V
Charge Pump Drive Output Current	18	500			µA	$V_{pin\ 18}$ = 0.7V
Charge Pump Amplifier Gain			6400			
Recommended Crystal Series Resistance		10		200	Ω	
Crystal Oscillator Drive Level			40		mVp-p	
Crystal Oscillator Source Impedance	2		-400		Ω	Nominal Spread ± 15%
Output Ports						
P0-P2 Sink Current*	11-13	0.7	1	1.5	mA	V_{OUT} = 12V
P0-P2 Leakage Current*	11-13			10	µA	V_{OUT} = 13.2V
P4-P7 Sink Current	9-6	10			mA	V_{OUT} = 0.7V
P4-P7 Leakage Current	9-6			10	µA	V_{OUT} = 13.2V
Input Ports						
P3 Input Current High	10			1	mA	V_{pin10} = V_{CC}
P3 Input Current Low	10			0.5	mA	V_{pin10} = 0V
P4,P5,P7 Input Voltage Low	9,8,6			0.8	V	
P4,P5,P7 Input Voltage High	9,8,6	2.7			V	
P6 Input Current High	7			+10	µA	See Table 3 for ADC Levels
P6 Input Current Low	7			-10	µA	

* Ports P0-P2 not present on the SP5056S.

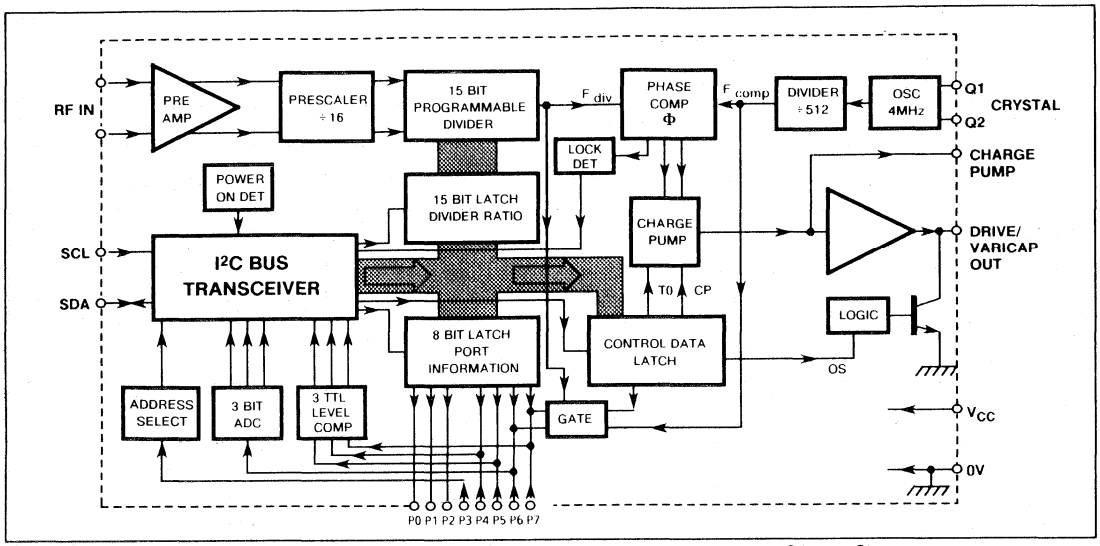


Fig.2 Block diagram of SP5056. (Ports P0-P2 not available on SP5056S)

FUNCTIONAL DESCRIPTION

The SP5056 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C BUS format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The last bit of the address byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5056 receives a correct address byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are programmed. When the SP5056 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode bytes 2 + 3 select the synthesised frequency while bytes 4 + 5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first bit of the next Byte determines whether that Byte is interpreted as byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid byte (i.e. by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-16 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is shown in Fig 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 16 times the comparison frequency F_{comp}.

When frequency data is entered, the phase comparator, via the charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-board 4MHz crystal controlled oscillator.

Note - the comparison frequency is 7.8125kHz when a 4MHz reference is used.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for $\pm 170\mu A$ and a logic 0 for $\pm 50\mu A$ allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{comp} to P6 and F_{div} to P7

Byte 5 programs the output ports P0 to P2 and P4 to P7, a logic 0 for a high impedance output and a logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power-on reset indicator and is set to a logic 1 if the power supply to the device has dropped below 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2,I1,I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5 level ADC.

The 5 level ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical Application is shown in Fig. 4. All input/ output interface circuits are shown in Fig. 6.

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	**BYTE 1**
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**BYTE 2**
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**BYTE 3**
CHARGE PUMP AND TEST BITS	1	CP	T1	T0	1	1	1	OS	A	**BYTE 4**
IO PORT CONTROL BITS	P7	P6	P5	P4	X	P2*	P1*	P0*	A	**BYTE 5**

Table 1 Write data format (MSB is transmitted first)

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	**BYTE 1**
STATUS BYTE	POR	FL	I2	I1	I0	A2	A1	A0	A	**BYTE 2**

Table 2 Read data format

A : Acknowledge Bit
MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select
T1 : Test mode selection
T0 : Charge pump disable
OS : Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P2*, P1*, P0* : control output states
POR : Power On Reset indicator
FL : Phase Lock detect Flag
I2, I1, I0 : Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0 : 5 Level ADC data from P6 (see Table 3)

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0.45V_{CC}$ to $0.6V_{CC}$
0	1	0	$0.3V_{CC}$ to $0.45\ V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.3\ V_{CC}$
0	0	0	0 to $0.15\ V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	$0 - 0.1\ V_{CC}$
0	1	OPEN CIRCUIT
1	0	$0.4 - 0.6\ V_{CC}$†
1	1	$0.9\ V_{CC} - V_{CC}$

Table 4 Address selection

NOTES: † Programmed by connecting a 15kΩ resistor between Address Select Port P3 and V_{CC}
* Don't care condition on SP5056S.

Fig. 3 Data Formats

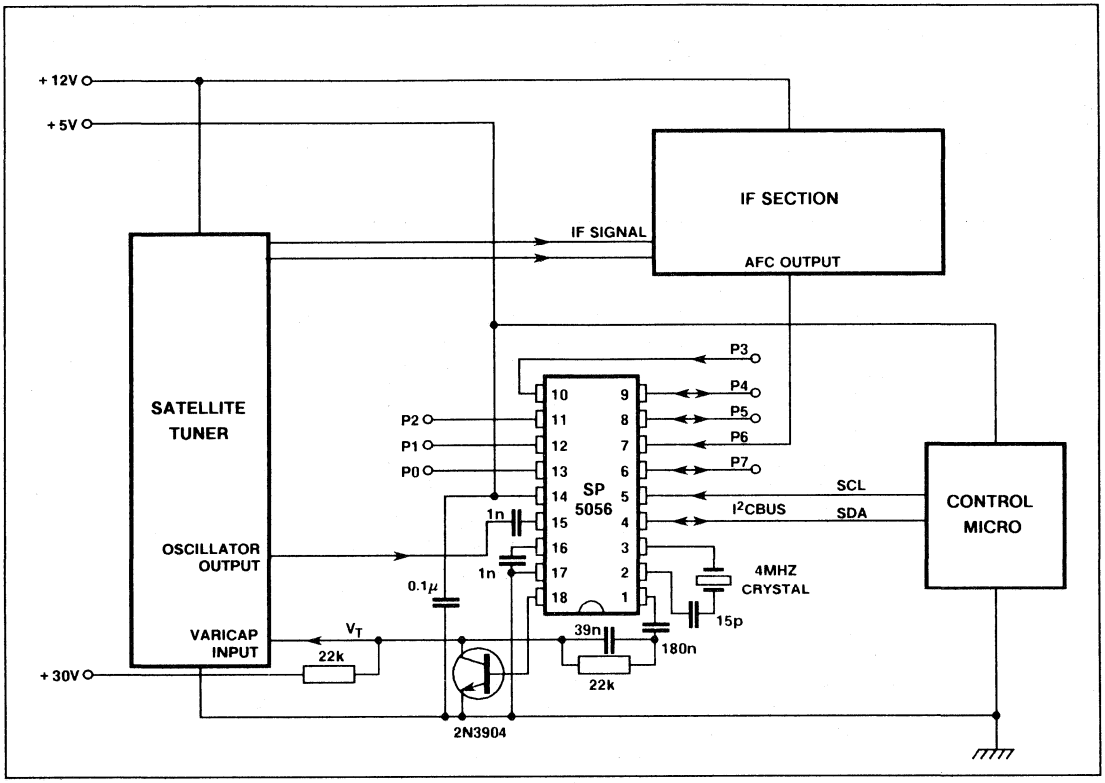


Fig.4 Typical SP5056 application

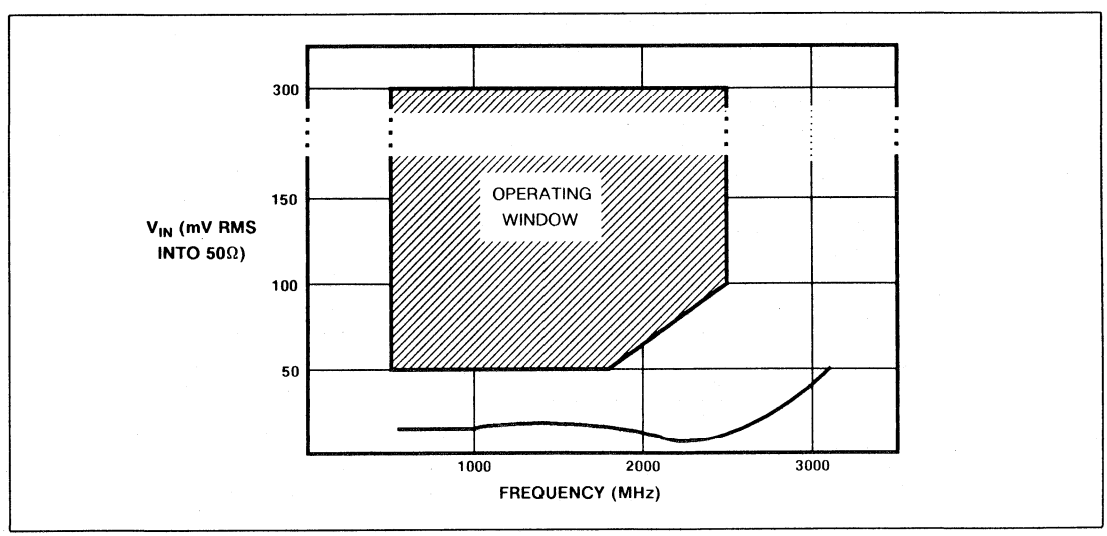
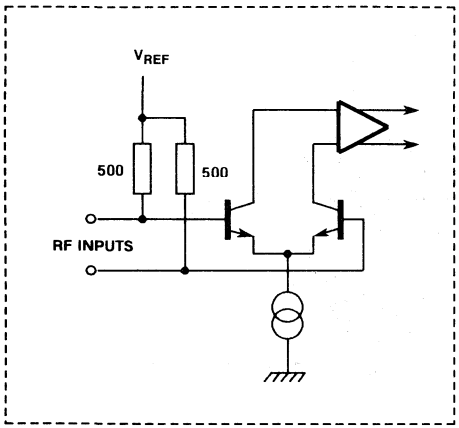
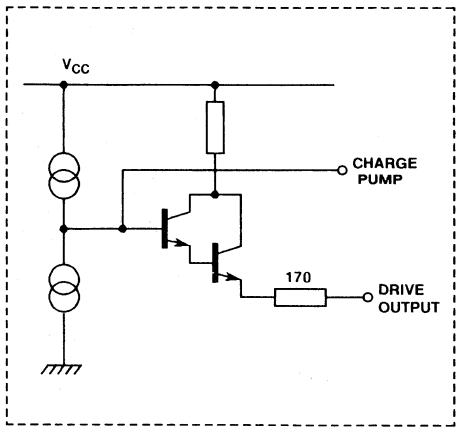


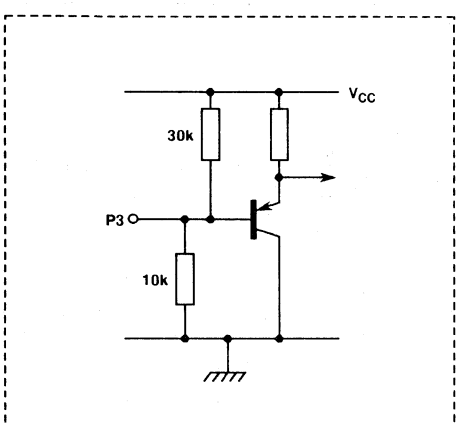
Fig.5 Typical input sensitivity



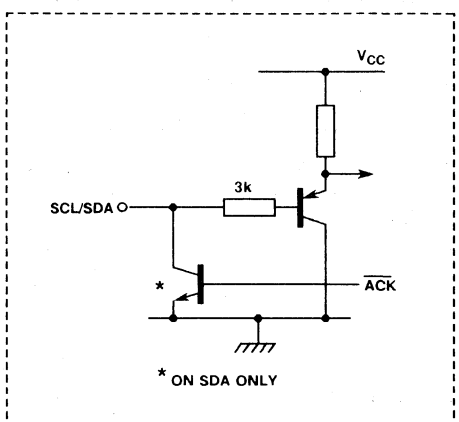
RF input



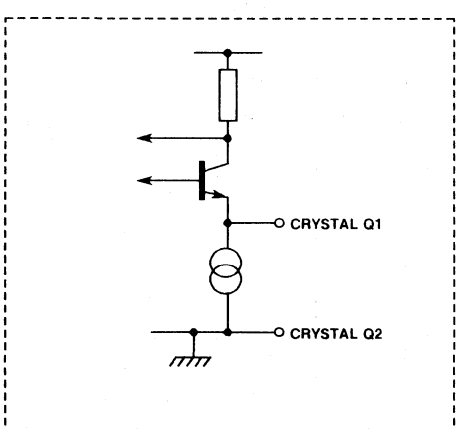
Loop amplifier



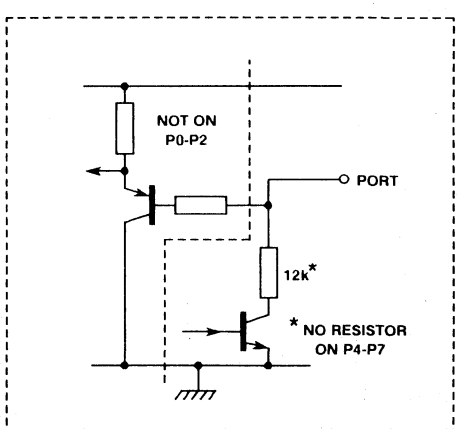
Address programming input



SCL and SDA input



Reference oscillator



Ports P0-P2 (SP5056 only) and P4-P7

Fig.6 SP5056 input/output interface circuits

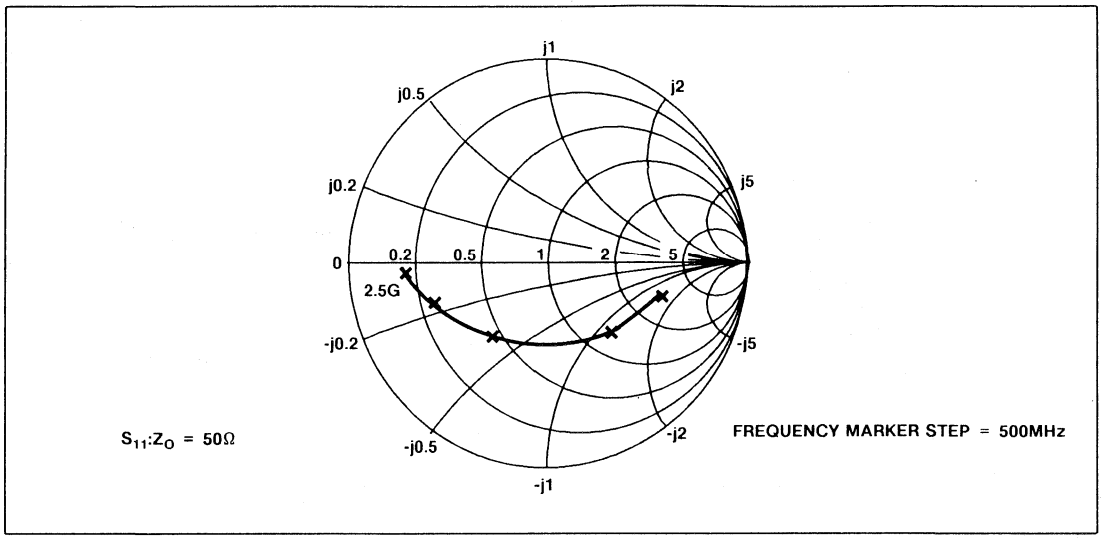


Fig.7 Typical input impedance

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V.

Parameter	Pin SP5056	Pin SP5056S	Value Min	Value Max	Units	Conditions
Supply voltage	14	12	-0.3	7	V	
RF input voltage	15, 16	13, 14		2.5	Vp-p	
Port voltage	6-9,11-13	6 - 9	-0.3	14	V	Port in off state
	6 - 9	6 - 9	-0.3	6	V	Port in on state
	11-13	-	-0.3	14	V	Port in on state
	10	10	-0.3	V_{CC} + 0.3	V	
Total port output current	6-9, 11-13	6-9		50	mA	
RF input DC offset	15, 16	13, 14	-0.3	V_{CC} + 0.3	V	
Charge pump DC offset	1	1	-0.3	V_{CC} + 0.3	V	
Drive DC offset	18	16	-0.3	V_{CC} + 0.3	V	
Crystal oscillator DC offset	2	2	-0.3	V_{CC} + 0.3	V	
SDA, SCL input voltage	4, 5	4, 5	-0.3	V_{CC} + 0.3	V	With V_{CC} applied
			-0.3	5.5	V	V_{CC} not applied
Storage temperature			-55	+ 125	°C	
Junction temperature				+ 150	°C	
DP18 thermal resistance, chip-to-ambient				78	°C/W	
DP18 thermal resistance, chip-to-case				24	°C/W	
MP16 thermal resistance, chip-to-ambient				111	°C/W	
MP16 thermal resistance, chip-to-case				41	°C/W	
Power consumption at 5.5V				440	mW	All ports off

3065-1.0

SP5060

2.0GHz FIXED MODULUS FREQUENCY SYNTHESISER

The SP5060 is for use in outdoor (head end) units of satellite TV receivers and together with an appropriate voltage controlled oscillator (VCO), forms a complete phase locked loop (PLL) synthesiser. The circuit consists of a prescaler with preamplifier and a fixed modulus divider. The phase comparator is fed with a reference frequency derived from an external oscillator or crystal. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

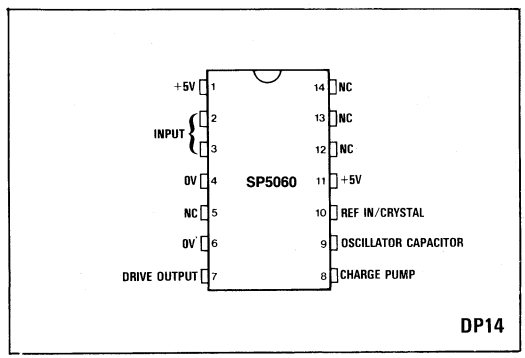


Fig.1 Pin connections - top view

FEATURES

- +5V, 50mA Supply
- Prescaler and Preamplifier Included
- High Comparator Frequency for Easier Filtering
- Charge Pump Amplifier with Feedback Point
- Synthesises Frequencies up to 2.0GHz
- For use at C-Band with Frequency Doubling Mixer

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**-10°C to +70°C**
Maximum junction temperature	175°C
Storage temperature	-55°C to +125°C
Supply voltage Pin 1 and Pin 11	7V
Prescaler input voltage	2.5V p-p

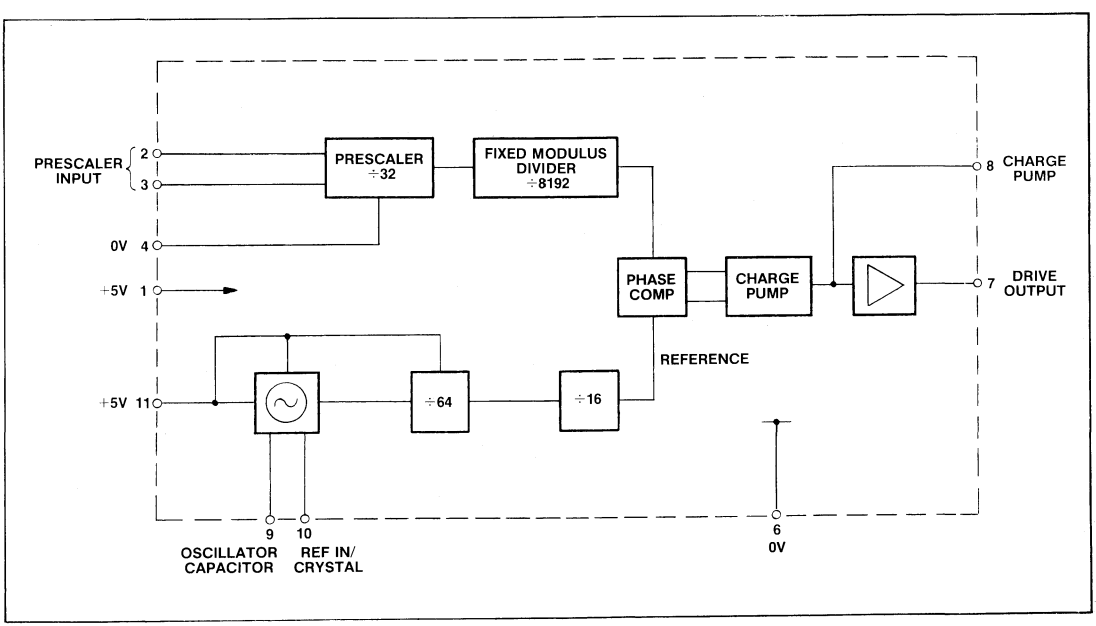


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C V_{CC} = +4.5V to 5.5V

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Operating voltage	V_{CC}	1,11	4.5		5.5	V	
Supply current	$I_{CC}(1)$	1		50	60	mA	
Supply current	$I_{CC}(11)$	11		1		mA	
Prescaler input voltage		2,3	100			mV	300MHz to 2.0GHz sinewave
Prescaler input impedance		2,3		50		Ohms	
Charge pump output current		8	±75	±100	±125	μA	V pin 8 = 2.0V
Charge pump leakage current		8			±1	μA	V pin 8 = 2.0V
Charge pump drive output current		7	1			mA	V pin 7 = 0.7V
Drift due to leakage				5		mV/s	At collector of external varicap drive transistor
Oscillator temperature stability		9,10		0.12		PPM/°C	Over 0 to 65°C temperature range IC variation only
Oscillator stability with supply voltage		9,10		0.25		PPM/V	V_{CC} = 4.5V to 5.5V
Reference clock frequency		10	2		8.0	MHz	
External reference amplitude		10	100		500	mV rms	
Reference input impedance		10		25		kohms	

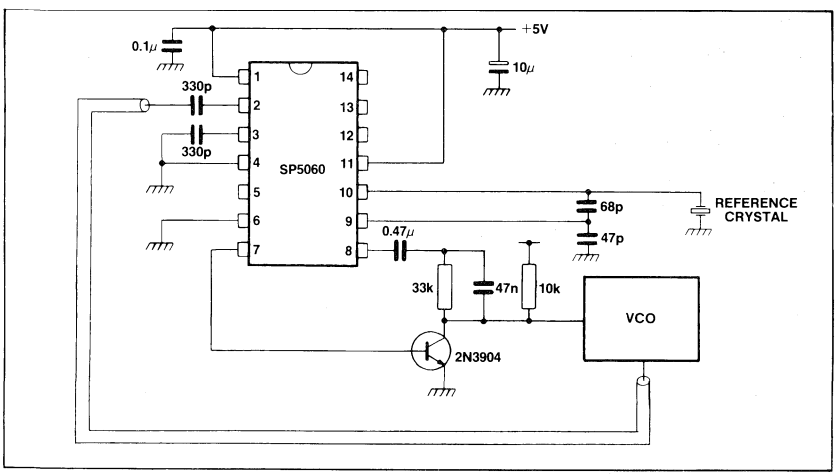


Fig.3 Typical application and test circuit (1024MHz with 4MHz reference crystal)

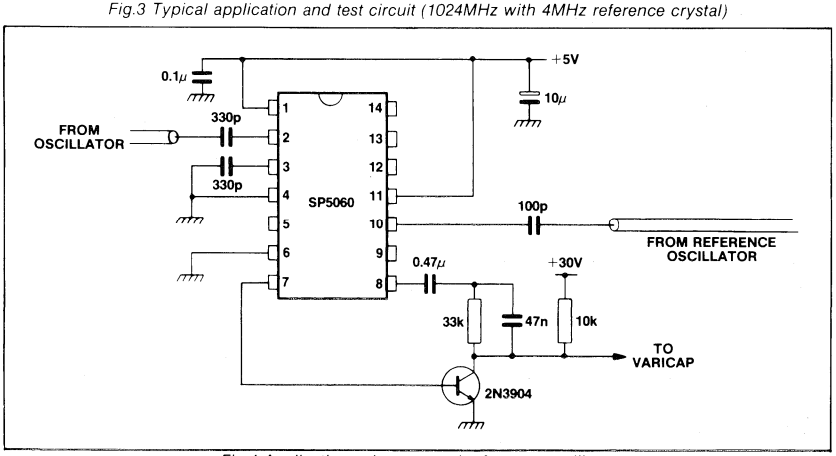


Fig.4 Application using external reference oscillator

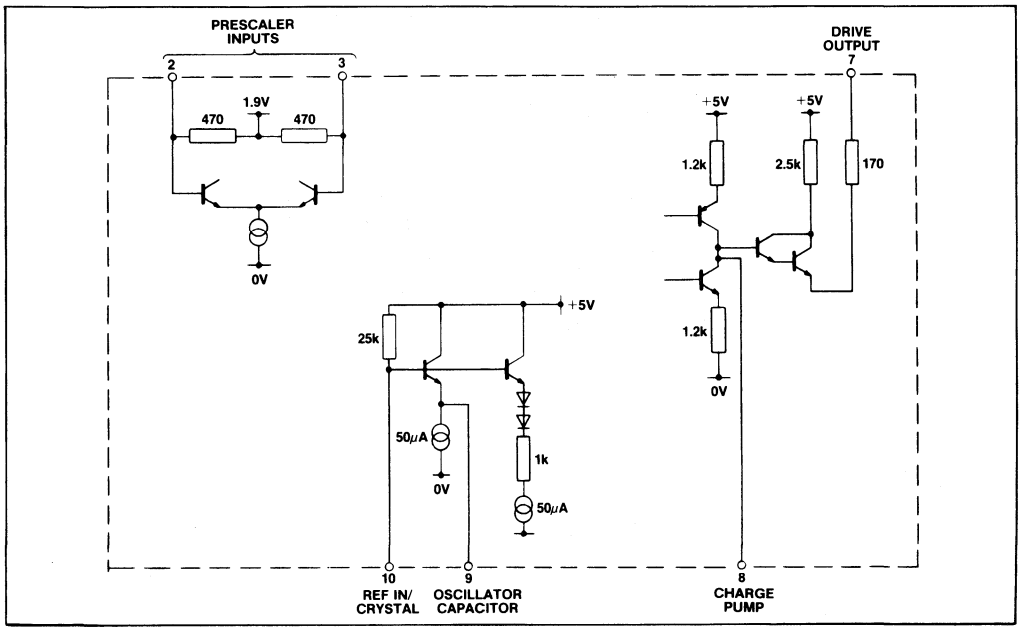


Fig.5 SP5060 input/output interface circuits

DESCRIPTION

The SP5060, when used with a voltage controlled oscillator, forms a complete phase locked loop frequency synthesiser.

The phase comparator reference frequency is obtained by dividing the reference frequency. This may be generated on chip, by means of a crystal, or from an external reference oscillator.

The output of the prescaler is divided by the fixed modulus divider, producing an output frequency which is phase locked to the reference frequency.

The divider stages are arranged to give a fixed ratio, between the synthesised frequency and the reference, of 256:1.

Any frequency within the range 300MHz to 2.0GHz may be achieved using the appropriate reference or crystal frequency.

A single external transistor, driven from the charge pump output, provides the output swing necessary for the oscillator varicap line.

To improve device stability the +5V and ground supplies to the chip are split and brought out to separate pins. It is therefore essential to connect all the supply pins for the device to operate correctly.

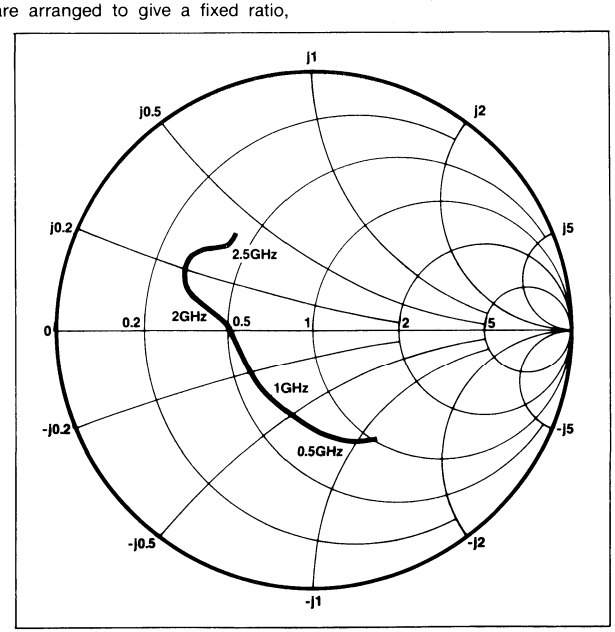


Fig.6 Typical input impedance Normalised to 50Ω

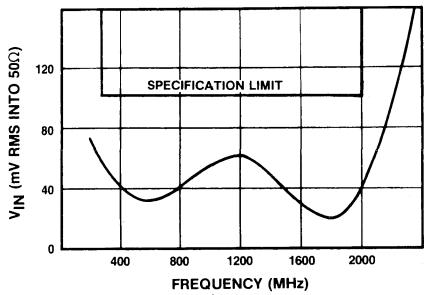


Fig.7 SP5060 typical input sensitivity

SP5070

2.4GHz FIXED MODULUS FREQUENCY SYNTHESISER

The SP5070 is a single modulus frequency synthesiser for use in satellite TV receivers and together with an appropriate voltage controlled oscillator (VCO), forms a complete phase locked loop (PLL) synthesiser. The circuit consists of a prescaler with preamplifier and a fixed modulus divider. The phase comparator is fed with a reference frequency derived from an external oscillator or crystal. The comparator has a charge pump output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

FEATURES

- Low Power Consumption (5V, 42mA)
- Prescaler and Preamplifier Included
- Charge Pump Amplifier with Feedback Point
- Charge Pump Disable Facility
- Synthesises Frequencies up to 2.4GHz
- Pin and Function Compatible with SP5060 and SP5062.
- Full ESD Protection *

* Normal ESD handling procedures should be observed

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems
- C-Band with Frequency Doubling Mixer

ORDERING INFORMATION

SP5070 DP - (14 lead Plastic Package)
SP5070F MP - (14 lead Miniature Plastic Package)

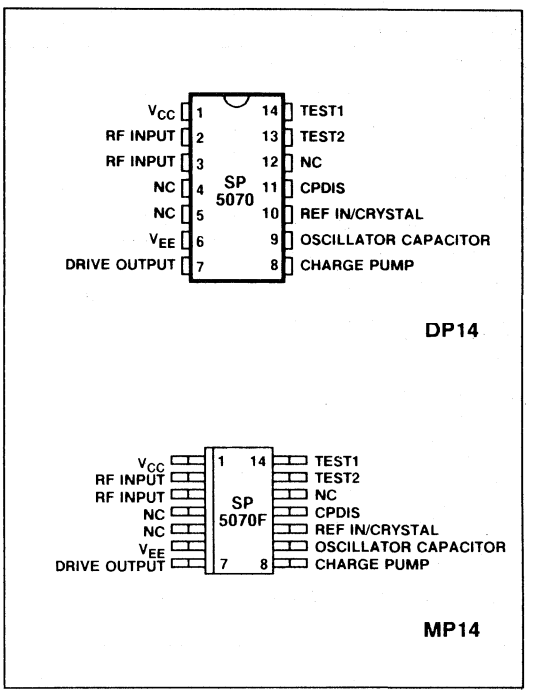


Fig.1 Pin connections - top view

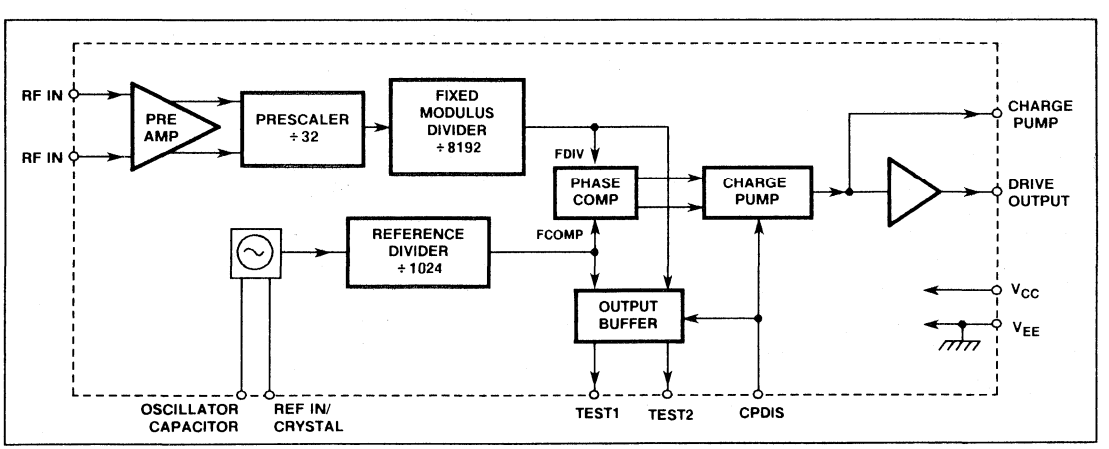


Fig.2 Block diagram of SP5070

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

T_{amb} = -40°C to +85°C, V_{CC} = +4.5V to +5.5V

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	1		42	50	mA	V_{CC} = 5V
Prescaler input voltage		2,3	50		300	mV_{RMS}	300MHz to 1.8GHz sinewave
Prescaler input voltage		2,3	100		300	mV_{RMS}	2.4GHz, see Fig. 5
Prescaler input impedance Input capacitance		2,3 2,3		50 2		Ω pF	
Charge pump output current		8		±100		µA	V pin 8 = 2.0V
Charge pump output leakage		8			±5	nA	V pin 8 = 2.0V
Drift due to leakage					5	mV/s	At Collector of External Varicap Drive Transistor
Charge pump drive output current		7	1			mA	V pin 7 = 0.7V
Charge pump amplifier gain				6400			Pin 7 Current 100µA
Oscillator temperature stability		9,10			2	ppm/°C	
Oscillator stability with supply voltage		9,10			2	ppm/V	
Reference clock frequency		10	2		10	MHz	
External reference amplitude		10	100		500	mV_{RMS}	
Charge pump disable/TEST1 and TEST2 enable Charge pump disable leakage current		11 11	-250		-500 10	µA µA	V_{IN} < 0V V pin 11 = V_{CC}
TEST1/TEST2 sink current		13, 14	1			mA	V_{OUT} = 0.7V
TEST1/TEST2 leakage current		13, 14			10	µA	V_{OUT} = V_{CC} + 0.3V
TEST1/TEST2 Voltage		13, 14			V_{CC} + 0.3	V	

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} = 0V.

Parameter	Pin	Value		Units
		Min	Max	
Supply voltage	1	-0.3	7	V
RF input voltage	2, 3		2.5	Vp-p
RF input DC offset	2, 3	-0.3	V_{CC} + 0.3	V
Charge pump DC offset Charge pump disable	8 11	-0.3 -0.7	V_{CC} + 0.3 V_{CC} + 0.3	V V
Drive DC offset	7	-0.3	V_{CC} + 0.3	V
Crystal oscillator DC offset	9, 10	-0.3	V_{CC} + 0.3	V
TEST outputs	13, 14	-0.3	V_{CC} + 0.3	V
Storage temperature		-55	+125	°C
Junction temperature			+150	°C
DP14 thermal resistance, chip-to-ambient DP14 thermal resistance, chip-to-case			78 30	°C/W °C/W
MP14 thermal resistance, chip-to-ambient MP14 thermal resistance, chip-to-case			123 45	°C/W °C/W
Power consumption at 5.5V			275	mW

FUNCTIONAL DESCRIPTION

The SP5070, when used with a voltage controlled oscillator, forms a complete phase locked loop frequency synthesiser.

The phase comparator comparison frequency is obtained by dividing the reference frequency. This may be generated on-chip by means of an external crystal, or from an external reference oscillator.

The output of the prescaler is divided by the fixed modulus divider, producing an output frequency which is phase locked to the comparison frequency

The divider stages are arranged to give a fixed ratio between the synthesised frequency and the reference of 256:1. Any frequency within the range of 300MHz to 2.4GHz may be achieved by using the appropriate reference or crystal frequency.

A single external transistor, driven from the charge pump output, provides the output drive necessary for the oscillator varicap line.

A test facility which disables the charge pump is also provided. This is activated when a negative voltage is applied to pin 11, see electrical characteristics above. When the device is in this mode, F_{COMP} and F_{DIV} are also available at outputs TEST1 and TEST2 respectively. These are open collector outputs and are each capable of sinking a minimum of 1mA. In normal mode of operation these outputs are high impedance.

For compatibility with SP5060/SP5062, pin 11 may be connected to V_{CC}.

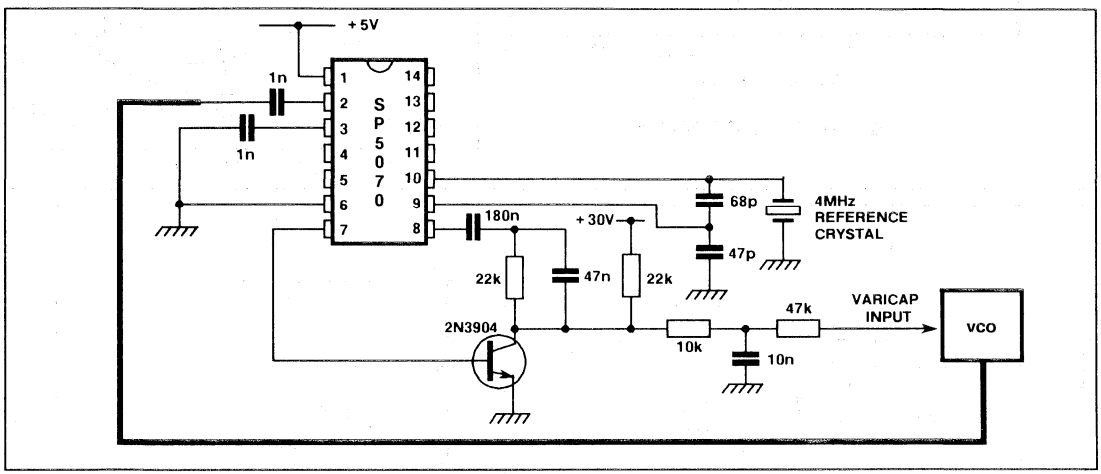


Fig.3. Typical application and test circuit (1024MHz with 4MHz reference crystal)

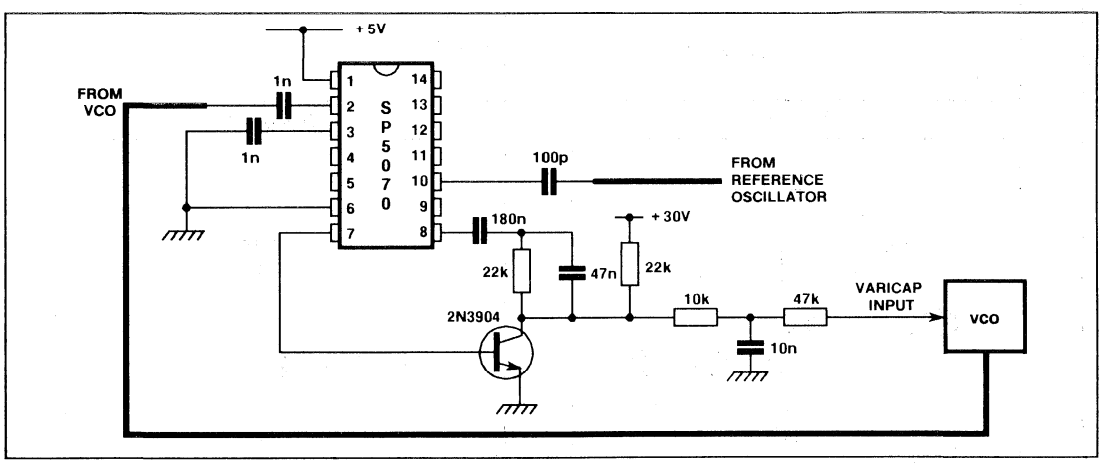


Fig.4. Application using external reference oscillator

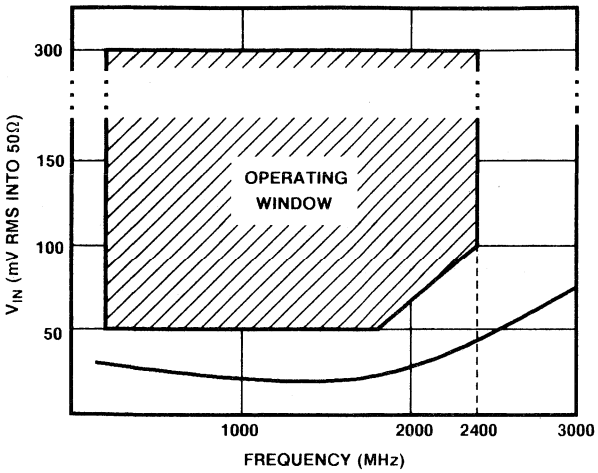


Fig.5. Typical input sensitivity

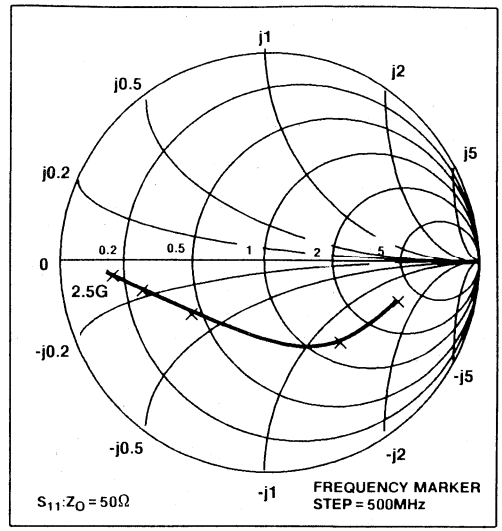


Fig.6 Typical input impedance

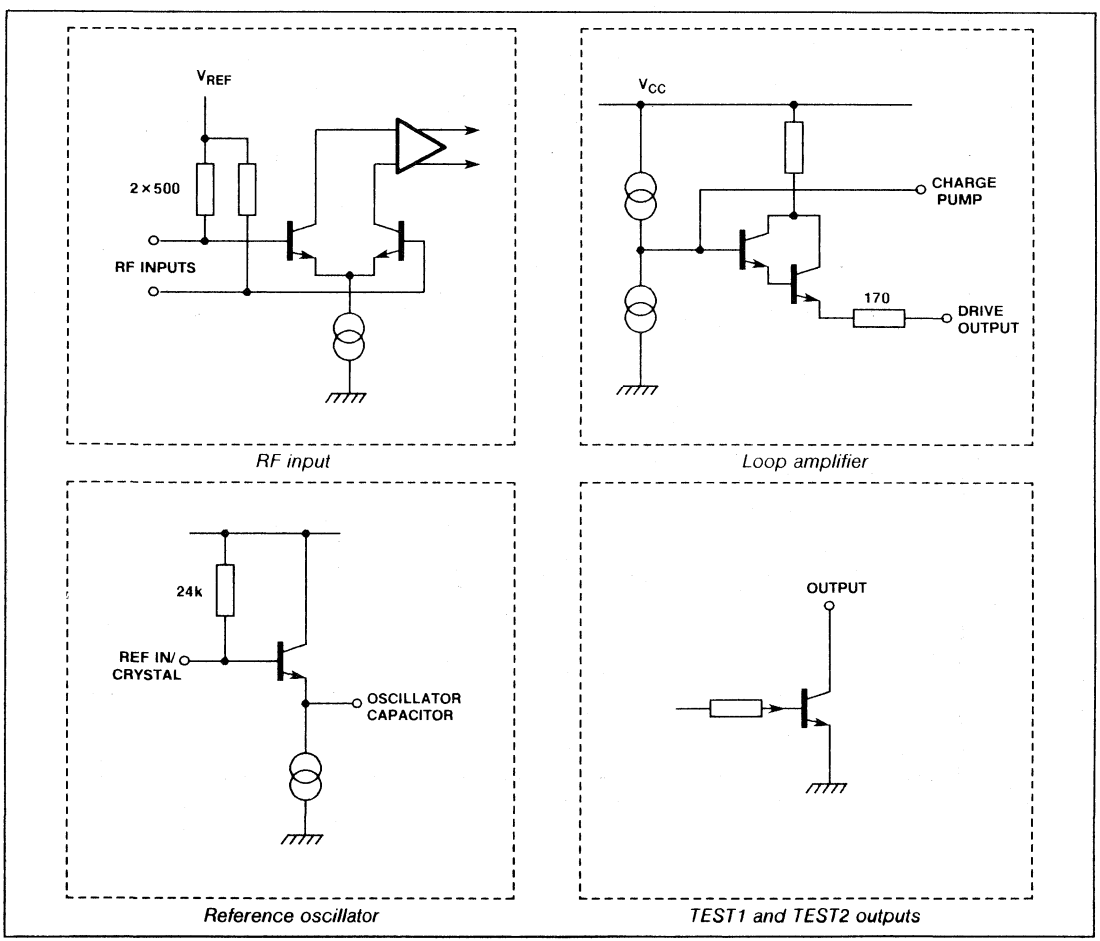


Fig.7 SP5070 Input/output interface circuits

SP5502

1.3GHz I²C BUS 4-ADDRESS SYNTHESISER

The SP5502 is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The SP5502 has 4 programmable I²C BUS addresses, which enables 2 or more synthesisers to be used in a system.

The device is available in three variants: the SP5502 in 14-lead plastic DIL, the SP5502F in 14-lead miniature plastic DIL and the SP5502S in 16-lead miniature plastic DIL. See Features below for functional differences between the devices.

FEATURES

- Complete 1.3GHz Single Chip System
- Programmable via I²C BUS
- Low Power Consumption (250mW)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 5 x 20mA Controllable Outputs (SP5502S)
- 3 x 20mA Controllable Outputs (SP5502, SP5502F)
- Variable I²C BUS Address For Multi Tuner Applications
- Full ESD Protection*

* Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV when Combined with SP4902 2.5GHz Prescaler
- Cable Tuning Systems
- VCRs

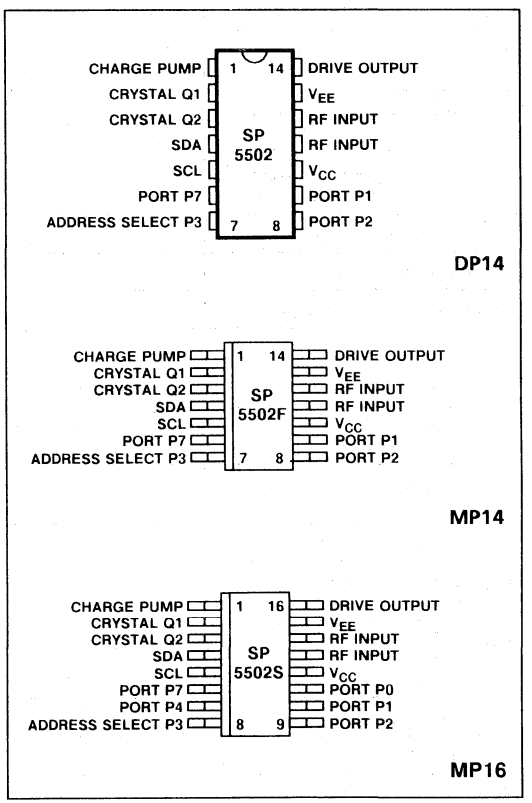


Fig.1 Pin connections - top view

ORDERING INFORMATION

SP5502 DP (14 lead Plastic package)
SP5502F MP (14 lead Miniature Plastic Package)
SP5502S MP (16 lead Miniature Plastic Package)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = −10°C, to + 80°C V_{CC} = + 4.5V to 5.5V. All pin references are to the SP5502S (MP16 package)

These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	12		48	60	mA	V_{CC} = 5V
Prescaler input voltage	13,14	12.5		300	mV_{RMS}	80MHz to 1GHz
Prescaler input voltage	13,14	30		300	mV_{RMS}	1.3GHz, see Fig. 5
Prescaler input impedance input capacitance	13,14		50 2		Ω pF	
SDA,SCL Input high voltage	4,5	3		V_{cc}	V	
Input low voltage	4,5	0		1.5	V	
Input high current	4,5			10	μA	Input Voltage = V_{CC}
Input low current	4,5			-10	μA	Input Voltage = 0V
Leakage current	4,5			10	μA	When V_{CC} = 0V
SDA Output voltage	4			0.4	V	I_{sink} = 3mA
Charge pump current low	1		± 50		μA	Byte 4 Bit 2 = 0, Pin 1 = 2V
Charge pump current high	1		± 170		μA	Byte 4 Bit 2 = 1, Pin 1 = 2V
Charge pump output leakage current	1			± 5	nA	Byte 4 Bit 4 = 1, Pin 1 = 2V
Charge pump drive output current	16	500			μA	V pin 16 = 0.7V
Charge Pump Amplifier Gain			6400			
Recommended crystal series resistance		10		200	Ω	
Crystal oscillator drive level			40		mVp-p	
Crystal oscillator source impedance	2		-400		Ω	Nominal Spread ± 15%
Output Ports						
Sink current	6,7,9-11	20			mA	V_{OUT} = 0.7V (See Note 1)
Leakage current	6,7,9-11			10	μA	V_{OUT} = 13.2V
Input Ports						
P3 input current high	8			1	mA	V pin 8 = V_{CC}
P3 input current low	8			-0.5	mA	V pin 8 = 0V

NOTE

1. Source impedance between all output ports and ground is approximately 5Ω. This should be taken into account when calculating output port saturation voltages.

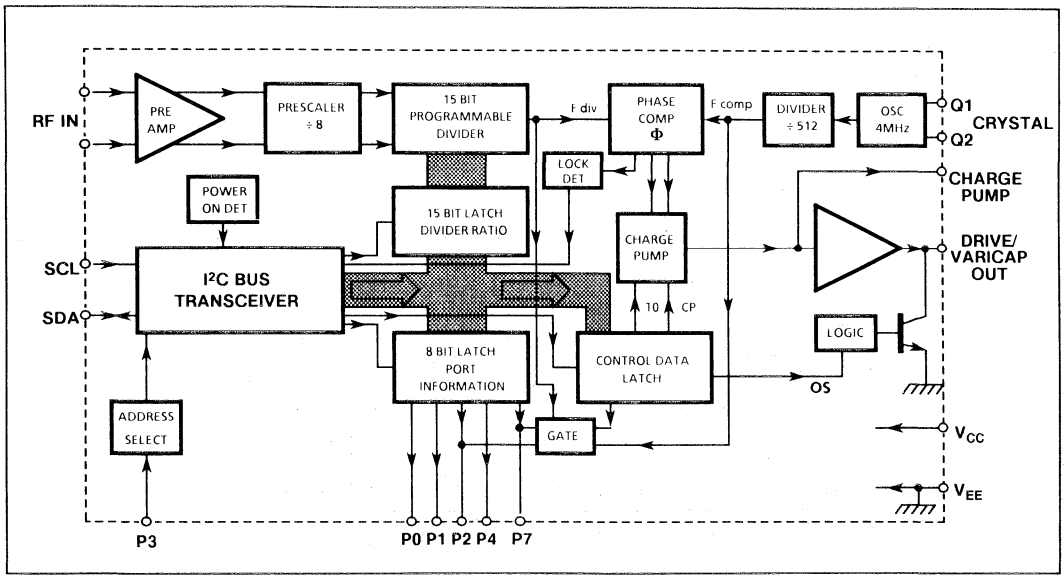


Fig 2 Block diagram of SP5502S. (Ports P0 and P4 not present on SP5502 and SP5502F)

FUNCTIONAL DESCRIPTION (Except where otherwise indicated, 'SP5502' refers to all variants)

The SP5502 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C BUS format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The address input is shown in Fig. 6. The last Bit of the address Byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5502 receives a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed. When the SP5502 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status Byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that Byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data Bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid byte (i.e. by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15 Bit shift register and is used to control the division ratio of the 15-Bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig 5. The input impedance is shown in Fig. 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{comp}.

When frequency data is entered, the phase comparator, via the charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-chip 4MHz crystal controlled oscillator.

Note - the comparison frequency is 7.8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ± 170μA and a logic 0 for ±50μA allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P2 and P7, a logic 1 connects F_{comp} to P2 and F_{div} to P7.

Byte 5 programs the output ports P0-P2, P4 and P7 on the SP5502S (P1, P2 and P7 only on SP5502 and SP5502F); a logic 0 for a high impedance output, a logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2. Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below a nominal 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	**BYTE 1**
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**BYTE 2**
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**BYTE 3**
CHARGE PUMP AND TEST BITS	1	CP	T1	T0	1	1	1	OS	A	**BYTE 4**
IO PORT CONTROL BITS	P7	X	X	P4*	X	P2	P1	P0*	A	**BYTE 5**

Table 1 write data format (MSB is transmitted first)

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	**BYTE 1**
STATUS BYTE	POR	FL	N	N	N	N	N	N	A	**BYTE 2**

Table 2 read data format

A : Acknowledge Bit
MA1, MA0 : Variable address bits (see table 4)
CP : Charge Pump Current Select
T1 : Test Mode Selection
T0 : Charge Pump Disable
OS : Varactor Drive Output Disable Switch
P7, P4*, P2, P1, P0*, : Control Output States
POR : Power On Reset Indicator
FL : Phase Lock Detect Flag
X = Don't care
N = Not Valid

MA1	MA0	Voltage input to P3
0	0	0 - 0.1 V_{CC}
0	1	OPEN CIRCUIT
1	0	0.4 - 0.6 V_{CC} †
1	1	0.9 V_{CC} - V_{CC}

Table 4 Address selection

NOTES: † Programmed by connecting a 15kΩ resistor between Address Select Port P3 and V_{CC}.
* Don't care condition on SP5502 and SP5502F

Fig.3 Data formats

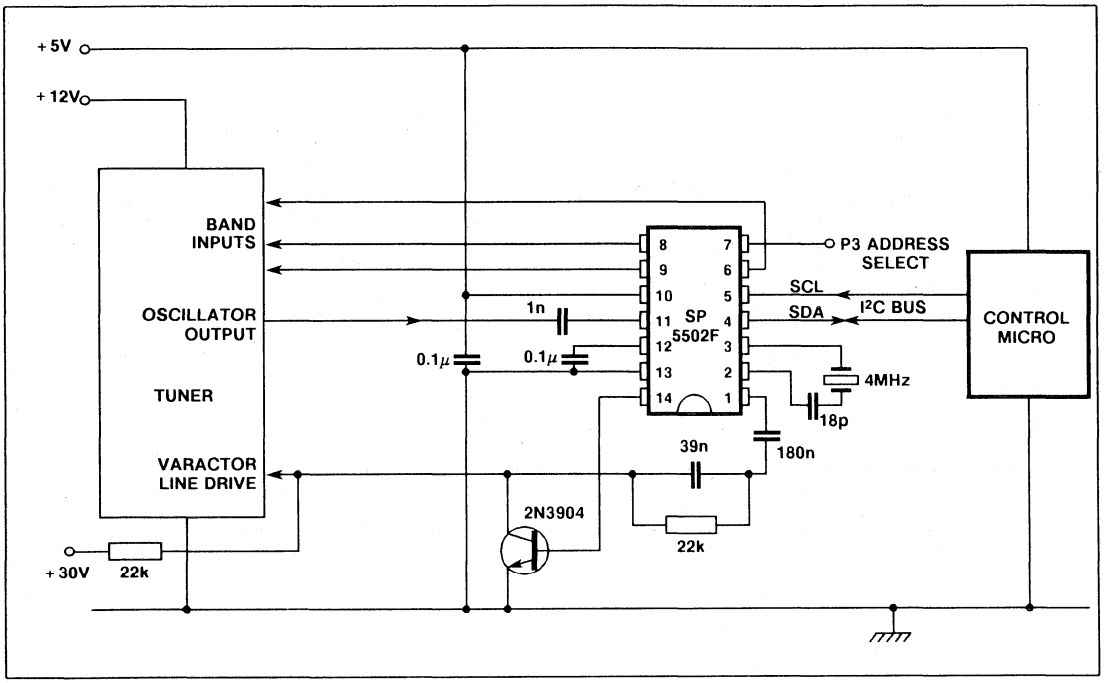


Fig. 4 Typical application

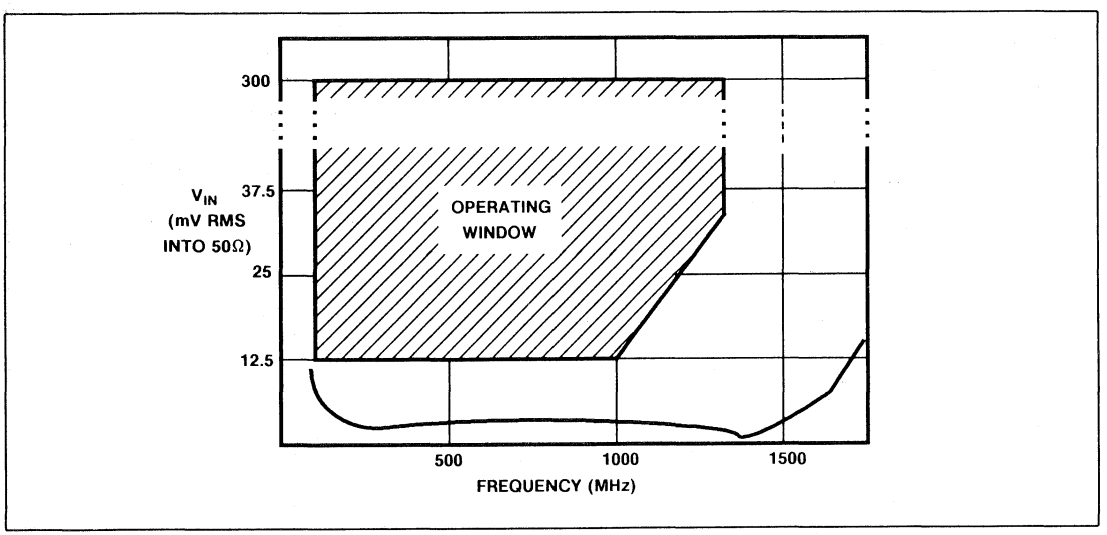
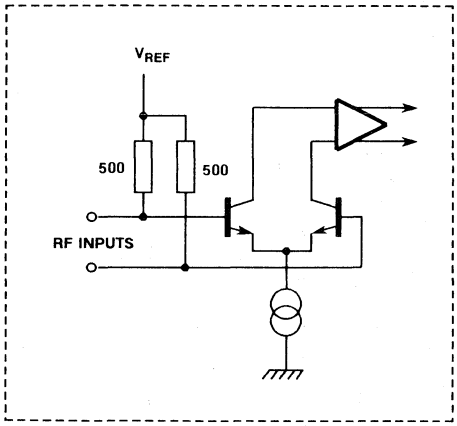
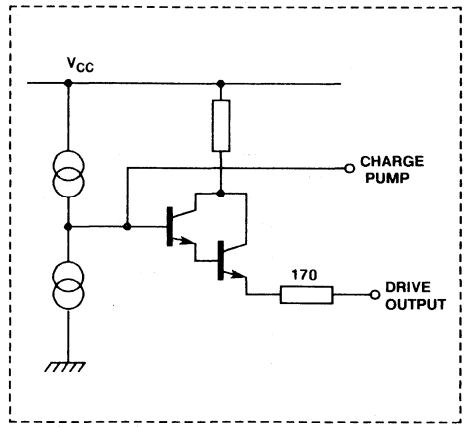


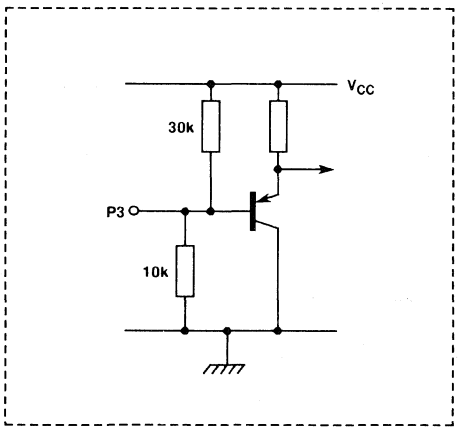
Fig.5 Typical input sensitivity



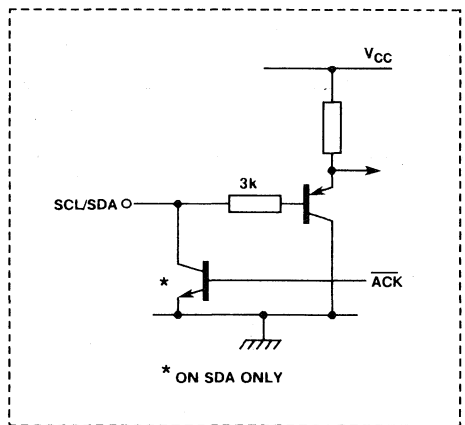
RF input



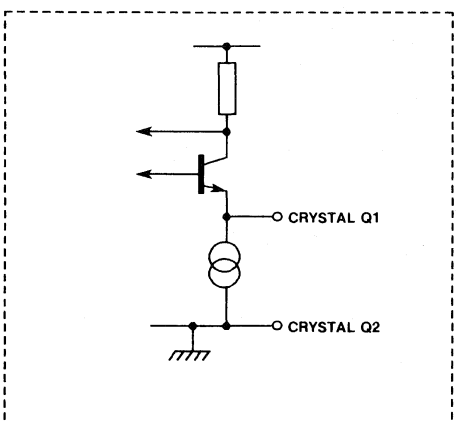
Loop amplifier



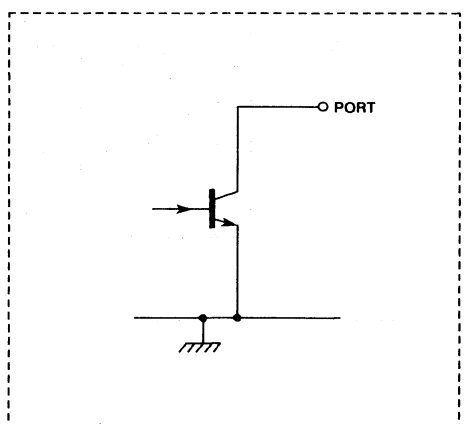
Address programming input



SCL and SDA input



Reference oscillator



Ports P0-P2, P4 and P7 (SP5502S), P1, P2 and P7 (SP5502 and SP5502F)

Fig.6 SP5502 input/output interface circuits

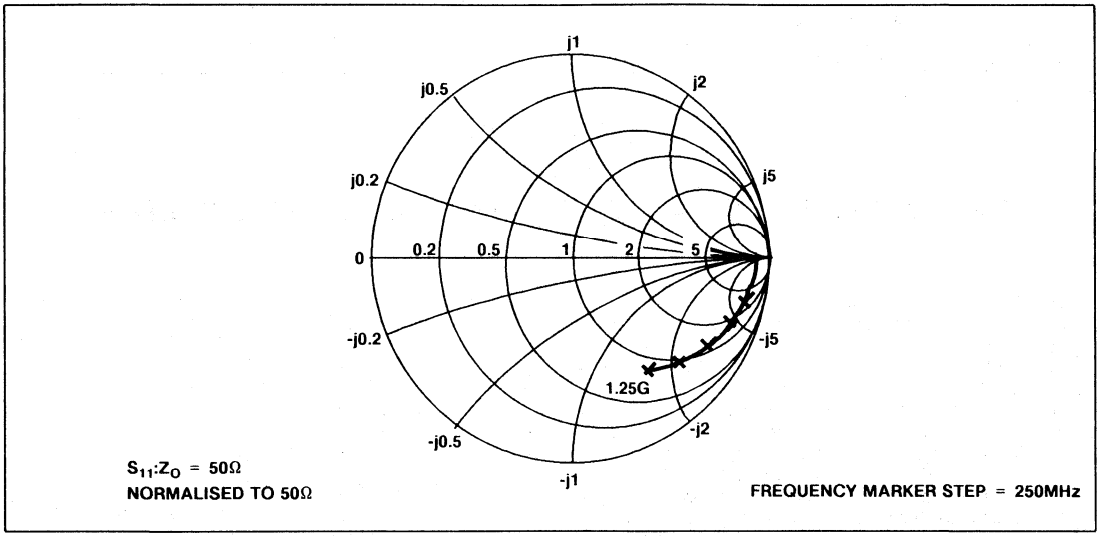


Fig.7 Typical input impedance

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} = 0V.

Parameter	Pin SP 5502S	Pin SP 5502/F	Value Min	Value Max	Units	Conditions
Supply voltage	12	10	-0.3	7	V	
RF input voltage	13, 14	11, 12		2.5	Vp-p	
Port voltage	6,7,9-11	6,8,9	-0.3	14	V	Port in off state
	6,7,9-11	6,8,9	-0.3	6	V	Port in on state
	8	7	-0.3	V_{CC} + 0.3	V	
Total port output current	6,7,9-11	6,8,9		50	mA	
RF input DC offset	13, 14	11, 12	-0.3	V_{CC} + 0.3	V	
Charge pump DC offset	1	1	-0.3	V_{CC} + 0.3	V	
Drive DC offset	16	14	-0.3	V_{CC} + 0.3	V	
Crystal oscillator DC offset	2	2	-0.3	V_{CC} + 0.3	V	
SDA, SCL input voltage	4, 5	4, 5	-0.3	V_{CC} + 0.3	V	With V_{CC} applied
			-0.3	5.5	V	V_{CC} not applied
Storage temperature			-55	+ 125	°C	
Junction temperature				+ 150	°C	
DP14 thermal resistance, chip-to-ambient				78	°C/W	
DP14 thermal resistance, chip-to-case				30	°C/W	
MP16 thermal resistance, chip-to-ambient				111	°C/W	
MP16 thermal resistance, chip-to-case				41	°C/W	
MP14 thermal resistance, chip-to-ambient				123	°C/W	
MP14 thermal resistance, chip-to-case				45	°C/W	
Power consumption at 5.5V				330	mW	

2184-1.3

SP5510

1.3 GHz BI-DIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

The SP5510 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. In 18-lead plastic DIL package (SP5510) and 20-lead miniature plastic package (SP5510T), the device has 4 addressable current-limited outputs ports (P0-P3) and four addressable bi-directional open-collector ports (P4-P7), one of which (P6) is a 3-Bit ADC. The information on these ports can be read via the I²C BUS. The SP5510S is a variant in a 16-lead miniature plastic package, without P0-P2 but functionally identical in other respects to the other two variants. The device has one fixed I²C BUS address and 3 programmable addresses, permitting 2 or more synthesisers to be used in a system.

FEATURES

- Complete 1.3GHz Single Chip System
- Programmable via I²C BUS
- Low power consumption (5V 43mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 8 Controllable Outputs, 4 Bi-Directional (SP5510, SP5510T)
- 5 Controllable Outputs, 4 Bi-Directional (SP5510S)
- 5 Level ADC
- Variable I²C BUS Address For Picture in Picture TV
- Full ESD Protection *

* Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV when combined with SP4902 2.5GHz Prescaler
- Cable Tuning Systems
- VCRs

ORDERING INFORMATION

SP5510 DP (18 Lead Plastic Package)
SP5510S MP (16 Lead Miniature Plastic Package)
SP5510T MP (20 Lead Wide Body Miniature Plastic Package)

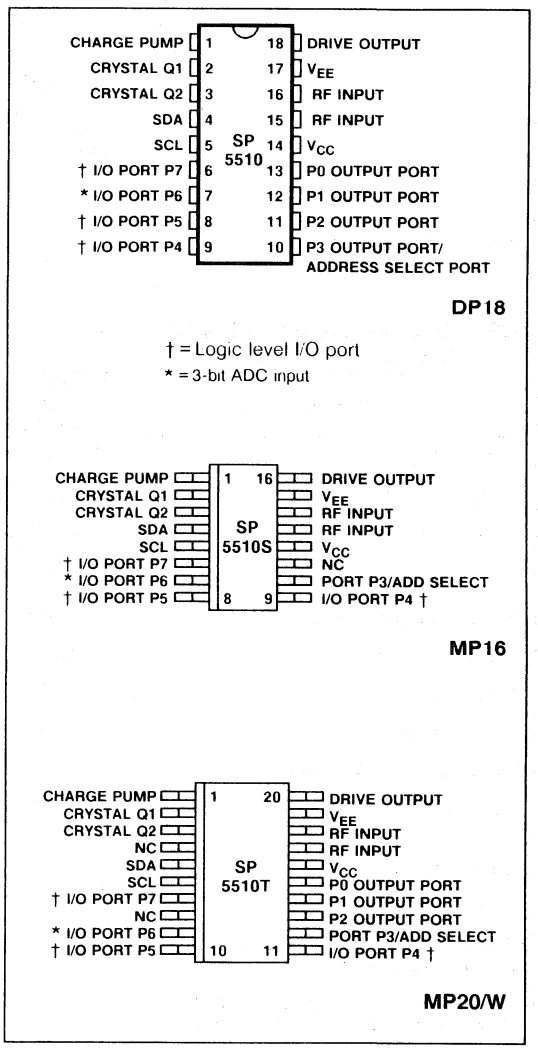


Fig.1 Pin connections - top view

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = –10°C to +80°C, V_{CC} = +4.5V to 5.5V

All pin connections refer to SP5510 (DP package)

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	14		43	53	mA	V_{CC} = 5V
Prescaler input voltage	15,16	12.5		300	mV_{RMS}	50MHz to 1GHz
Prescaler input voltage	15,16	30		300	mV_{RMS}	1.3GHz, see Fig. 5
Prescaler Input impedance Input capacitance	15,16		50 2		Ω pF	
SDA,SCL Input high voltage Input low voltage Input high current Input low current Leakage current	4,5 4,5 4,5 4,5 4,5	3 0		5.5 1.5 10 -10 10	V V µA µA µA	 Input voltage = V_{CC} Input voltage = 0V When V_{CC} = 0V
SDA Output voltage	4			0.4	V	I_{sink} = 3mA
Charge pump current low	1		±50		µA	Byte 4 Bit 2 = 0, Pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4 Bit 2 = 1, Pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4 Bit 4 = 1, Pin 1 = 2V
Charge pump drive output current	18	500			µA	V pin 18 = 0.7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	
Crystal oscillator drive level			40		mVp-p	
Crystal oscillator source impedance	2		-400		Ω	Nominal spread ± 15%
Output Ports						
P0-P3 sink current*	10-13	0.7	1	1.5	mA	V_{OUT} = 12V
P0-P3 leakage current*	10-13			10	µA	V_{OUT} = 13.2V
P4-P7 sink current	6-9	10			mA	V_{OUT} = 0.7V
P4-P7 leakage current	6-9			10	µA	V_{OUT} = 13.2V
Input Ports						
P3 Input current high	10			+10	µA	V pin10 = 13.2V
P3 Input current low	10			-10	µA	V pin10 = 0V
P4,P5,P7 input voltage low	6,8,9			0.8	V	
P4,P5,P7 input voltage high	6,8,9	2.7			V	
P6 Input current high	7			+10	µA	See Table 3 for ADC Levels
P6 Input current low	7			-10	µA	

* Ports P0-P2 not present on the SP5510S.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V. Pin references are for SP5510 (DP18 package)

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Supply voltage	14	-0.3	7	V	
RF input voltage	15, 16		2.5	Vp-p	
Port voltage	6 - 13	-0.3	14	V	Port in off state
	6 - 9	-0.3	6	V	Port in on state
	10-13	-0.3	14	V	Port in on state
Total port output current	6-13		50	mA	
RF input DC offset	15, 16	-0.3	$V_{CC}+0.3$	V	
Charge pump DC offset	1	-0.3	$V_{CC}+0.3$	V	
Drive DC offset	18	-0.3	$V_{CC}+0.3$	V	
Crystal oscillator DC offset	2	-0.3	$V_{CC}+0.3$	V	
SDA, SCL input voltage	4, 5	-0.3	$V_{CC}+0.3$	V	With V_{CC} applied
		-0.3	5.5	V	V_{CC} not applied
Storage temperature		-55	+125	°C	
Junction temperature			+150	°C	
DP18 thermal resistance, chip-to-ambient			78	°C/W	
DP18 thermal resistance, chip-to-case			24	°C/W	
MP16 thermal resistance, chip-to-ambient			111	°C/W	
MP16 thermal resistance, chip-to-case			41	°C/W	
MP20 thermal resistance, chip-to-ambient			93	°C/W	
MP20 thermal resistance, chip-to-case			34	°C/W	
Power consumption at 5.5V			275	mW	

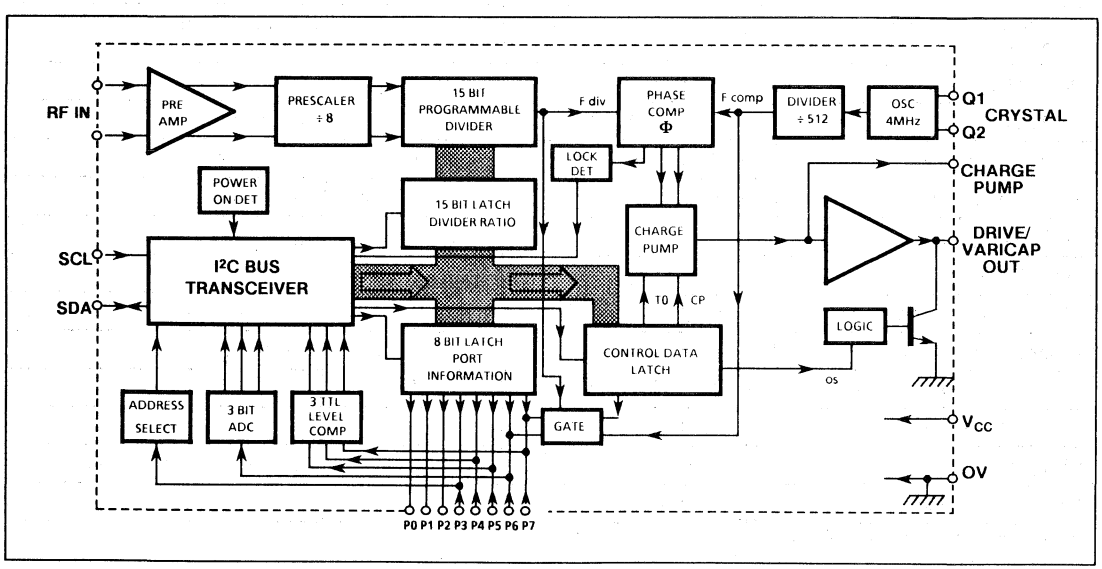


Fig. 2 Block diagram. (Ports P0-P2 not present on SP5510S)

FUNCTIONAL DESCRIPTION

The SP5510 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C BUS format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The last Bit of the address Byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5510 receives a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed. When the SP5510 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status Byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that Byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data Bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid byte (i.e., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15 Bit shift register and is used to control the division ratio of the 15 Bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is shown in Figs. 7 and 8.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP}.

When frequency data is entered, the phase comparator, via the charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by the on-chip 4MHz crystal controlled oscillator.

Note - the comparison frequency is 7.8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for $\pm 170\mu A$ and a logic 0 for $\pm 50\mu A$ allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{COMP} to P6 and F_{DIV} to P7

Byte 5 programs the output ports P0 to P7, a logic 0 for a high impedance output; a logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2,I1,I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with standard TTL voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5 level ADC.

The 5-level ADC can be used to feed AFC information to the microprocessor from the IF section of the television, as illustrated in the typical application circuit.

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig 6.

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	**BYTE 1**
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**BYTE 2**
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**BYTE 3**
CHARGE PUMP AND TEST BITS	1	CP	T1	T0	1	1	1	OS	A	**BYTE 4**
IO PORT CONTROL BITS	P7	P6	P5	P4	P3	P2*	P1*	P0*	A	**BYTE 5**

Table 1 Write data format (MSB is transmitted first)

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	**BYTE 1**
STATUS BYTE	POR	FL	I2	I1	I0	A2	A1	A0	A	**BYTE 2**

Table 2 Read data format

A : Acknowledge Bit
MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select
T1 : Test mode selection
T0 : Charge pump disable
OS : Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P2*, P1*, P0* : control output states
POR : Power On Reset indicator
FL : Phase Lock detect Flag
I2, I1, I0 : Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0 : 5 Level ADC data from P6 (see Table 3)

A2	A1	A0	Voltage input to P6
1	0	0	0.6V_{CC} to 13.2V
0	1	1	0.45V_{CC} to 0.6V_{CC}
0	1	0	0.3V_{CC} to 0.45 V_{CC}
0	0	1	0.15V_{CC} to 0.3 V_{CC}
0	0	0	0 to 0.15 V_{CC}

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	0 - 0.2 V_{CC}
0	1	ALWAYS VALID
1	0	0.3 - 0.7 V_{CC}
1	1	0.8 V_{CC} - 13.2V

Table 4 Address selection

NOTE: * Don't care condition on SP5510S

Fig. 3 Data Formats

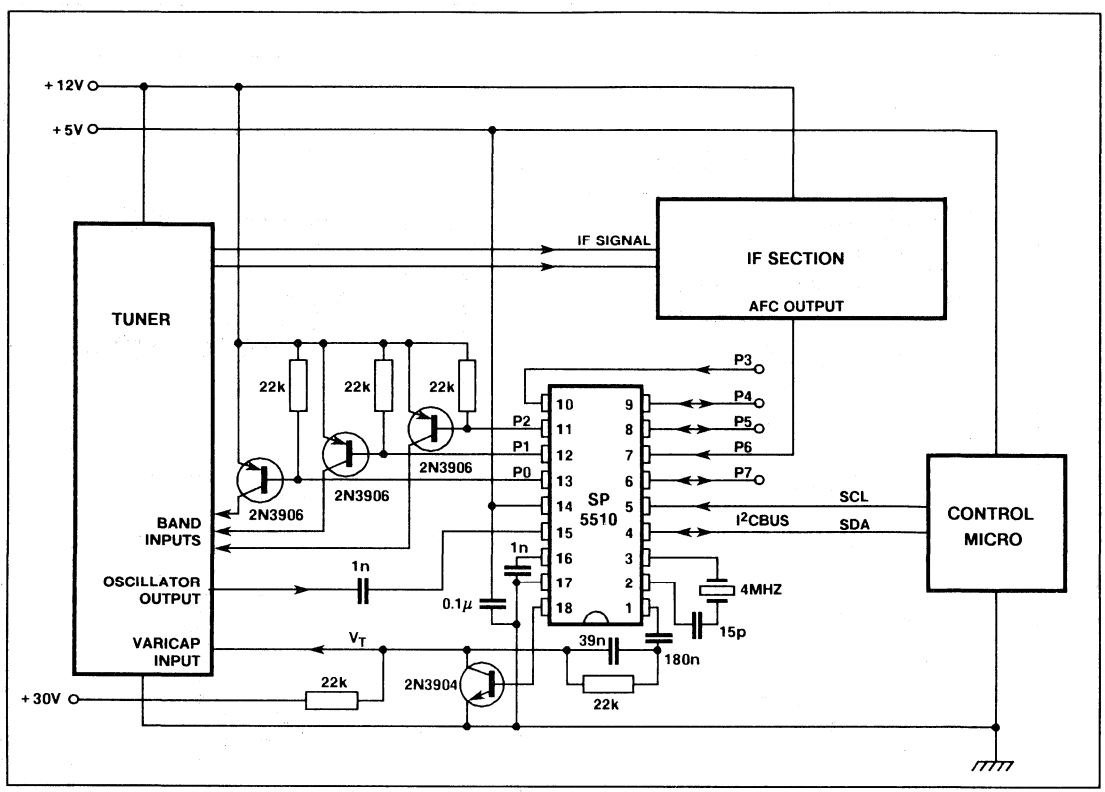


Fig.4 Typical SP5510 application

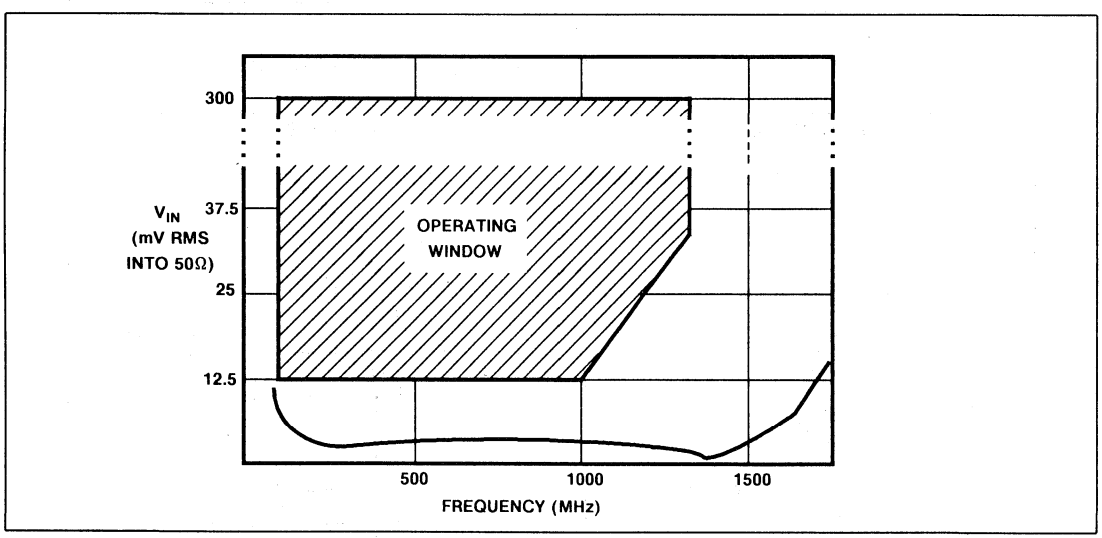
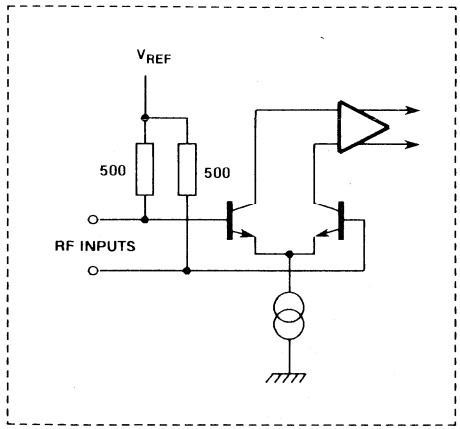
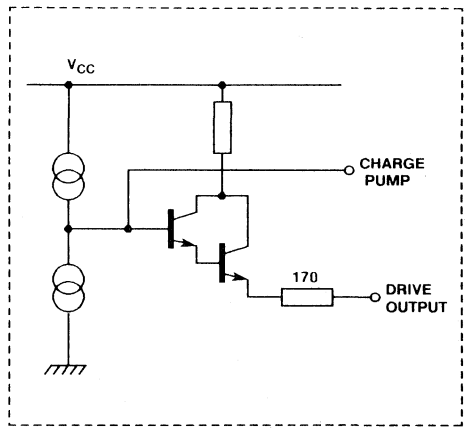


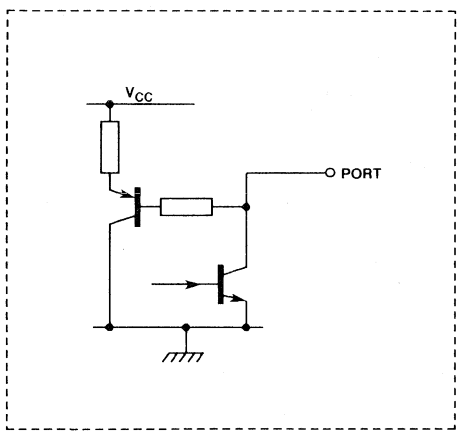
Fig.5 Typical input sensitivity



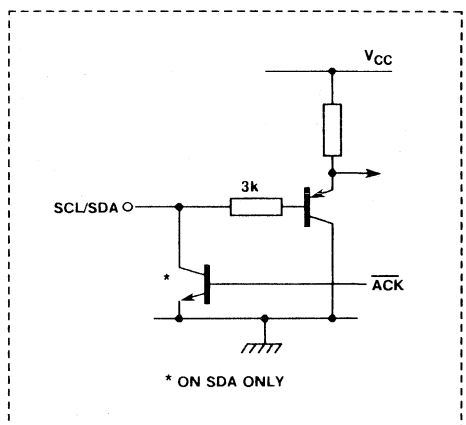
RF input



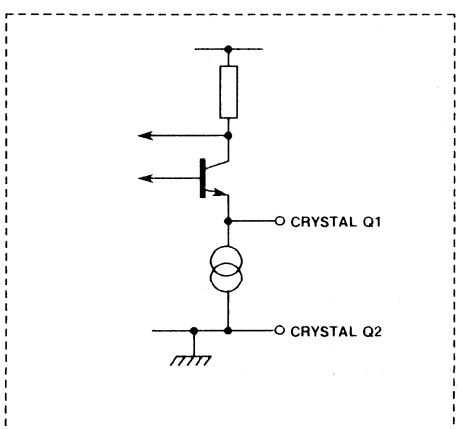
Loop amplifier



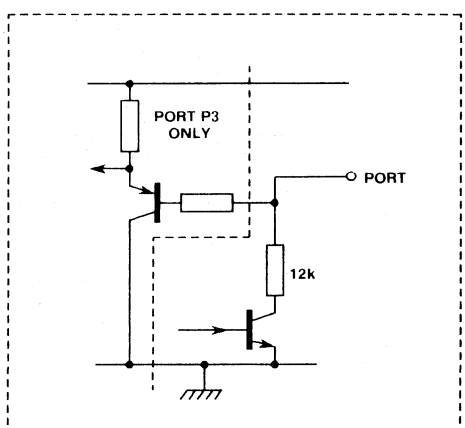
Ports P7 - P4



SCL and SDA input



Reference oscillator



Ports P0-P3 (SP5510, SP5510T), P3 only on SP5510S

Fig.6 SP5510 input/output interface circuits

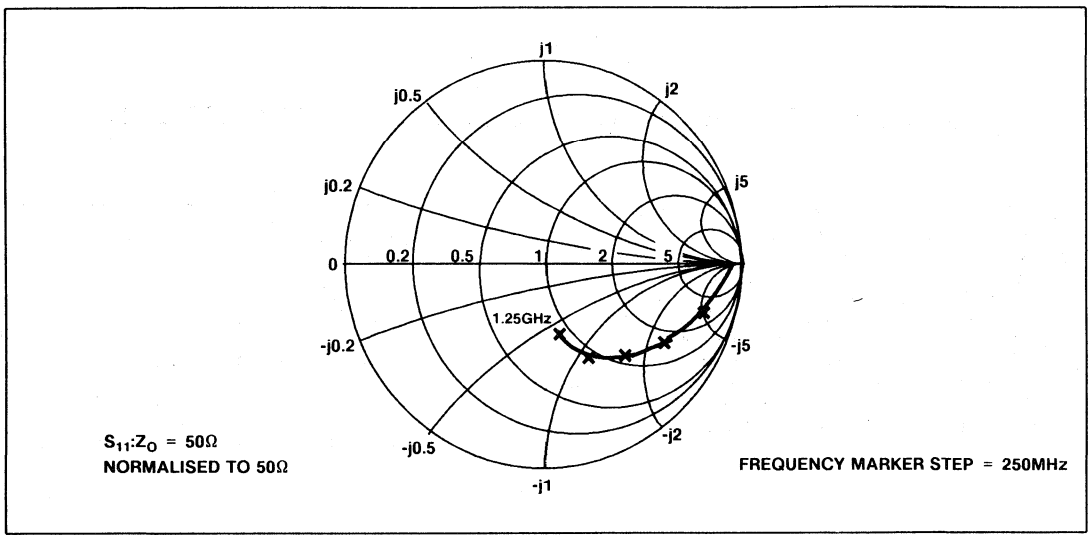


Fig.7 Typical input Impedance SP5510

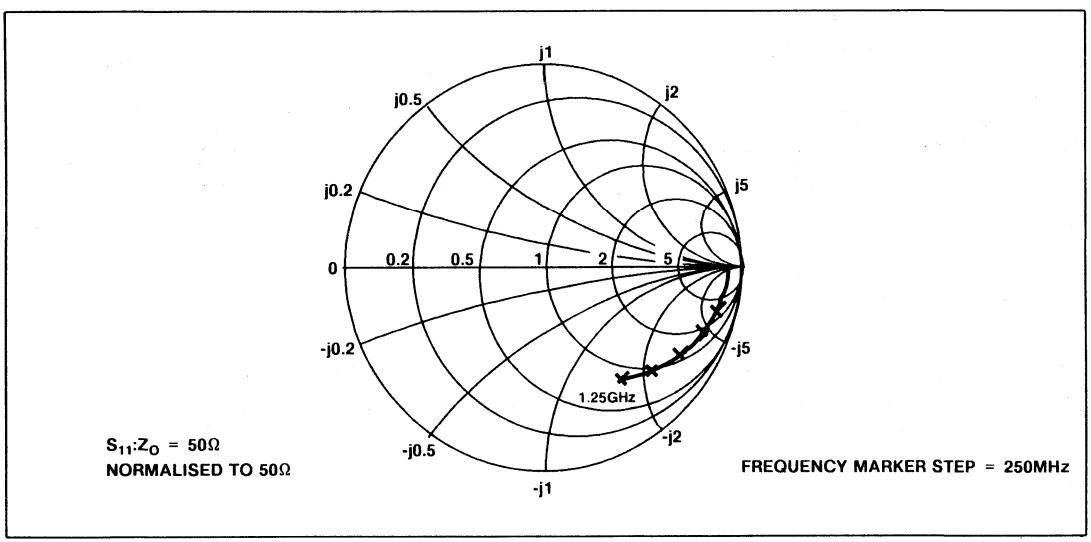


Fig.8 Typical input impedance SP5510S and SP5510T

3090-1.2

SP5511

1.3 GHz BI-DIRECTIONAL I²C BUS 4-ADDRESS SYNTHESISER

The SP5511 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. In 18-lead plastic DIL package, the SP5511 has 3 addressable current limited outputs (P0-P2) and 4 addressable bi-directional open-collector ports (P4-P7) of which P6 is a 3-Bit ADC. The SP5511S is a variant in a 16-lead miniature platic package, without P0-P2 but identical in other respects to the SP5511. The information on these ports can be read via the I²C BUS. The device has 4 programmable I²C BUS addresses, permitting 2 or more synthesisers to be used in a system.

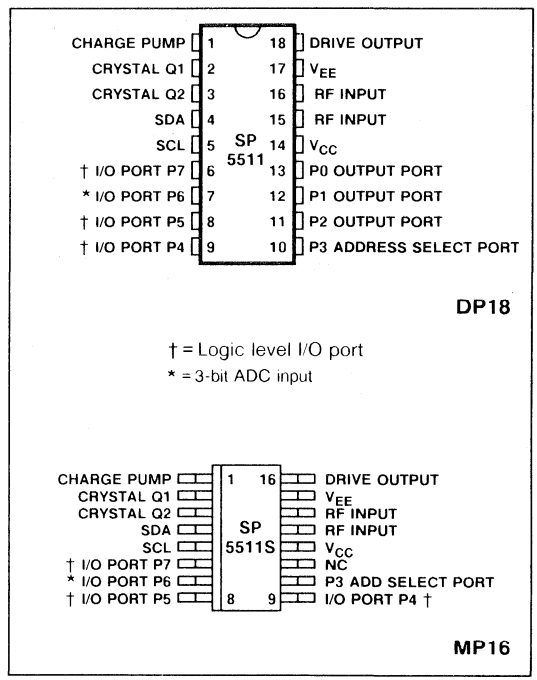


Fig.1 Pin connections - top view

FEATURES

- Complete 1.3GHz Single Chip System
- Programmable via I²C BUS
- Low power consumption (5V 48mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 7 Controllable Outputs, 4 Bi-Directional (SP5511)
  4 Bi-Directional Controllable Outputs (SP5511S)
- 5 Level ADC
- Variable I²C BUS Address For Picture in Picture TV
- Full ESD Protection *

* Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV when combined with SP4902 2.5GHz Prescaler
- Cable Tuning Systems
- VCRs

ORDERING INFORMATION

SP5511 DP (18 Lead Plastic Package)
SP5511S MP (16 Lead Miniature Plastic Package)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = –10°C to +80°C, V_{CC} = +4.5V to 5.5V

All pin connections refer to SP5511 (DP package)

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	14		48	60	mA	V_{CC} = 5V
Prescaler input voltage	15,16	12.5		300	mV_{RMS}	80MHz to 1GHz
Prescaler input voltage	15,16	30		300	mV_{RMS}	1.3GHz, see Fig. 5
Prescaler Input impedance Input capacitance	15,16		50 2		Ω pF	
SDA,SCL Input high voltage Input low voltage Input high current Input low current Leakage current	4,5 4,5 4,5 4,5 4,5	3 0		5.5 1.5 10 -10 10	V V µA µA µA	 Input voltage = V_{CC} Input voltage = 0V When V_{CC} = 0V
SDA Output voltage	4			0.4	V	I_{sink} = 3mA
Charge pump current low	1		± 50		µA	Byte 4 Bit 2 = 0, Pin 1 = 2V
Charge pump current high	1		± 170		µA	Byte 4 Bit 2 = 1, Pin 1 = 2V
Charge pump output leakage current	1			± 5	nA	Byte 4 Bit 4 = 1, Pin 1 = 2V
Charge pump drive output current	18	500			µA	V pin 18 = 0.7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	
crystal oscillator drive level			40		mVp-p	
Crystal oscillator source impedance	2		-400		Ω	Nominal spread ± 15%
Output Ports						
P0-P2 sink current*	11-13	0.7	1	1.5	mA	V_{OUT} = 12V
P0-P2 leakage current*	11-13			10	µA	V_{OUT} = 13.2V
P4-P7 sink current	6-9	10			mA	V_{OUT} = 0.7V
P4-P7 leakage current	6-9			10	µA	V_{OUT} = 13.2V
Input Ports						
P3 Input current high	10			1	mA	V pin10 = V_{CC}
P3 Input current low	10			-0.5	mA	V pin10 = 0V
P4,P5,P7 input voltage low	6,8,9			0.8	V	
P4,P5,P7 input voltage high	6,8,9	2.7			V	
P6 Input current high	7			+ 10	µA	See Table 3 for ADC Levels
P6 Input current low	7			-10	µA	

* Ports P0-P2 not present on the SP5511S.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V.

Parameter	Pin SP5511	Pin SP5511S	Value Min	Value Max	Units	Conditions
Supply voltage	14	12	-0.3	7	V	
RF input voltage	15, 16	13, 14		2.5	Vp-p	
Port voltage	6-9,11-13	6 - 9	-0.3	14	V	Port in off state
	6 - 9	6 - 9	-0.3	6	V	Port in on state
	11-13	-	-0.3	14	V	Port in on state
	10	10	-0.3	V_{CC} + 0.3	V	
Total port output current	6-9,11-13	6 - 9		50	mA	
RF input DC offset	15, 16	13, 14	-0.3	V_{CC} + 0.3	V	
Charge pump DC offset	1	1	-0.3	V_{CC} + 0.3	V	
Drive DC offset	18	16	-0.3	V_{CC} + 0.3	V	
Crystal oscillator DC offset	2	2	-0.3	V_{CC} + 0.3	V	
SDA, SCL input voltage	4, 5	4, 5	-0.3	V_{CC} + 0.3	V	With V_{CC} applied
			-0.3	5.5	V	V_{CC} not applied
Storage temperature			-55	+ 125	°C	
Junction temperature				+ 150	°C	
DP18 thermal resistance, chip-to-ambient				78	°C/W	
DP18 thermal resistance, chip-to-case				24	°C/W	
MP16 thermal resistance, chip-to-ambient				111	°C/W	
MP16 thermal resistance, chip-to-case				41	°C/W	
Power consumption at 5.5V				275	mW	

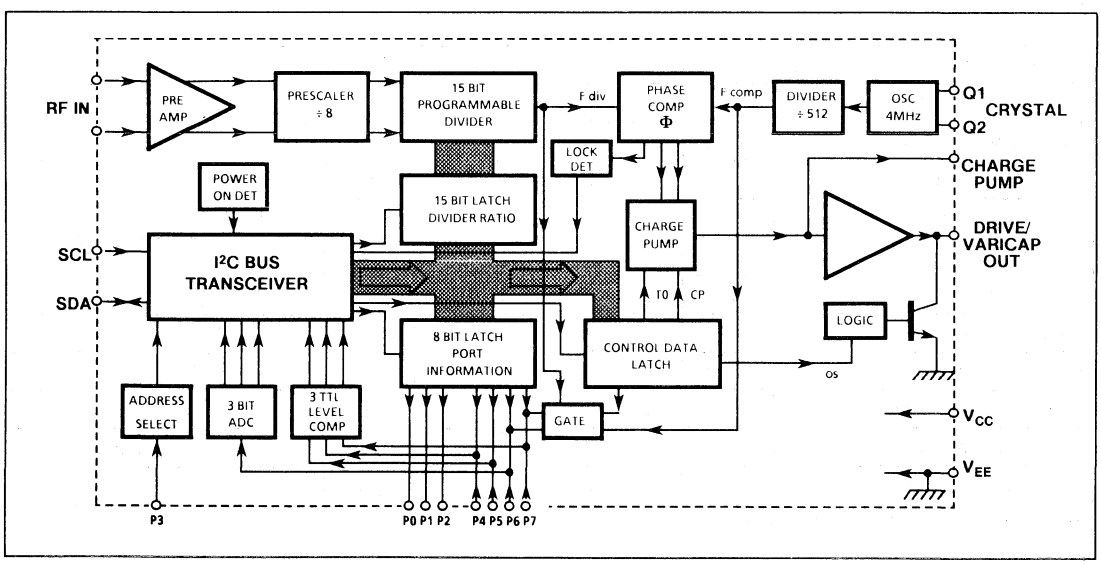


Fig. 2 Block diagram. (Ports P0-P2 not present on SP5511S)

FUNCTIONAL DESCRIPTION

The SP5511 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C BUS format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The address input is shown in Fig.6. The last Bit of the address Byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5511 receives a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed. When the SP5511 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status Byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2 + 3 select the synthesised frequency while Bytes 4 + 5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that Byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data Bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid byte (e.g. by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15 Bit shift register and is used to control the division ratio of the 15 Bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is displayed in Figs. 7 and 8.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{comp}.

When frequency data is entered, the phase comparator, via the charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-board 4MHz crystal controlled oscillator.

Note - the comparison frequency is 7.8125KHz when a 4Mhz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ± 170µA and a logic 0 for ± 50 µA allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{comp} to P6 and F_{div} to P7.

Byte 5 programs the output ports P0 to P2 and P4 to P7; a logic 0 for a high impedance output , a logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below 3 Volts and the programmed information lost (eg: when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2,I1,I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with standard TTL voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5 level ADC.

The 5 level ADC can be used to feed AFC information to the microprocessor from the IF section of the television, as illustrated in the typical application circuit.

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	**BYTE 1**
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**BYTE 2**
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**BYTE 3**
CHARGE PUMP AND TEST BITS	1	CP	T1	T0	1	1	1	OS	A	**BYTE 4**
IO PORT CONTROL BITS	P7	P6	P5	P4	X	P2*	P1*	P0*	A	**BYTE 5**

Table 1 Write data format (MSB is transmitted first)

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	**BYTE 1**
STATUS BYTE	POR	FL	I2	I1	I0	A2	A1	A0	A	**BYTE 2**

Table 2 Read data format

A : Acknowledge Bit
MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select
T1 : Test mode selection
T0 : Charge pump disable
OS : Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P2*, P1*, P0* : control output states
POR : Power On Reset indicator
FL : Phase Lock detect Flag
I2, I1, I0 : Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0 : 5 Level ADC data from P6 (see Table 3)
X : Don't care

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0.45V_{CC}$ to $0.6V_{CC}$
0	1	0	$0.3V_{CC}$ to $0.45\ V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.3\ V_{CC}$
0	0	0	0 to $0.15\ V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	$0 - 0.1\ V_{CC}$
0	1	OPEN CIRCUIT
1	0	$0.4 - 0.6\ V_{CC}$ †
1	1	$0.9\ V_{CC} - V_{CC}$

Table 4 Address selection

NOTES: * Don't care condition on SP5511S
† Programmed by connecting a 15kΩ resistor between pin 10 and V_{CC}

Fig. 3 Data Formats

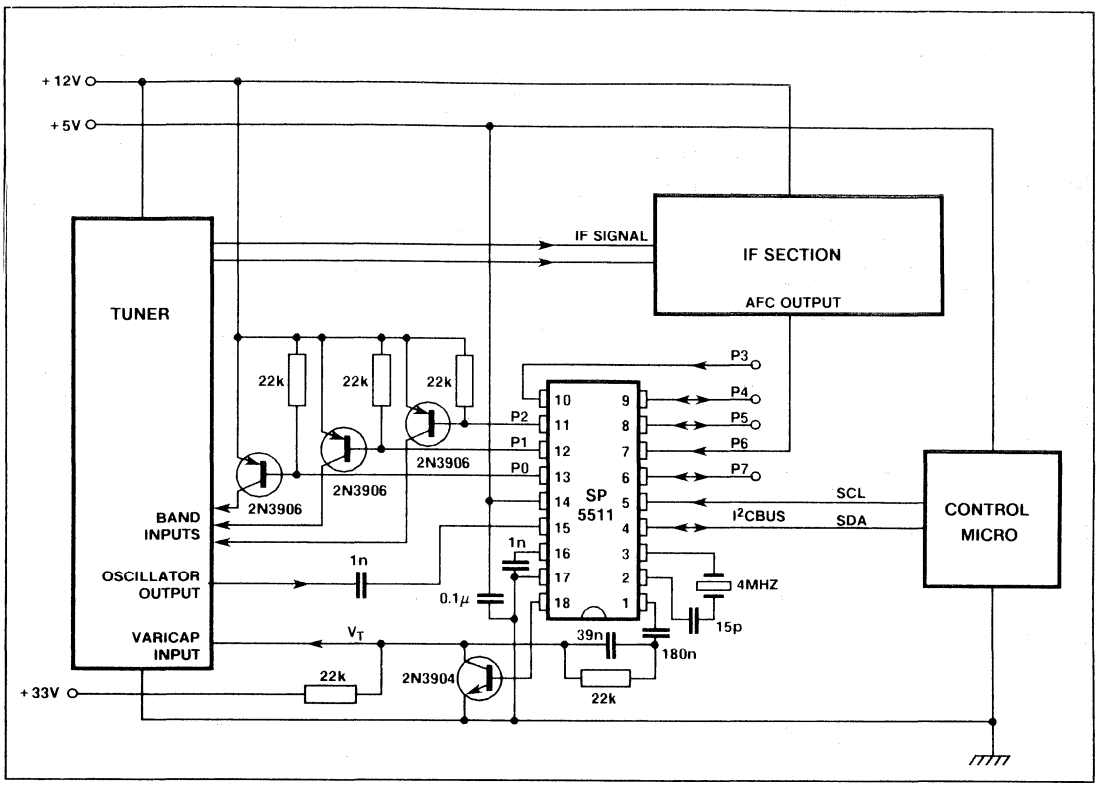


Fig.4 Typical SP5511 application

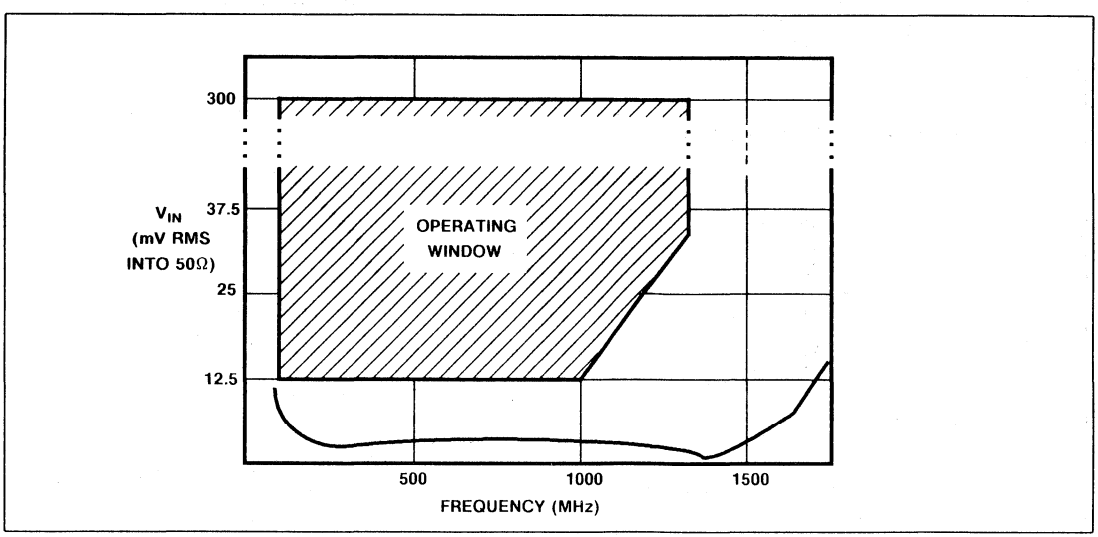
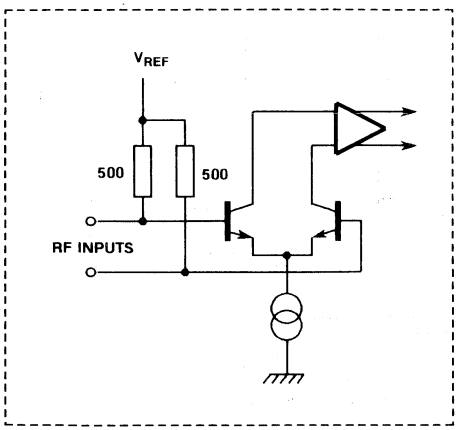
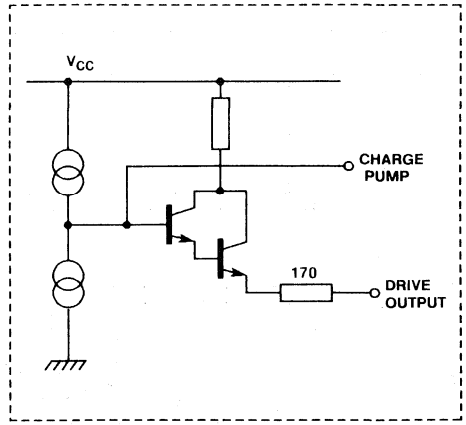


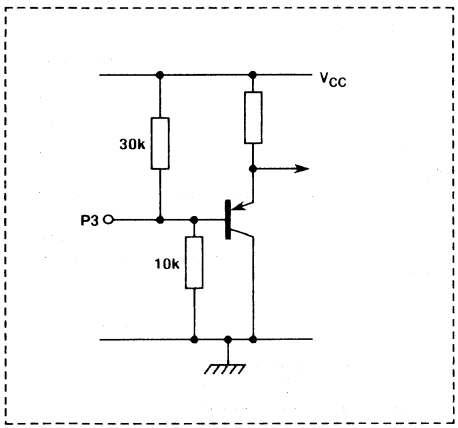
Fig.5 Typical input sensitivity



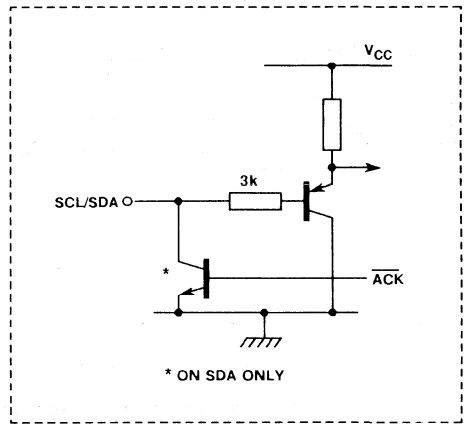
RF input



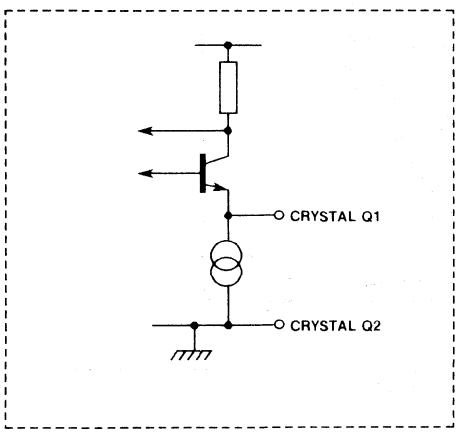
Loop amplifier



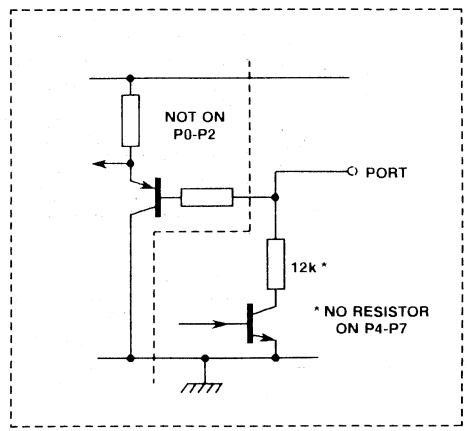
Address programming port



SCL and SDA input



Reference oscillator



Ports P0-P2 and P4-P7 (SP5511), P4-P7 only on SP5511S

Fig.6 SP5511 input/output interface circuits

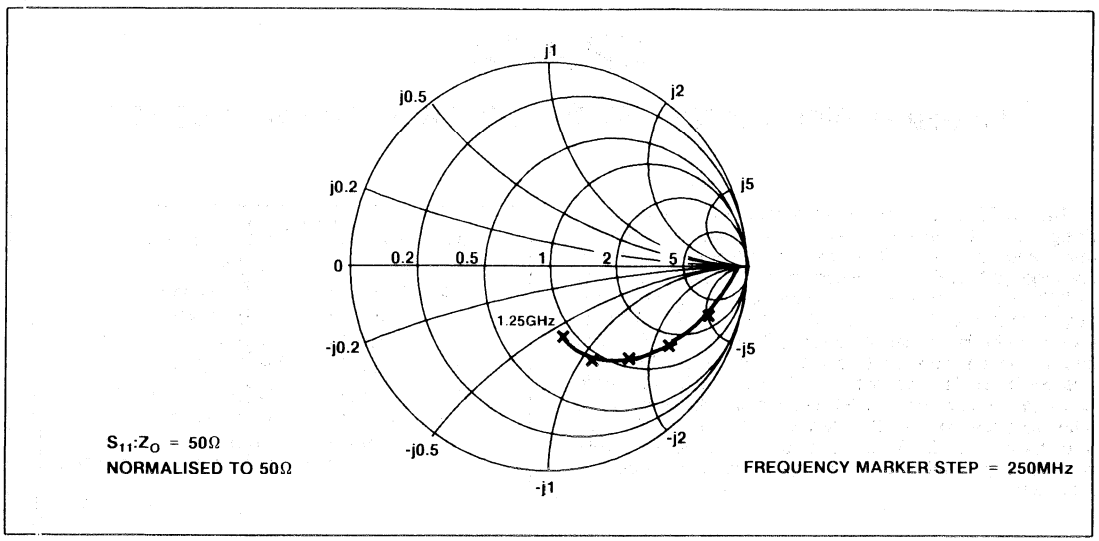


Fig.7 Typical input Impedance SP5511

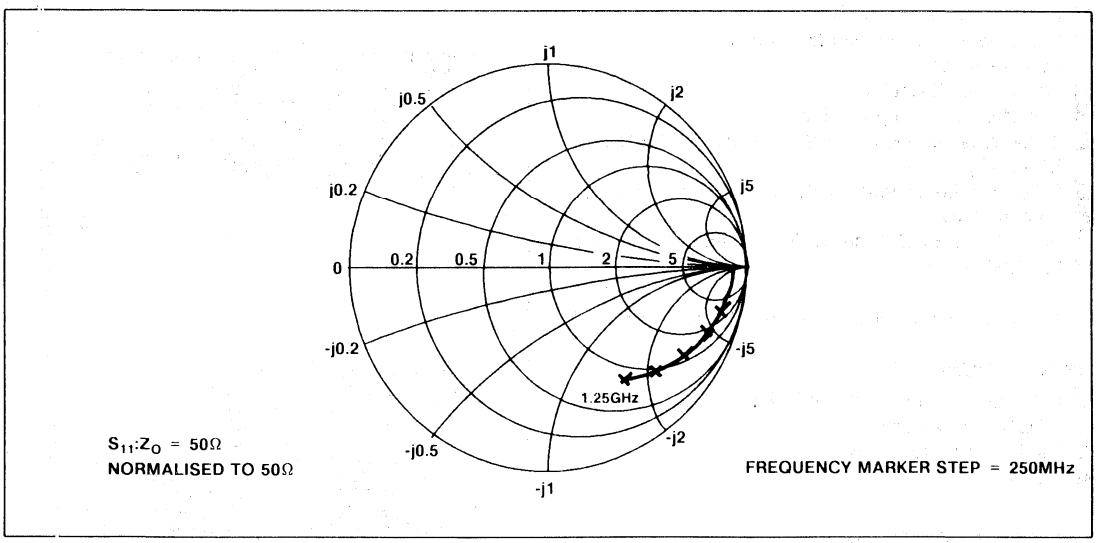


Fig.8 Typical input impedance SP5511S

2384-1.2

SP5512

1.3 GHz BI-DIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

The SP5512 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. In 18-lead plastic DIL package (SP5512) and 20-lead miniature plastic package (SP5512T), the device has 8 controllable open-collector output ports (P0-P7) each capable of sinking 20mA. Ports P4-P7 are bi-directional; in addition, P6 is a 3-Bit ADC. The information on these ports can be read via the I²C BUS. The SP5512S is a variant in a 16-lead miniature plastic package, without P0 and P1 but functionally identical in other respects to the other two variants. The device has one fixed I²C BUS address and 3 programmable addresses, permitting 2 or more synthesisers to be used in a system.

FEATURES

- Complete 1.3GHz Single Chip System
- Programmable via I²C BUS
- Low power consumption (5V 43mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 8 Controllable Outputs, 4 Bi-Directional (SP5512, SP5512T)
- 6 Controllable Outputs, 4 Bi-Directional (SP5512S)
- 5 Level ADC
- Variable I²C BUS Address For Picture in Picture TV
- Full ESD Protection *

* Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV when combined with SP4902 2.5GHz Prescaler
- Cable Tuning Systems
- VCRs

ORDERING INFORMATION

SP5512 DP (20 Lead Plastic Package)
SP5512S MP (16 Lead Miniature Plastic Package)
SP5512T MP (20 Lead Wide Body Miniature Plastic Package)

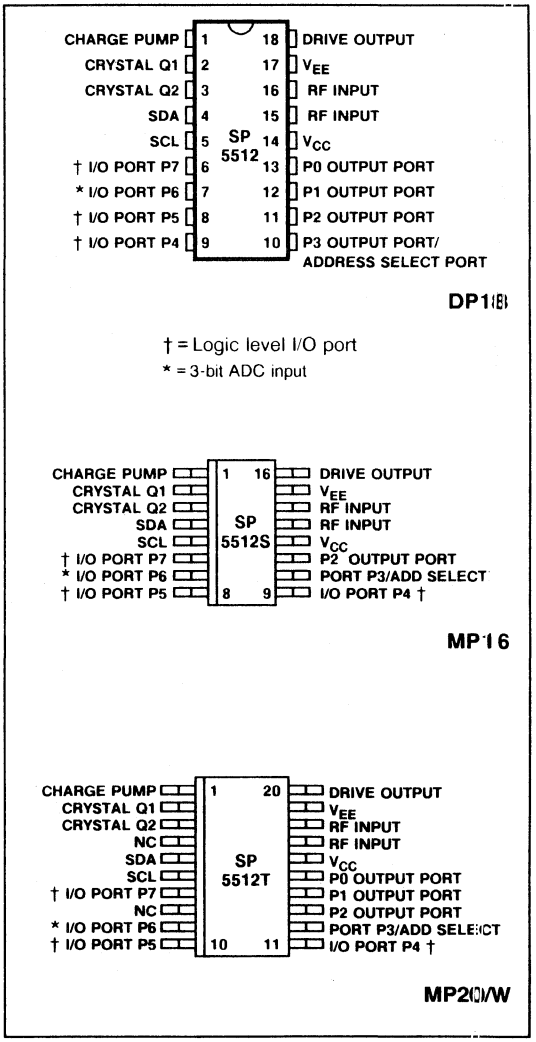


Fig.1 Pin connections - top view

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = –10°C to +80°C, V_{CC} = +4.5V to 5.5V

All pin connections refer to SP5512 (DP package)

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	14		43	53	mA	V_{CC} = 5V
Prescaler input voltage	15,16	12.5		300	mV_{RMS}	50MHz to 1GHz
Prescaler input voltage	15,16	30		300	mV_{RMS}	1.3GHz, see Fig. 5
Prescaler Input impedance Input capacitance	15,16		50 2		Ω pF	
SDA,SCL Input high voltage Input low voltage Input high current Input low current Leakage current	4,5 4,5 4,5 4,5 4,5	3 0		5.5 1.5 10 -10 10	V V µA µA µA	 Input voltage = V_{CC} Input voltage = 0V When V_{CC} = 0V
SDA Output voltage	4			0.4	V	I_{sink} = 3mA
Charge pump current low	1		±50		µA	Byte 4 Bit 2 = 0, Pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4 Bit 2 = 1, Pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4 Bit 4 = 1, Pin 1 = 2V
Charge pump drive output current	18	500			µA	V pin 18 = 0.7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	
Crystal oscillator drive level			40		mVp-p	
Crystal oscillator source impedance	2		-400		Ω	Nominal spread ± 15%
Output Ports						
P0-P7 sink current (see note 1)	6-13	20			mA	V_{OUT} = 0.7V, see note 2
P0-P7 leakage current (see note 1)	6-13			10	µA	V_{OUT} = 13.2V
Input Ports						
P3 Input current high	10			+10	µA	V pin10 = 13.2V
P3 Input current low	10			-10	µA	V pin10 = 0V
P4,P5,P7 input voltage low	6,8,9			0.8	V	
P4,P5,P7 input voltage high	6,8,9	2.7			V	
P6 Input current high	7			+10	µA	See Table 3 for ADC levels
P6 Input current low	7			-10	µA	

NOTES

1. Ports P0 and P1 not present on the SP5512S.
2. Source impedance between all output ports and ground is approximately 5Ω. This should be taken into account when calculating output port saturation voltages.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V. Pin references are for SP5512 (DP18 package)

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Supply voltage	14	-0.3	7	V	
RF input voltage	15, 16		2.5	Vp-p	
Port voltage	6 - 13 6 - 13	-0.3 -0.3	14 6	V V	Port in off state Port in on state
Total port output current	6-13		50	mA	
RF input DC offset	15, 16	-0.3	V_{CC} + 0.3	V	
Charge pump DC offset	1	-0.3	V_{CC} + 0.3	V	
Drive DC offset	18	-0.3	V_{CC} + 0.3	V	
Crystal oscillator DC offset	2	-0.3	V_{CC} + 0.3	V	
SDA, SCL input voltage	4, 5	-0.3 -0.3	V_{CC} + 0.3 5.5	V V	With V_{CC} applied V_{CC} not applied
Storage temperature		-55	+ 125	°C	
Junction temperature			+ 150	°C	
DP18 thermal resistance, chip-to-ambient DP18 thermal resistance, chip-to-case			78 24	°C/W °C/W	
MP16 thermal resistance, chip-to-ambient MP16 thermal resistance, chip-to-case			111 41	°C/W °C/W	
MP20 thermal resistance, chip-to-ambient MP20 thermal resistance, chip-to-case			93 34	°C/W °C/W	
Power consumption at 5.5V			275	mW	All ports off

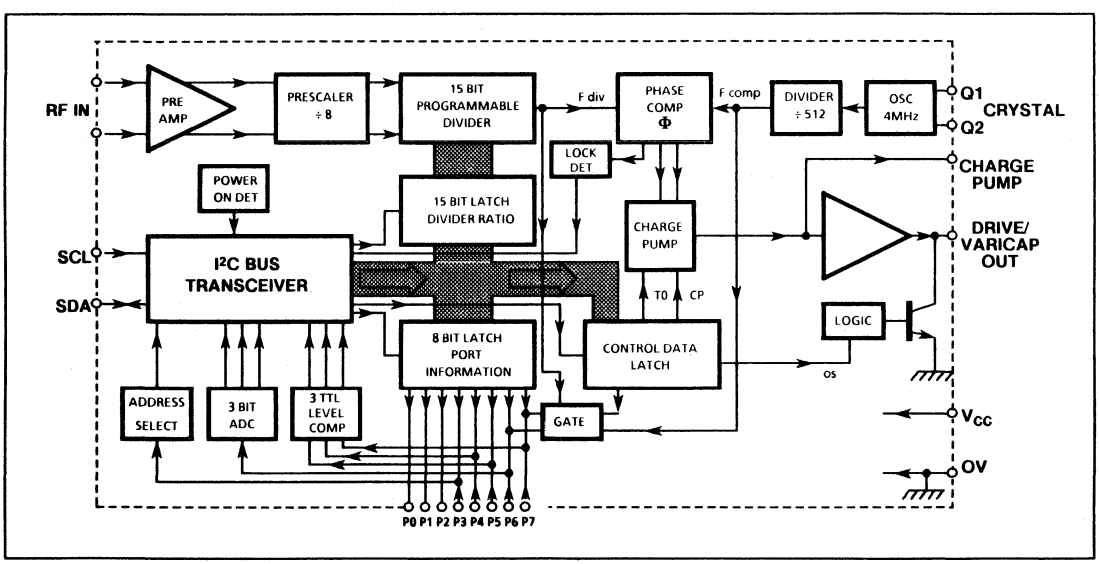


Fig. 2 Block diagram. (Ports P0 and P1 not present on SP5512S)

FUNCTIONAL DESCRIPTION

The SP5512 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C BUS format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The last Bit of the address Byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5512 receives a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed. When the SP5512 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status Byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that Byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data Bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid byte (e.g.., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15 Bit shift register and is used to control the division ratio of the 15 Bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is shown in Figs. 7 and 8.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP}.

When frequency data is entered, the phase comparator, via the charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by the on-chip 4MHz crystal controlled oscillator.

Note - the comparison frequency is 7.8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for $\pm 170\mu A$ and a logic 0 for $\pm 50\mu A$ allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{COMP} to P6 and F_{DIV} to P7

Byte 5 programs the output ports P0 to P7, a logic 0 for a high impedance output; a logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2,I1,I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with standard TTL voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5 level ADC.

The 5-level ADC can be used to feed AFC information to the microprocessor from the IF section of the television, as illustrated in the typical application circuit.

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig 6.

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	**BYTE 1**
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**BYTE 2**
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**BYTE 3**
CHARGE PUMP AND TEST BITS	1	CP	T1	T0	1	1	1	OS	A	**BYTE 4**
IO PORT CONTROL BITS	P7	P6	P5	P4	P3	P2	P1*	P0*	A	**BYTE 5**

Table 1 Write data format (MSB is transmitted first)

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	**BYTE 1**
STATUS BYTE	POR	FL	I2	I1	I0	A2	A1	A0	A	**BYTE 2**

Table 2 Read data format

A : Acknowledge Bit
MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select
T1 : Test mode selection
T0 : Charge pump disable
OS : Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P2, P1*, P0* : control output states
POR : Power On Reset indicator
FL : Phase Lock detect Flag
I2, I1, I0 : Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0 : 5 Level ADC data from P6 (see Table 3)

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0.45V_{CC}$ to $0.6V_{CC}$
0	1	0	$0.3V_{CC}$ to $0.45\ V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.3\ V_{CC}$
0	0	0	0 to $0.15\ V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	$0 - 0.2\ V_{CC}$
0	1	ALWAYS VALID
1	0	$0.3 - 0.7\ V_{CC}$
1	1	$0.8\ V_{CC}$ - 13.2V

Table 4 Address selection

NOTE: * Don't care condition on SP5512S

Fig. 3 Data Formats

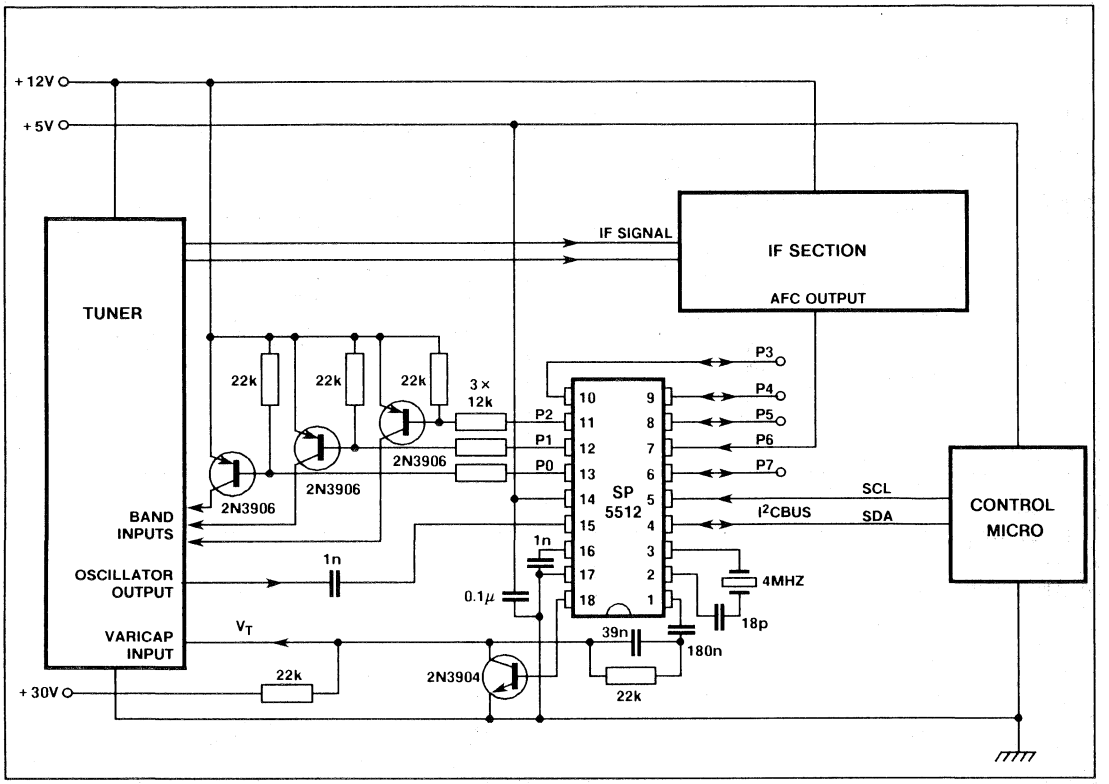


Fig.4 Typical SP5512 application

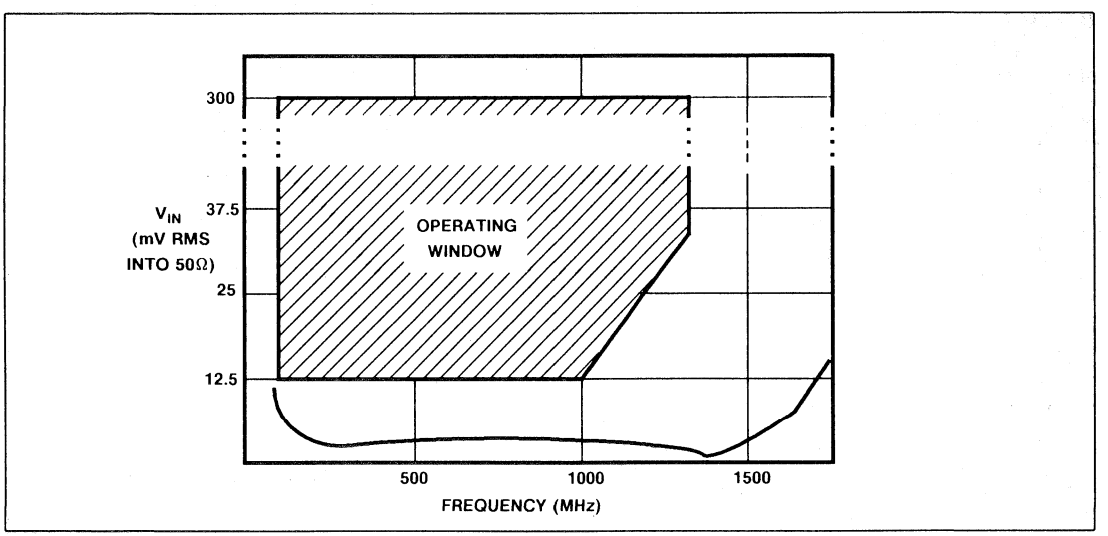
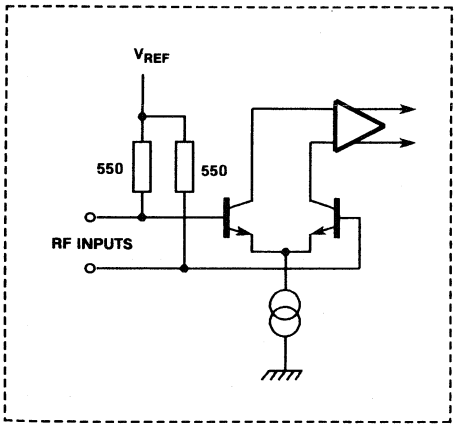
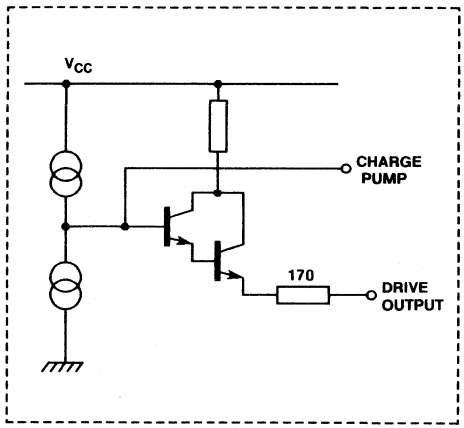


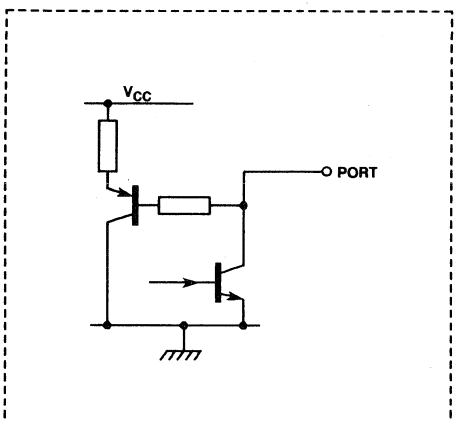
Fig.5 Typical input sensitivity



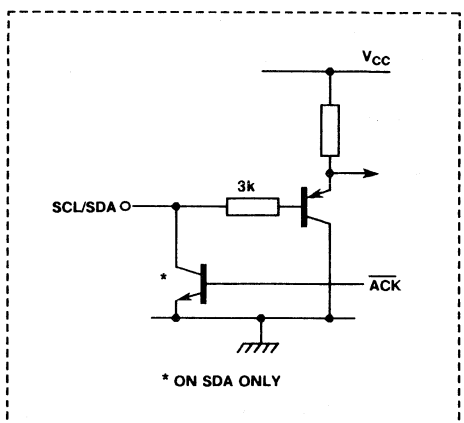
RF input



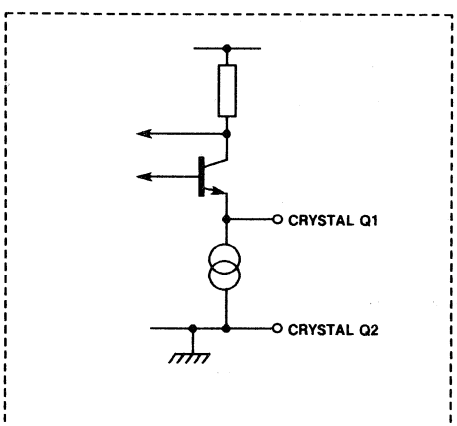
Loop amplifier



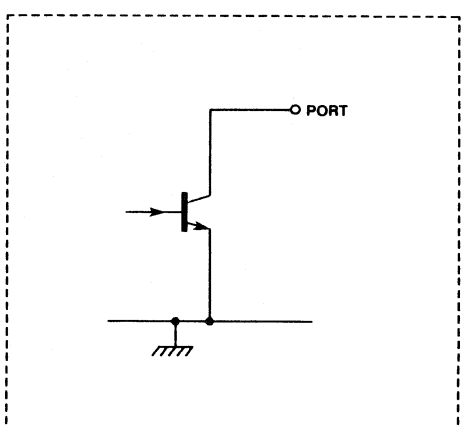
Ports P3 - P7



SCL and SDA input



Reference oscillator



Ports P0-P2 (P0 and P1 not present on SP5512S)

Fig.6 SP5512 input/output interface circuits

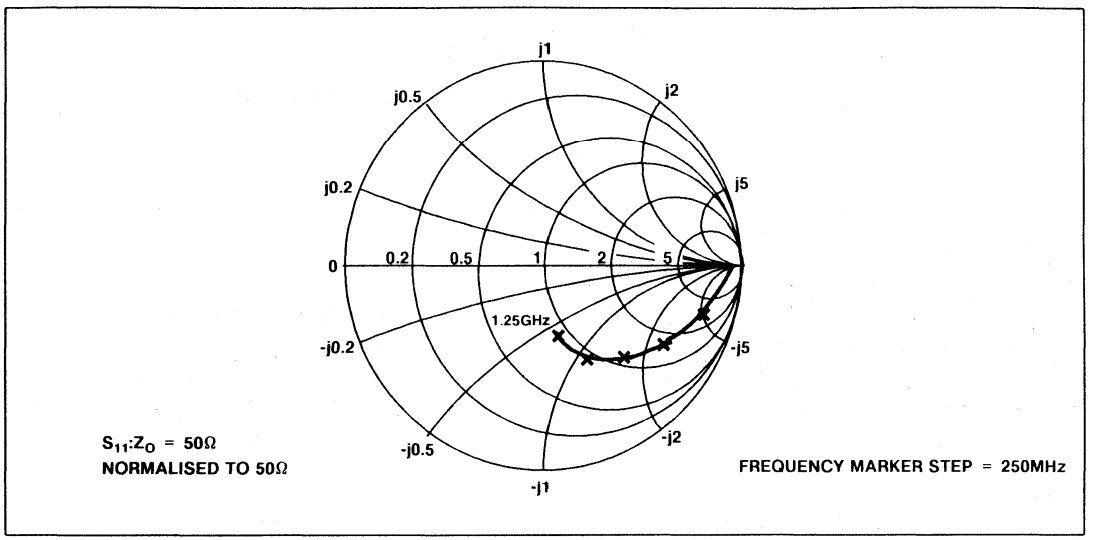


Fig.7 Typical input Impedance SP5512

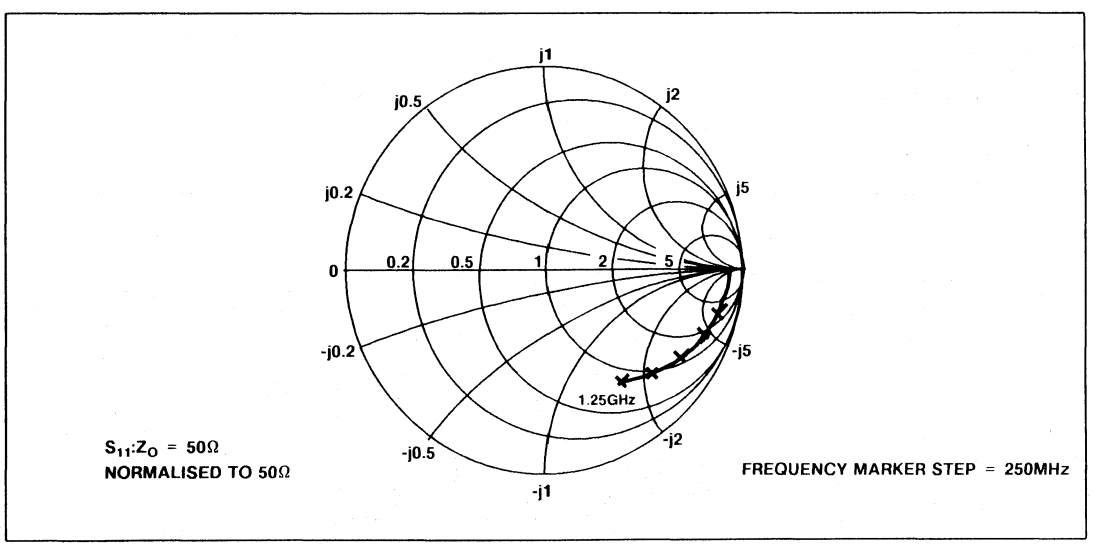


Fig.8 Typical input impedance SP5512S and SP5512T

SP5514S

1.3 GHz I²C BUS CONTROLLED SYNTHESISER

The SP5514S is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format, at a maximum rate of 500kHz. The device has one addressable current limited output port, P3, and four addressable open collector ports, P4-P7. The SP5514S has one fixed I²C BUS address and 3 programmable addresses, permitting 2 or more synthesisers to be used in a system. The comparison frequency is 7.8125kHz derived from a 4MHz crystal controlled oscillator.

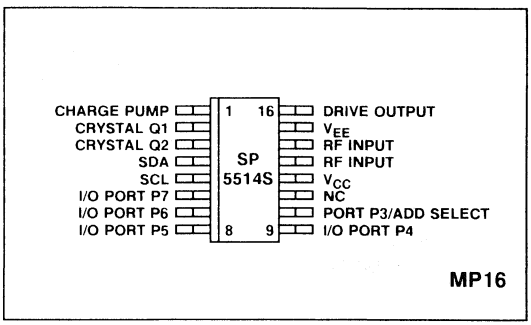


Fig.1 Pin Connections (Top View)

FEATURES

- Complete 1.3GHz Single Chip System
- Programmable via I²C BUS
- Low power consumption (5V 43mA)
- Low Radiation
- Varactor Drive Amp Disable
- 5 Controllable Outputs
- Full ESD Protection*
- 500kHz Clock Rate

* Normal ESD handling procedures should be observed

APPLICATIONS

- Satellite TV when combined with SP4902 2.5GHz Prescaler
- Cable Tuning Systems
- VCRs

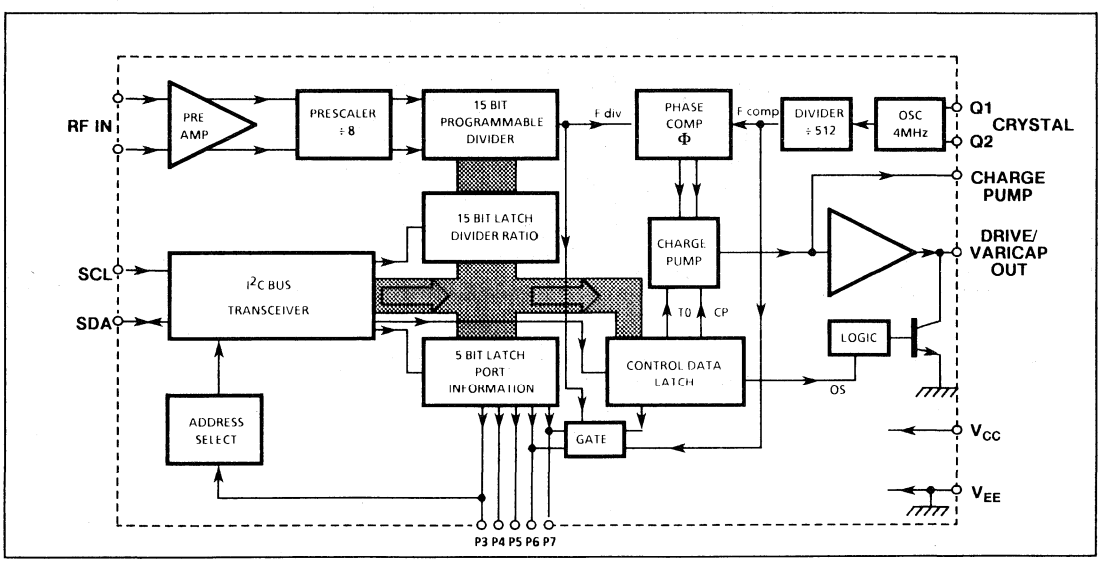


Fig.2 Block diagram of SP5514S

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = -10°C to 80°C, V_{CC} = +4.5V to 5.5V

These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	12		43	53	mA	V_{CC} = 5V
Prescaler input voltage	13,14	12.5		300	mV_{RMS}	50MHz to 1GHz
Prescaler input voltage	13,14	30		300	mV_{RMS}	1.3GHz, see Fig. 5
Prescaler Input impedance Input capacitance	13,14		50 2		Ω pF	
SDA,SCL Input high voltage Input low voltage Input high current Input low current Leakage current	4,5 4,5 4,5 4,5 4,5	3 0		5.5 1.5 10 -10 10	V V μA μA μA	 Input Voltage = V_{CC} Input Voltage = 0V When V_{CC} = 0V
SDA Output voltage	4			0.4	V	I_{sink} = 3mA
SCL clock rate	5			0.5	MHz	
Charge pump current low	1		±50		μA	Byte 4 Bit 2 = 0 Pin 1 = 2V
Charge pump current high	1		±170		μA	Byte 4 Bit 2 = 1 Pin 1 = 2V
Charge pump output leakage Current	1			±1	μA	Byte 4 Bit 4 = 1 Pin 1 = 2V
Charge pump drive output Current	16	500			μA	$V_{pin\ 16}$ = 0.7V
Output Ports						
P3 sink current	10	0.7	1	1.5	mA	V_{OUT} = 12V
P3 leakage current	10			10	μA	V_{OUT} = 13.2V
P4-P7 sink current	6-9	10			mA	V_{OUT} = 0.7V
P4-P7 leakage current	6-9			10	μA	V_{OUT} = 13.2V
Input Port						
P3 Input current high	10			+10	μA	$V_{pin\ 10}$ = 5.5V
P3 Input current low	10			-10	μA	$V_{pin\ 10}$ = 0V

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V.

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Supply voltage	12	-0.3	7	V	
RF input voltage	13, 14		2.5	Vp-p	
Port voltage	6 - 10	-0.3	14	V	Port in off state
	6 - 9	-0.3	6	V	Port in on state
	10	-0.3	14	V	Port in on state
Total port output current	6-10		50	mA	
RF input DC offset	13, 14	-0.3	$V_{CC}+0.3$	V	
Charge pump DC offset	1	-0.3	$V_{CC}+0.3$	V	
Drive DC offset	16	-0.3	$V_{CC}+0.3$	V	
Crystal oscillator DC offset	2	-0.3	$V_{CC}+0.3$	V	
SDA, SCL input voltage	4, 5	-0.3	$V_{CC}+0.3$	V	With V_{CC} applied
		-0.3	5.5	V	V_{CC} not applied
Storage temperature		-55	+125	°C	
Junction temperature			+150	°C	
Thermal resistance, chip-to-ambient			111	°C/W	
Thermal resistance, chip-to-case			41	°C/W	
Power consumption at 5.5V			275	mW	All ports off

FUNCTIONAL DESCRIPTION

The SP5514S is programmed from an I²C BUS. The data is fed in on the SDA line and clock on the SCL line as dictated by the I²C BUS format at an increased clock rate of 0.5MHz. The Tables in Fig 3 illustrate the format of the data in write mode. The device can be programmed to respond to several addresses. This enables the use of more than one synthesiser in an I²C BUS system. Table 2 shows how the address is selected by applying a voltage to P3. The last bit of the address Byte R/W must be set to 0 for correct write operation. When the SP5514S receives a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed.

Once the correct address is received and acknowledged the first bit of the next byte determines whether that byte is interpreted as byte 2 or 4. A logic 0 for byte 2, frequency information and 1 for byte 4, control information. Byte 2 must be followed by byte 3 or STOP; similarly byte 5 follows byte 4. Until an I²C BUS stop condition is recognised, additional data Bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid byte (e.g. by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15 Bit shift register and is used to control the division ratio of the 15-Bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is shown in Fig. 7.

When frequency data is entered, the phase comparator, via the charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the 7.8125kHz reference obtained by dividing the output of the 4MHz crystal oscillator by 512.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit a logic 1 for $\pm 170\mu A$ and a logic 0 for $\pm 50\mu A$ allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects P6 to F_{comp} and P7 to F_{div}.

Byte 5 programs the output ports P3 to P7 a logic 0 for a high impedance output, a logic 1 for low impedence (on). When any of the optional addresses are used P3 must be programmed in its high impedance state.

APPLICATION

A typical application is shown in Fig. 4. All interface circuitry is shown in Fig. 6.

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	**BYTE 1**
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**BYTE 2**
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**BYTE 3**
CHARGE PUMP AND TEST BITS	1	CP	T1	T0	1	1	1	OS	A	**BYTE 4**
IO PORT CONTROL BITS	P7	P6	P5	P4	P3	X	X	X	A	**BYTE 5**

Table 1 write data format (MSB is transmitted first)

A : Acknowledge Bit
MA1, MA0 : Variable address bits (see table 2)
CP : Charge Pump Current Select
T1 : Test Mode Selection
T0 : Charge Pump Disable
OS : Varactor Drive Output Disable Switch
P7, P6, P5, P4, P3, : Control Output States
X : DONT CARE

MA1	MA0	Voltage input to P3
0	0	0-0.2V_{CC}
0	1	ALWAYS VALID
1	0	0.3-0.7V_{CC}
1	1	0.8V_{CC}-13.2V

Table 2 Address selection

Fig.3 Data formats

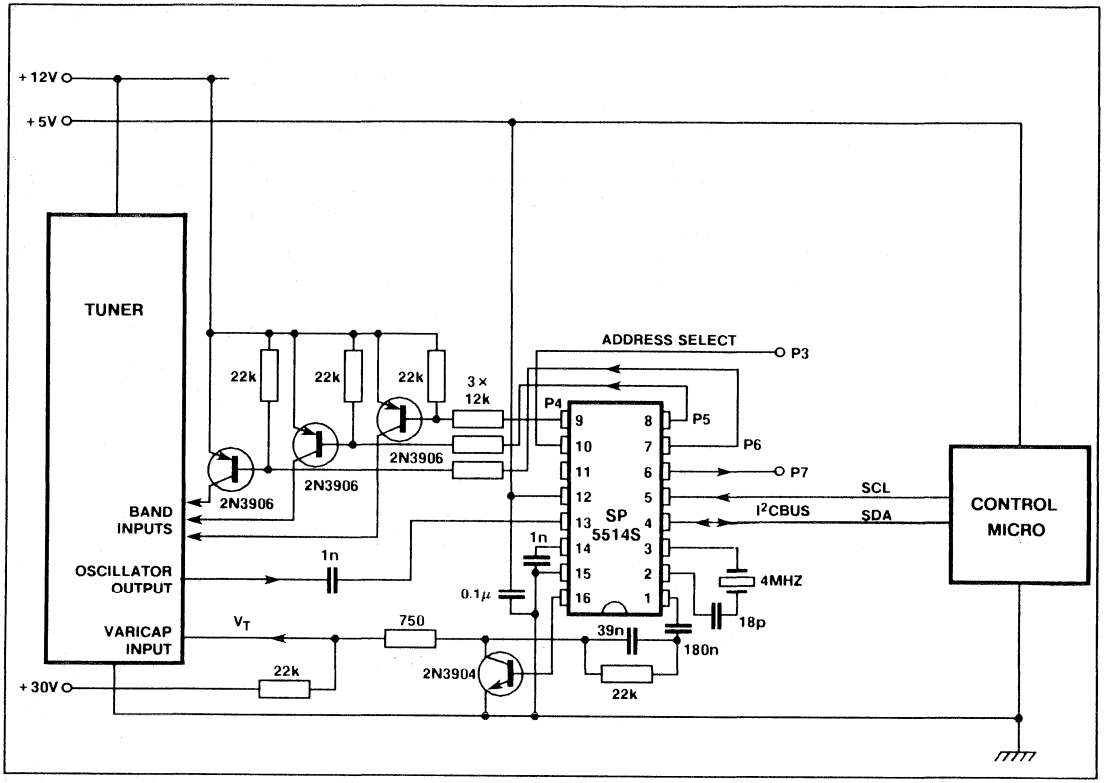


Fig.4 Typical SP5514S application

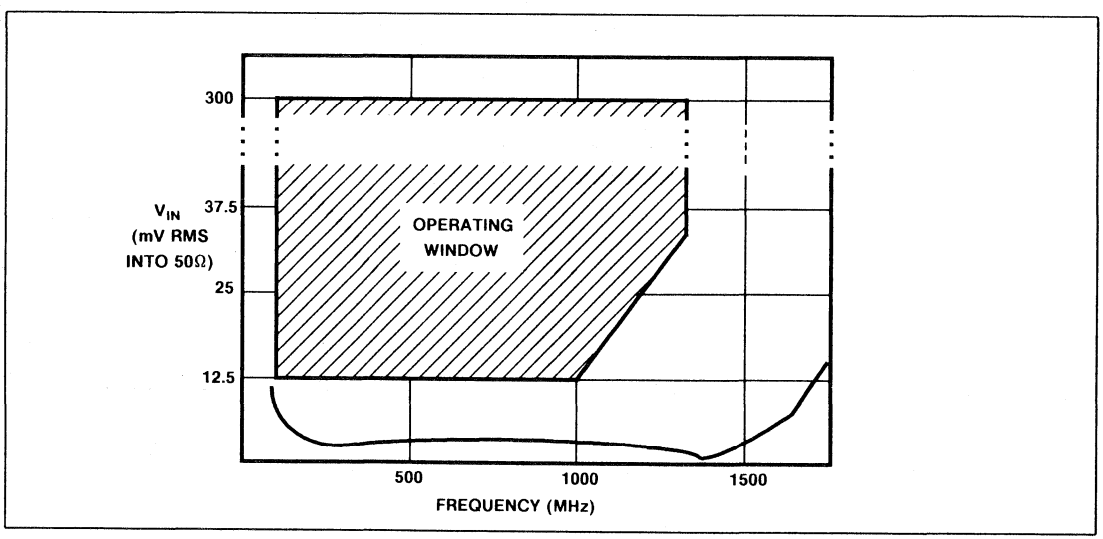
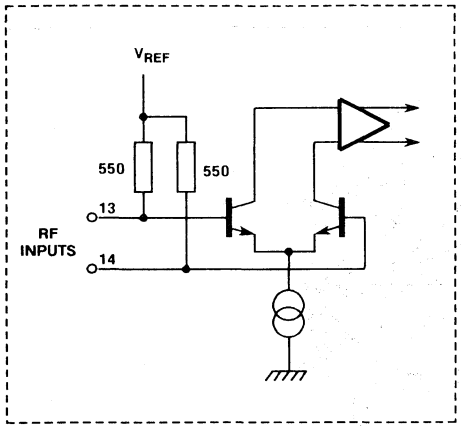
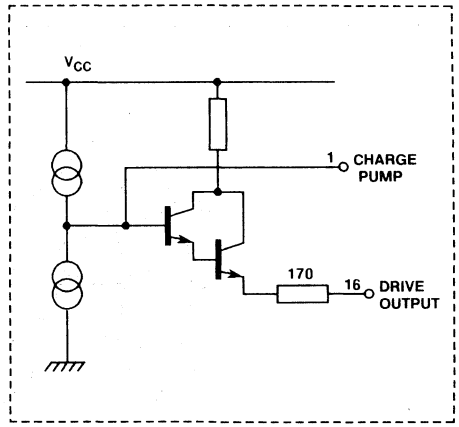


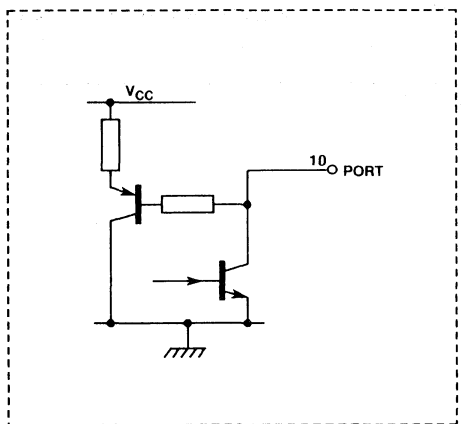
Fig.5 Typical input sensitivity



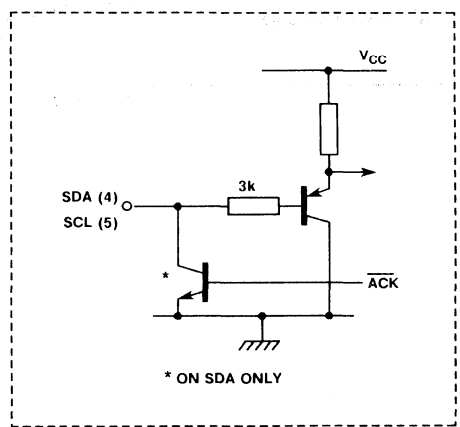
RF input



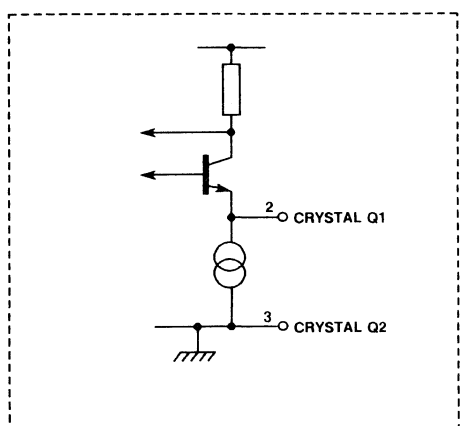
Loop amplifier



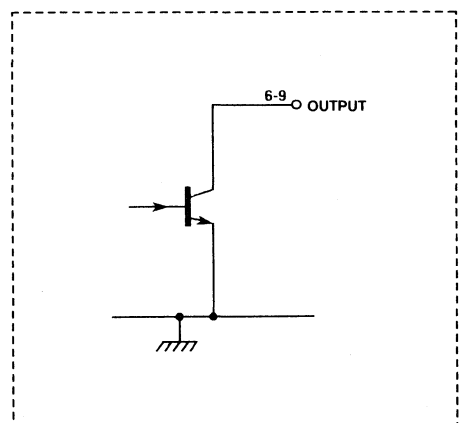
Port P3



SCL and SDA input



Reference oscillator



Ports P7-P4

Fig.6 SP5514S input/output interface circuits

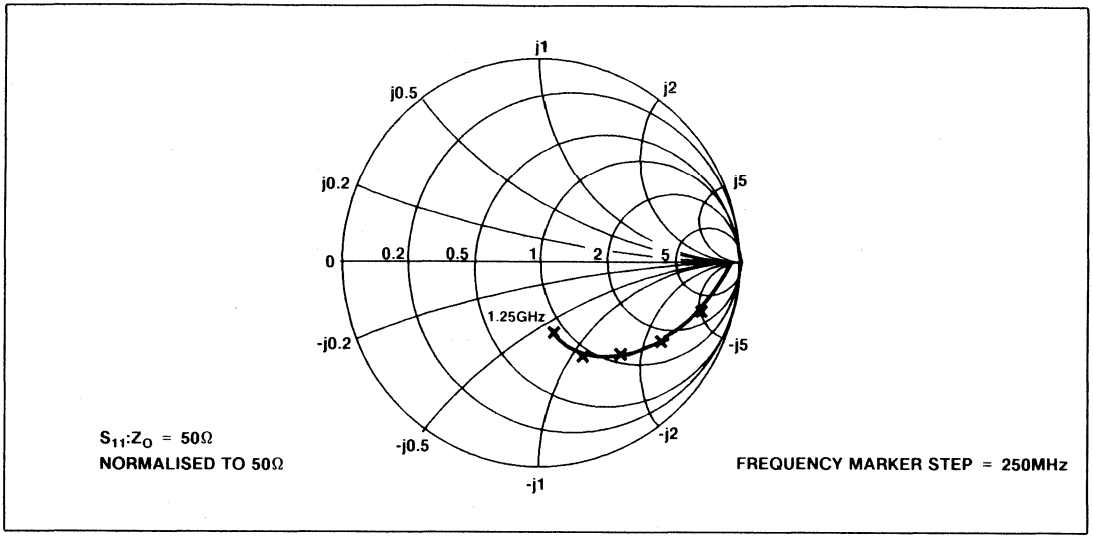


Fig.7 Typical input Impedance SP5514S

SL5066

VIDEO MODULATOR

The SL5066 is a video up converter, able to operate up to 900MHz. It is compatible with all video standards PAL, NTSC and SECAM - accepting baseband video and sound inputs and modulating up to any desired VHF or UHF channel.

Output drive is directly into 75Ω. Prescaler outputs are also provided enabling the use of a synthesiser to control oscillator frequency. The SL5066 operates from a 5V supply.

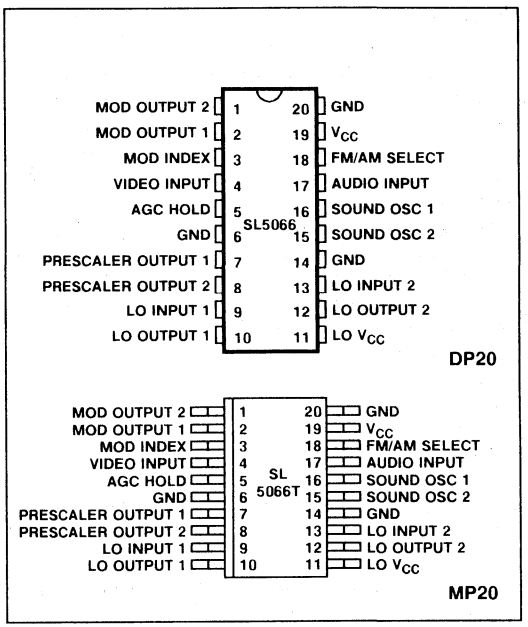


Fig.1 Pin connections - top view

FEATURES

- 5V Operation
- Symmetrical RF Oscillator Operating up to 900MHz
- Symmetrical RF drive to a frequency synthesiser
- Video Signal Input Clamp
- Video Peak White Level Detection and Automatic Gain Control
- Negative and Positive Video Modulation
- Control of Video Modulation Index
- Direct Drive into 75Ω, via Symmetrical Outputs
- FM and AM Sound
- Control of Sound Modulation Index
- Picture Carrier to Sound Carrier Ratio Adjustment
- Low Radiation
- Good Oscillator Stability
- Low External Component Count
- Full ESD Protection *

* Normal ESD handling procedures should be observed.

APPLICATIONS

- Video Recorders
- Cable Systems
- Video Cameras
- Personal Computers
- Video Security Systems
- Cableless In-home Video Distribution (LPTV)

ORDERING INFORMATION

SL5066 DP - (20 lead DIL Plastic Package)
SL5066T MP - (20 lead Miniature Plastic Package)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = -10 to +80°C, V_{CC} = 4.5 to 5.5V

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	11,19	4.5		5.5	V	
Supply current	11,19		51		mA	
LO prescaler output level	7,8		10		mV RMS	Single ended into 50Ω
LO Prescaler output impedance	7,8		50		Ω	
LO drift with temp. from switch-on	10,12		70		kHz	See Note 1
LO variation with supply	10,12		330		kHz	See Note 1, V_{CC} = 4.5V to 5.5V
RF carrier output level	1,2		80		dBμV	Single ended into 75Ω
Video Input	4	0.5	1.0	1.5	V p-p	
Video mod index	1,2		73		%	See Note 2
Video Signal/Noise Ratio	1,2		59		dB	Weighted PAL 200kHz to 5.5MHz
Sound Subcarrier temp. drift from switch-on	15,16		4		kHz	See Note 1
Sound drift with supply	15,16		2.5		kHz	V_{CC} = 4.5V to 5.5V } L = 20μH, f_S = 6MHz
Sound IF shift on switch from FM to AM	15,16		20		kHz	See Note 1
Audio input impedance	17		25		kΩ	
Audio input voltage reference	17		2		V	
Audio input level	17			2	V p-p	
FM THD	1,2		0.1		%	Q = 3, Δf = ± 20kHz
AM THD	1,2		0.3		%	V_{AUDIO} = 880mV p-p
Picture/sound carrier ratio (FM)	1,2		11.5		dB	R = 0, See Note 3
Sound oscillator FM deviation	1,2		70		kHz/V	C = 150pF, L = 4.7μH (Q_L = 10)

NOTES

1. Including external component effects
2. May be increased by use of external resistor, see Fig.3
3. May be adjusted by use of external resistor, see Fig.4

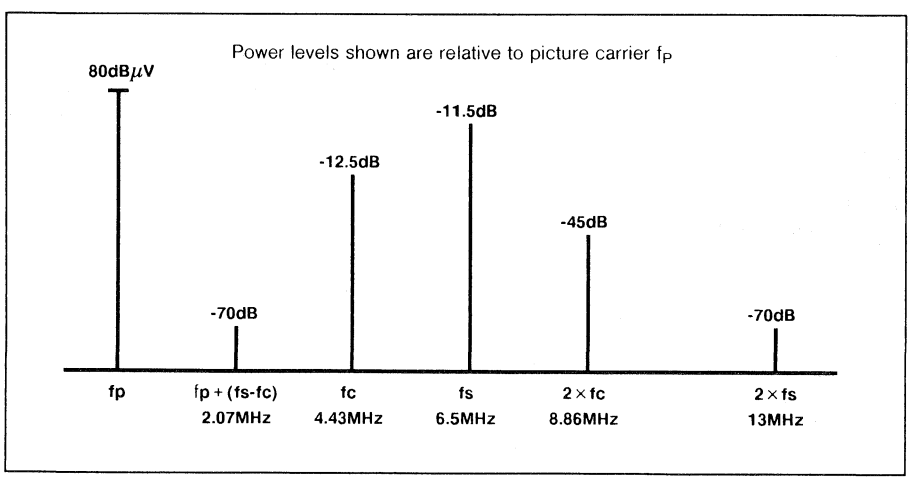


Fig.2 Frequency spectrum above the picture carrier

VIDEO

The Video signal is applied to pin 4 via a coupling capacitor (see Fig. 7). This capacitor provides both clamping and black level hold. The internal peak white AGC can cope with an input signal of between 0.5 and 1.5 Volts peak to peak. The full 9.5dB AGC range is handled within a 600mV span on this storage capacitor.

Pin 3 (MOD INDEX) determines whether the modulation is either positive or negative and also sets the modulation index.

For negative modulation (PAL) with an 80% modulation index, pin 3 should be connected directly to ground. For positive modulation with an 80% modulation index, pin 3 should be connected to V_{CC}.

In both cases, the modulation index is increased by connecting a resistor between pin 3 and either ground or V_{CC} depending on type of modulation desired, see Fig 3.

AUDIO

The sound IF oscillator can operate from 4.5MHz to 6.5MHz to cover all sound standards. The centre frequency is determined by the sound IF tank LC connected between pins 15 and 16.

The centre frequency is given by:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

The Q factor of the tank is given by:

$$Q = \frac{1770}{2\pi f_0 L} = 1770 \times 2\pi f_0 C$$

The Q factor of the inductor must be high, i.e., >20
A graph of FM deviation v. C_{TANK} is given in Fig. 11.

Good temperature stability can be achieved by the correct choice of temperature coefficients for C_{AUDIO} and L_{AUDIO}.

The audio signal should be coupled into pin 17 via a 470nF capacitor. The maximum input level is 2V peak-to-peak. For AM, the input must consist of an AC signal with a DC offset. The ratio of the AC peak to voltage to the DC offset determines the AM index.

The DC offset is given by:

$$DC_{OFFSET} = \frac{2 \times 25}{25 + R_{AM}} \text{ V, with } R_{AM} \text{ in k}\Omega$$

For the example given in the application diagram (Fig. 12) a value of 68kΩ is used for R_{AM}. This gives a DC offset of 540mV. An audio input of 880mV peak-to-peak (440mV peak) thus gives an AM index of 80%.

Selection of AM or FM sound is made via pin 18 (FM/AM select). For FM, the pin should be connected to ground via a resistor. For AM, the pin should be connected to V_{CC}. The value of the resistor will determine the Picture Carrier to Sound Carrier Ratio. For the FM case see Fig.4

MODULATED RF OUTPUT

The RF output drive from pins 1 and 2 is designed to drive directly into a 75Ω load. Output drive level is 80μV single ended into 75Ω.

LOCAL OSCILLATOR

The local oscillator is able to operate up to 900MHz enabling the SL5066 to be used over all VHF and UHF channels. By careful choice of components and layout it is possible to tune over an octave using a fixed inductor.

Good isolation between the local oscillator and the modulated RF outputs is required to prevent signal coupling and affecting apparent modulation index. This is best performed by the use of a ground plane to cut down radiation.

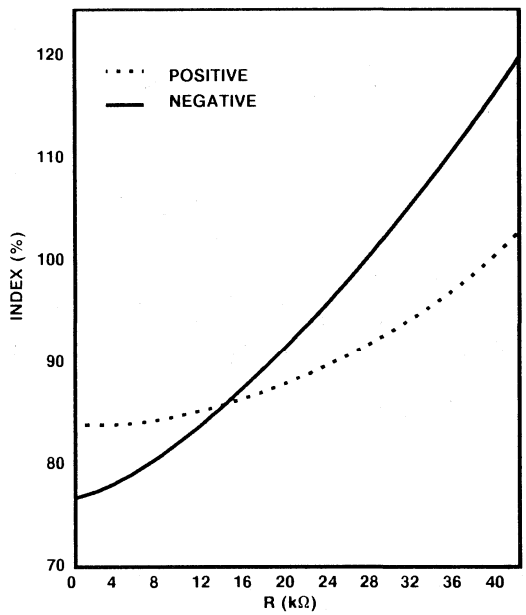


Fig.3 Typical video modulation Index (SL5066)

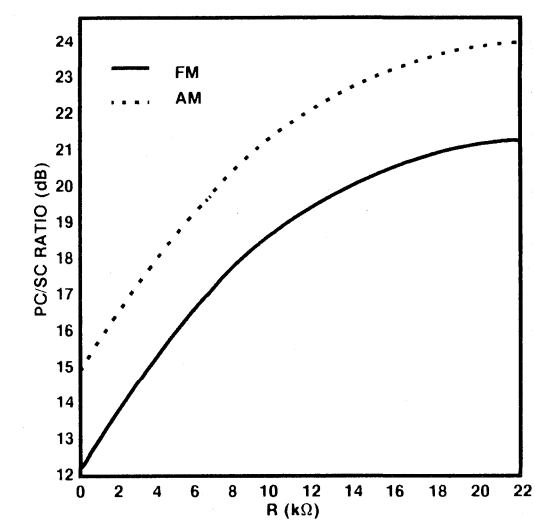


Fig.4 Typical picture/sound carrier ratio (SL5066)

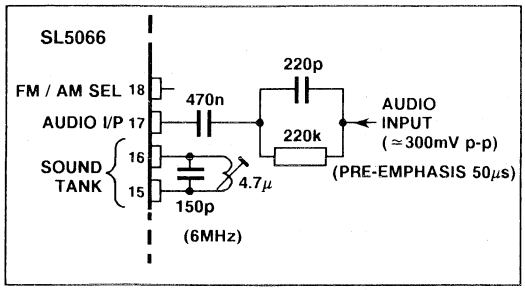


Fig.5 Typical FM sound section

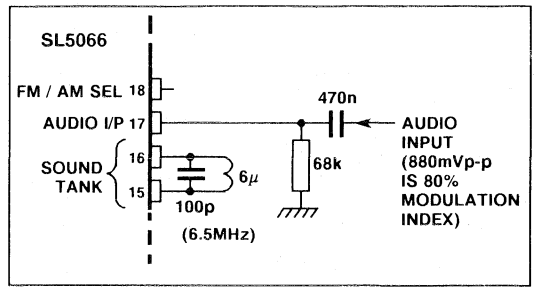


Fig.6 Typical AM sound section

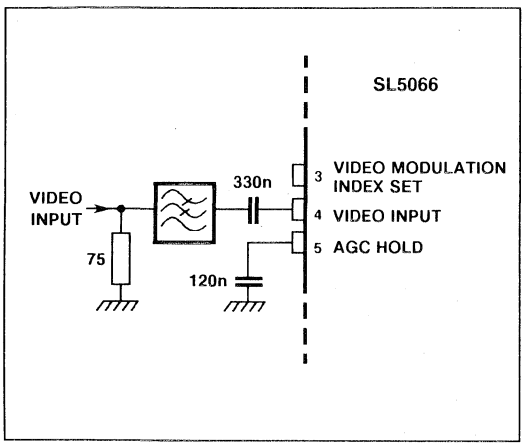


Fig.7 Video input

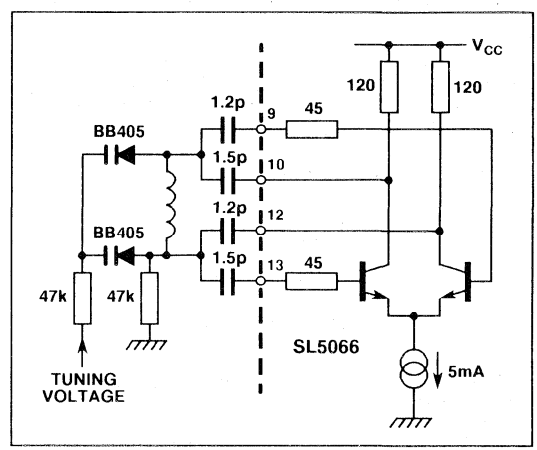


Fig.8 RF oscillator

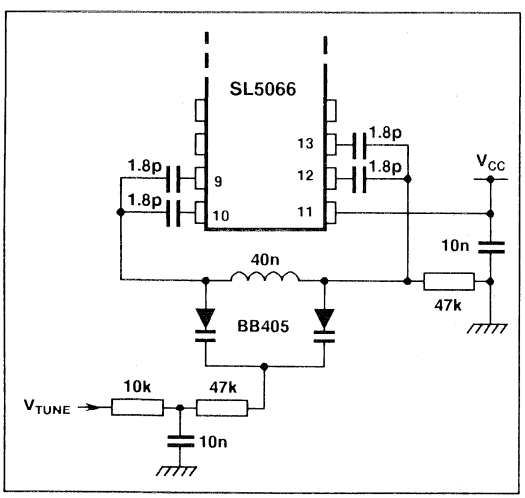


Fig.9 Test circuit

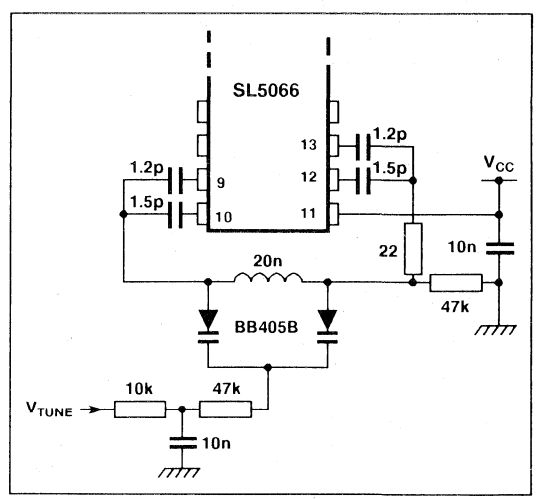


Fig.10 UHF application

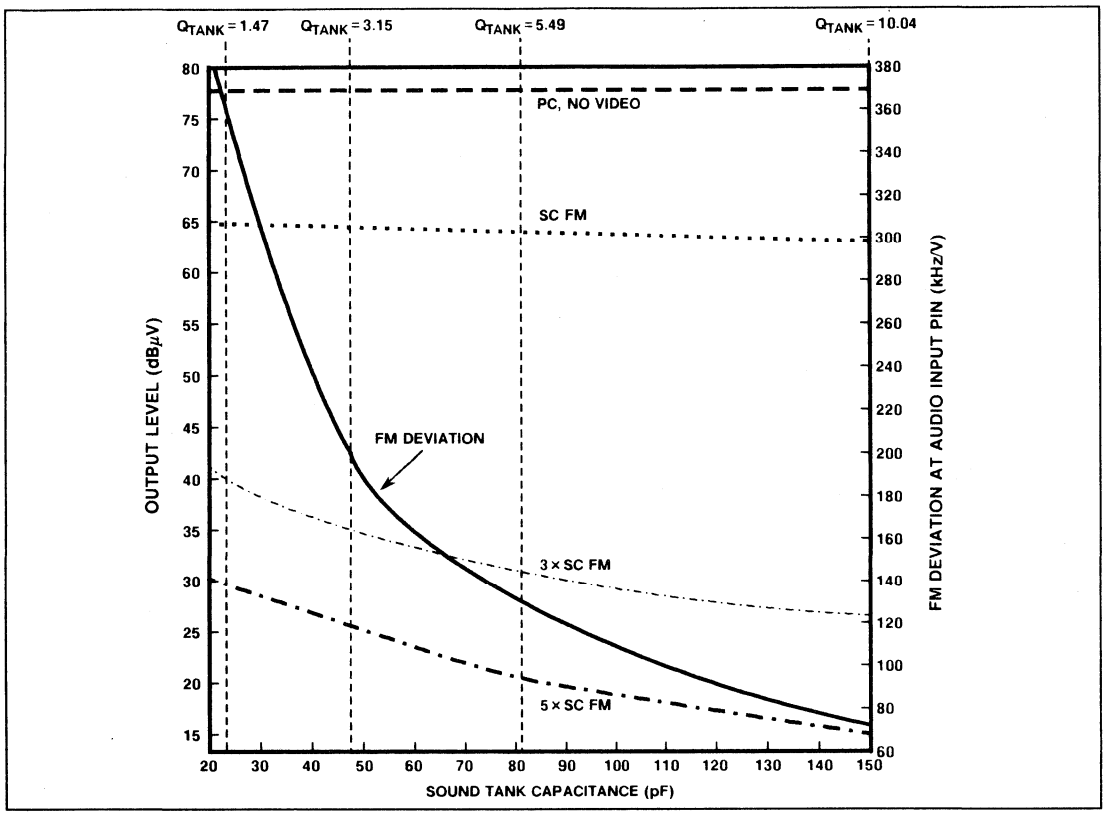


Fig.11 Sound oscillator harmonics and FM deviation v. tank capacitance (f_{SOUND} = 6.0MHz)

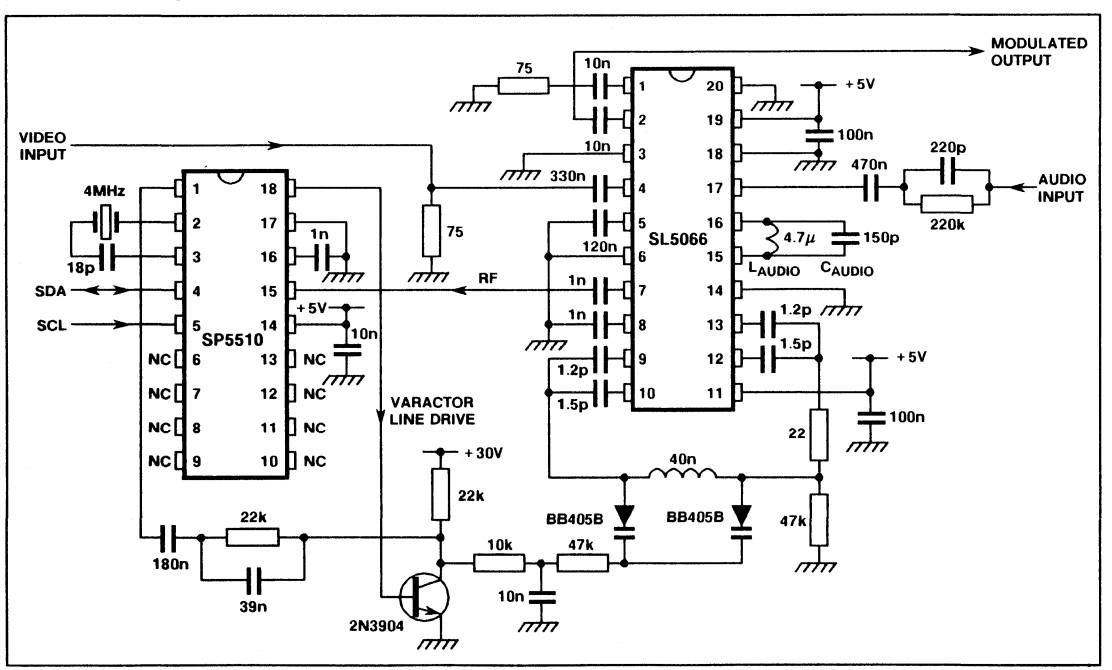


Fig.12 Typical application showing video modulator with synthesised oscillator

Section 2

Satellite TV Receiver Circuits

2042-1.0

SL1451

WIDEBAND PLL FM DETECTOR FOR SATELLITE TV

The SL1451 EXP is a phase locked loop demodulator for use in wideband FM systems. It is intended for use with an IF input frequency from 300MHz to 700MHz in satellite receivers. It consists of an input RF amplifier, signal level detector, UHF phase detector, UHF oscillator and video/loop amplifier. Both positive and negative going video outputs are available.

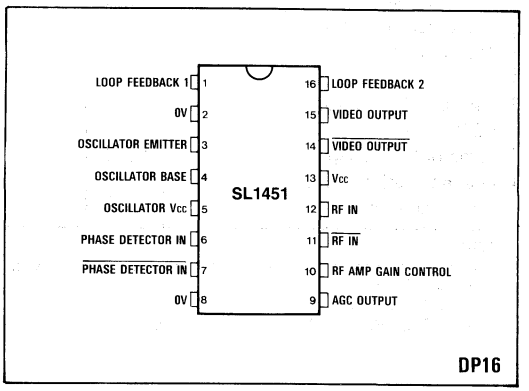


Fig.1 Pin connections - top view

FEATURES

- Complete PLL System for Wideband FM Demodulator
- 8dB Noise Threshold Performance Typical
- Low External Component Count
- Positive and Negative Going Video Output Available
- Demodulates FM Signals with up to 28MHz Pk to Pk Deviation

APPLICATIONS

- DBS Receivers
- Wideband Data Communications Demodulation

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**-10° C to 80° C**
Supply voltage	11V
Storage temperature range	-55° C to 125° C
Junction temperature	+175° C

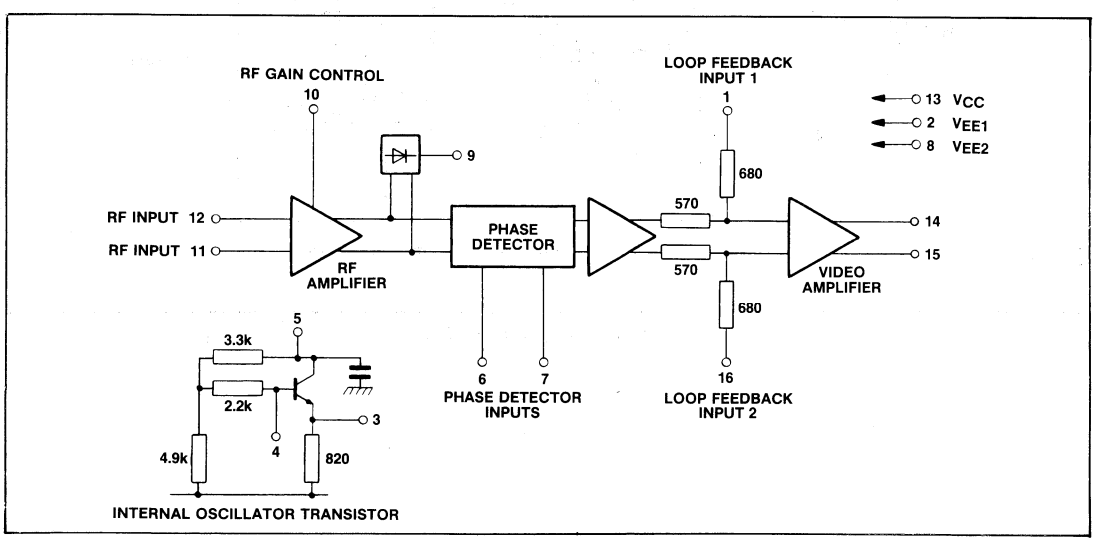


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C V_{CC} = 7.4V to 9V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	13,5	40	55	70	mA	
Supply voltage	13,5	7.4	8.2	9	V	
Minimum oscillator frequency			300		MHz	
Maximum oscillator frequency			700		MHz	
Phase detector input level						
from oscillator	6,7	400	70	100	mV	
RF input level	11,12	12.5	40	125	mV	
Phase detector gain			0.5		V/Radian	
AGC output	9		300		μA	No input signal
			140		μA	-20dBm input signal
Oscillator lock range			50		MHz	See Note 1
VCO slope			14		MHz/V	
Video output voltage	14,15		1.5		Vt pk to pk	21.4MHz pk to pk deviation
Intermodulation products			-40		dBm	See Note 2
Video bandwidth			18		MHz	

NOTES
1. All characteristics from oscillator lock range to video bandwidth are determined by the application circuit. These results were gained with the circuit in Fig.3.
2. Signal 1 4.433MHz Deviation = 21.4MHz pk-pk
   Signal 2 6MHz Deviation = 3MHz pk-pk

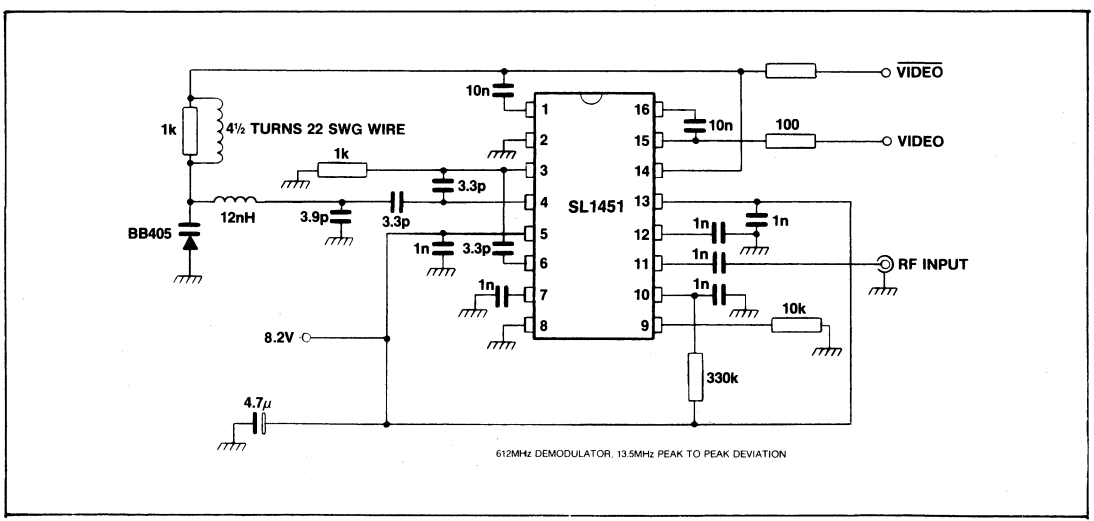


Fig.3 Typical application circuit

2029-1.0

SL1452

WIDEBAND LINEAR FM DETECTOR FOR SATELLITE TV

With a minimum of external components, the SL1452 forms a complete wideband FM detector suitable for use in satellite TV. The video output voltage and bandwidth may be optimised by adjustment of the working Q of the quadrature coil. The device features electrostatic protection on all pins.

FEATURES

- High Operating Frequency Simplifies Image Filtering
- Excellent Threshold
- Negligible Differential Gain and Phase Errors
- Video Bandwidth Suitable for High Definition TV
- High Sensitivity and Wide Dynamic Range
- Wide operating frequency range 300 to 1000MHz

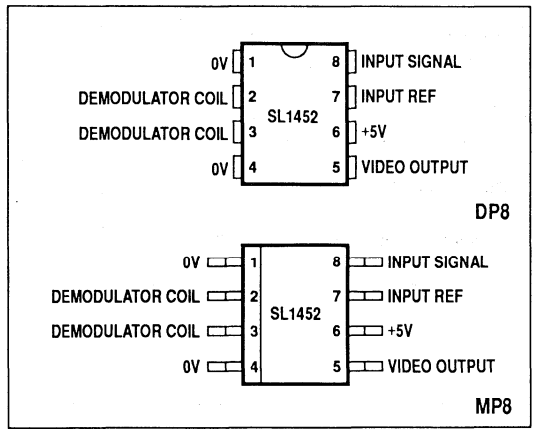


Fig.1 Pin connections - top view (not to scale)

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**-10°C to +80°C**
Storage temperature	-55°C to +125°C
Supply voltage Pin 6	7V
Input voltage Pin 7 or 8	2.5V p-p
Junction temperature	+175°C

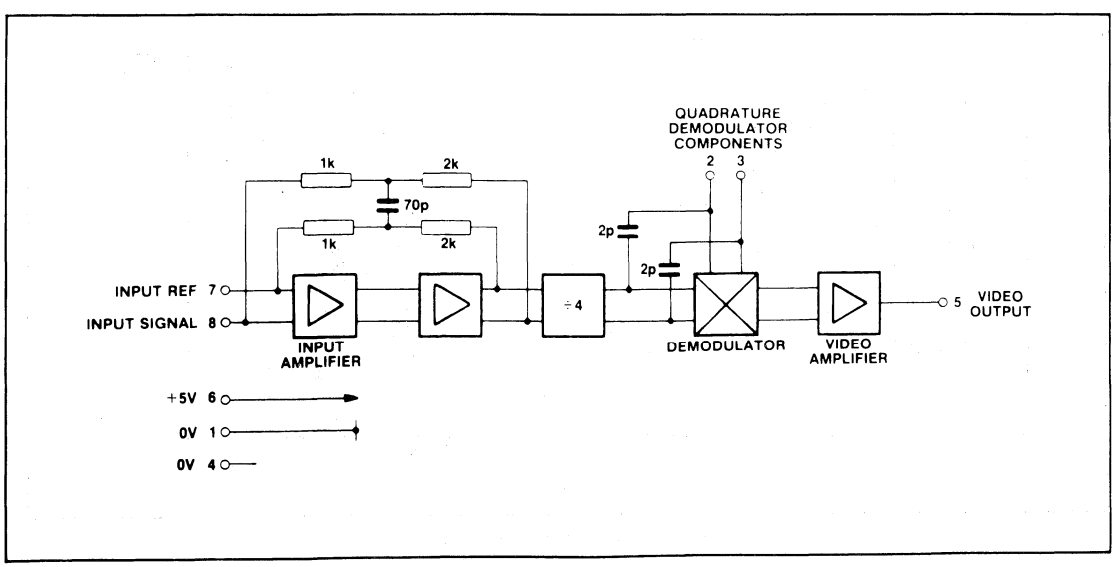


Fig.2 SL1452 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = +25°C; Vcc = +4.5V to +5.5V; Q = 6 f = 612MHz

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current Ic	6		40	50	mA	Vcc = 5V
Video output voltage	5		0.7		V p-p	Δf = 13.5MHz p-p
Video bandwidth	5		14		MHz	
Minimum operating frequency	8		300		MHz	
Maximum operating frequency	8		1000		MHz	
Input voltage	8	10		300	mV rms	
Intermodulation	5		-60		dB	product of input modulation f = 4.4MHz Δf = 13.5MHz p-p and f = 6MHz Δf = 2MHz p-p (PAL colour and sound subcarriers)
Differential gain	5		<±1%			Δf = 13.5MHz p-p. Demodulated staircase referred to input staircase before modulation
Differential phase	5		<±1		deg	demodulated colour bar waveform referred to waveform before modulation
Signal to noise ratio	5	70			dB	ratio of output with Δf = 13.5MHz p-p at 1MHz to output rms noise in 10MHz bandwidth with Δf = 0

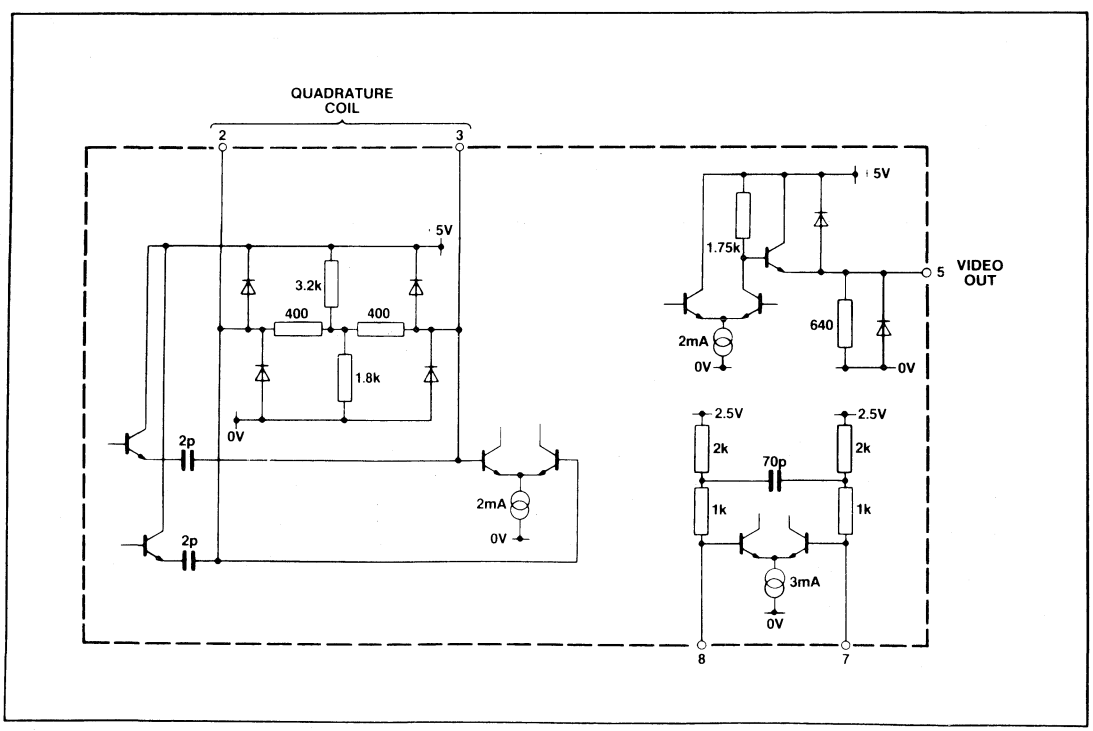


Fig.3 Input output interface circuits

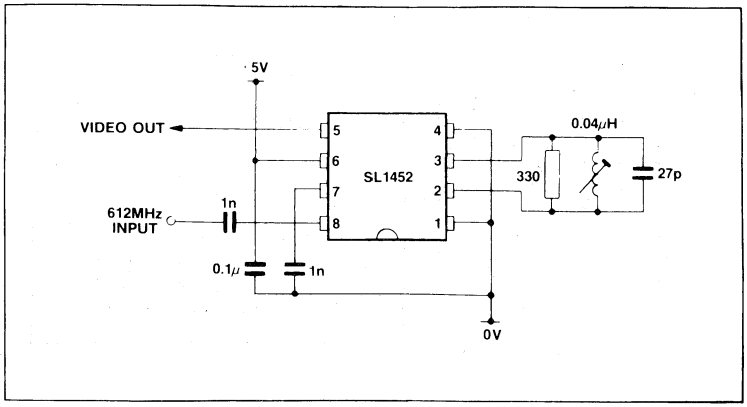


Fig.4 Typical application

SL1452 QUADRATURE DEMODULATOR

The SL1452 FM demodulator has a simple application with very low external component count. This is demonstrated by the applications circuit diagram Fig.4, but as with most integrated circuits, particularly those working at high frequencies, some attention to good RF layout techniques and correct component selection will ensure optimum results.

A good layout can usually be ensured by the simple precaution of keeping all components close to the SL1452, maintaining short lead lengths and ensuring a good low impedance ground plane. Double sided board layout enables these objectives to be easily met, but is not essential for satisfactory operation. All coupling and decoupling capacitors should be chosen for low impedance characteristics at high frequencies: multilayer ceramic types usually providing small size and adequate high frequency performance. For the quadrature coil tuning capacitor a fairly stable component should be selected to prevent excessive drift. The power supply decoupling capacitor from pin 6 to ground should be 0.1μF minimum but the input coupling and decoupling values can be smaller, about 330pF being adequate.

The only remaining components to be selected are those forming the quadrature circuit on pins 2 and 3 and some care in the determination of values for these is required if maximum performance is to be obtained.

First determine the quadrature circuit operating frequency, which is a quarter of the input frequency on pin 8 due to the two internal divide by 2 circuits (see Fig.2).

Choose suitable values for L and C to resonate at the correct frequency using:

$$f = \frac{1}{2\pi\sqrt{(LC)}}$$

The value of C should be greater than 15pF to prevent stray capacitance effects introducing errors and distortion of the demodulation curve, but the use of very large capacitances with small inductance values will lower the impedance of the tuned circuit at the required Q value, reducing the drive level to the demodulator and thereby restrict the video output available. In general for operation in the 400 to 600MHz range, an inductance value between 40 and 60nH is recommended.

Once suitable L and C values have been determined, the working Q for the quadrature circuit should be set, the Q value determining the video output level and bandwidth. Video output is proportional to Q whereas video bandwidth is inversely proportional. The effect of Q variations on video bandwidth and amplitude can be determined from Table 1 and the graphs in Fig.5.

A value for total damping resistor value to obtain the required Q can be calculated from:

$$R = Q2\pi fL$$

The internal 800 resistor between pins 2 and 3 must be allowed for when calculating R.

Example

Design a quadrature circuit to demodulate a carrier on pin 8 with centre frequency 480MHz and video bandwidth of 10MHz.

For L = 40nH and f_{quad} = 120MHz,
C = 43.98pF (nearest preferred value 47pF)
From Table 1, Q required is approximately 6
therefore total R required is:

$$R = Q2\pi fL$$

$$= 6 \times 2 \times \pi \times \frac{480}{4} \times 10^6 \times 0.04 \times 10^{-6}$$

$$= 181 \text{ ohms}$$

allowing for the internal 800 ohm resistance between pins 2 and 3 (see Fig.3), the external resistance required is 234 ohms. Choose 270 ohms.

It should be remembered that the internal 800 ohm resistance is subject to production tolerances and if fairly close control of video bandwidth is required, the L and C ratio may require some adjustment to ensure that the external R is sufficiently low to swamp the effect of internal resistance changes. The value of 270 ohms obtained in the example is low enough to allow adequate control.

In order to overcome the effects of component tolerances, it will usually be necessary to make either the L or C a variable component, the value being adjusted to obtain best linearity.

Q	BANDWIDTH
10	7.5MHz
6	14MHz
4	23MHz

Table 1

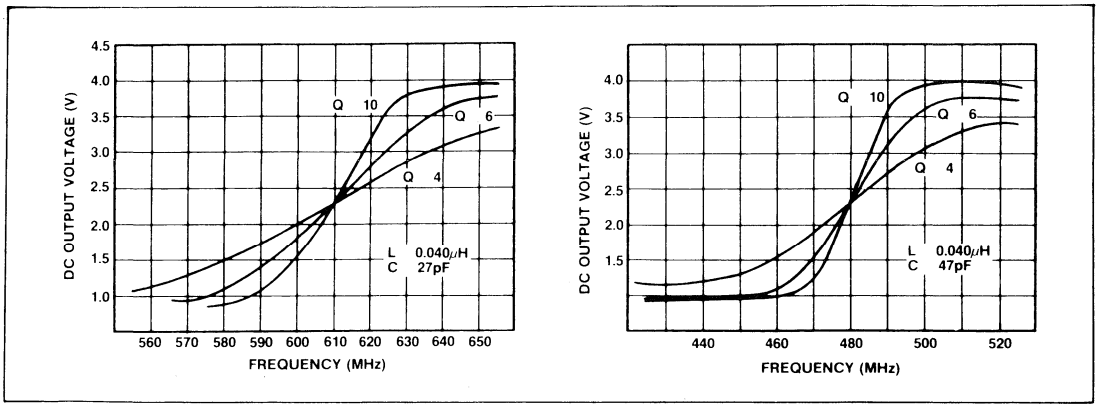


Fig.5 Output voltage versus input frequency

2039-1.0

SL1454

WIDEBAND LINEAR FM DETECTOR FOR SATELLITE TV

The SL1454 is a wideband FM demodulator designed to operate with a carrier frequency between 70 and 150MHz. The internal circuitry of the device is similar to that of the SL1452 except that the quadrature demodulator is working at the input frequency.

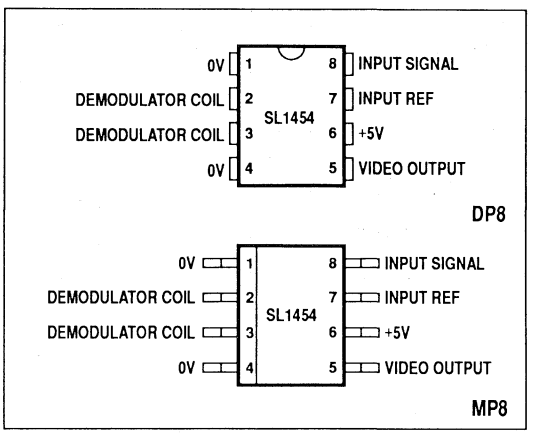


Fig.1 Pin connections - top view (not to scale)

FEATURES

- Excellent Threshold
- Negligible Differential Gain and Phase Errors
- Video Bandwidth Suitable for High Definition TV
- High Sensitivity and Wide Dynamic Range
- Wide Operating Frequency Range 70 to 150MHz

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**-10°C to +70°C**
Storage temperature	-55°C to +125°C
Supply voltage Pin 6	7V
Input voltage Pin 7 or 8	2.5V p-p
Junction temperature	+175°C

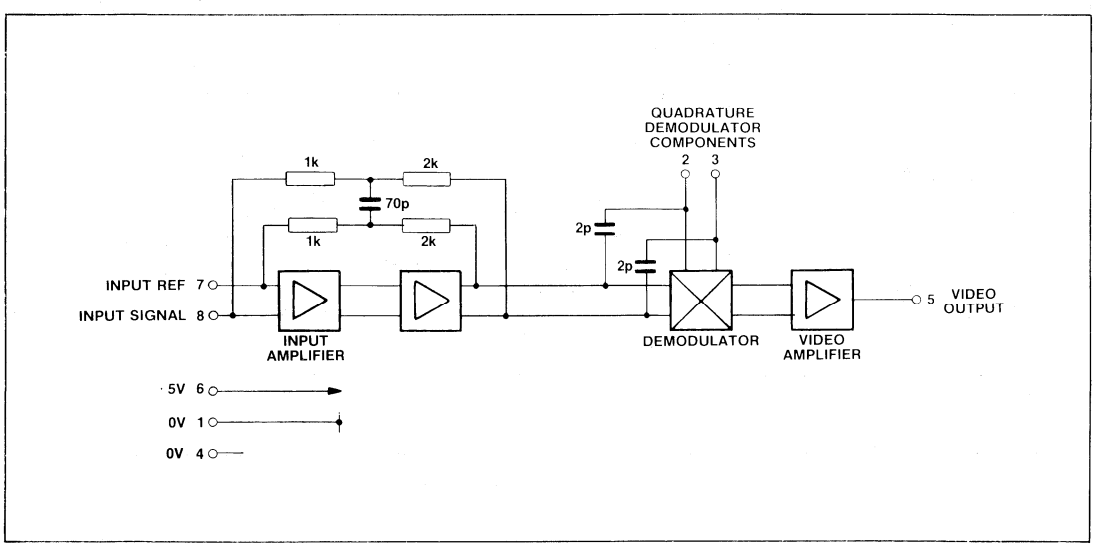


Fig.2 SL1454 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C; V_{CC} = +4.5V to +5.5V; Q = 2; f = 140MHz

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current Ic	6		30	35	mA	V_{CC} = 5V
Video output voltage	5		0.4		V p-p	Δf = 21.4MHz p-p
Video bandwidth	5		10		MHz	
Minimum operating frequency	8		70		MHz	
Maximum operating frequency	8		150		MHz	
Input voltage	8	10	5	300	mV rms	
Intermodulation	5		-50		dB	product of input modulation f = 4.4MHz Δf = 21.4MHz p-p and f = 6MHz Δf = 3MHz p-p (PAL colour and sound subcarriers)
Differential gain	5		<±2		%	Δf = 21.4MHz p-p. Demodulated staircase referred to input staircase before modulation
Differential phase	5		<±2		deg	demodulated colour bar waveform referred to waveform before modulation
Signal to noise ratio	5	70			dB	ratio of output with Δf = 21.4MHz p-p at 1MHz to output rms noise in 10MHz bandwidth with Δf = 0

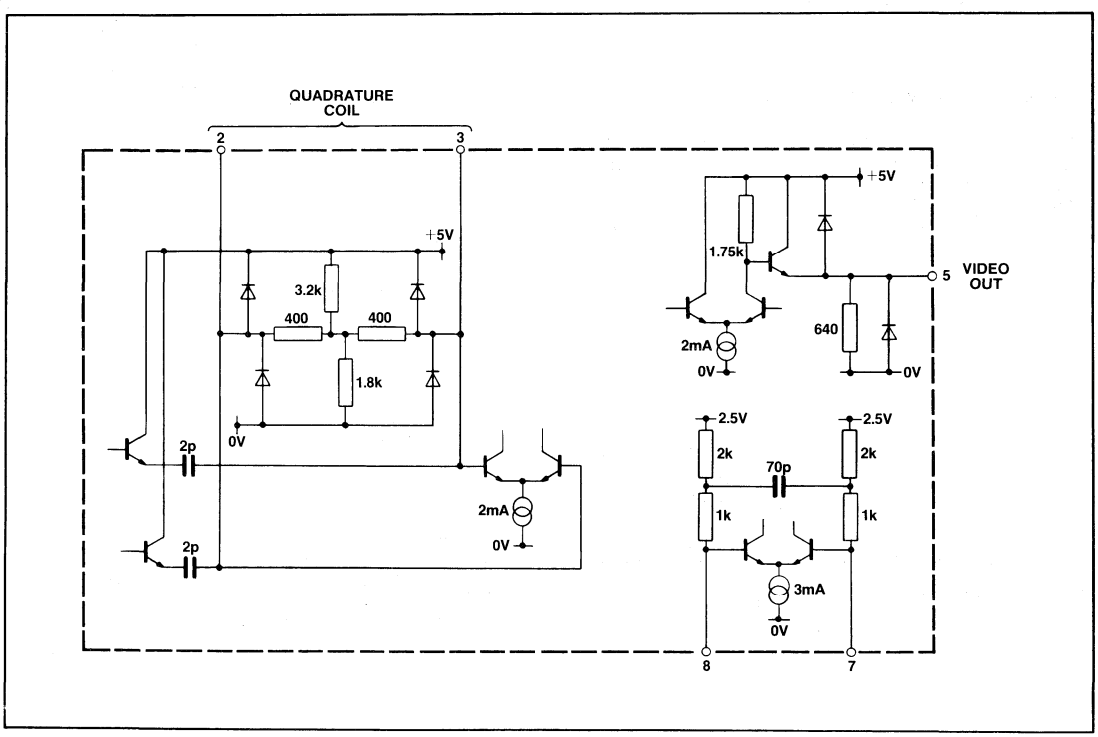


Fig.3 Input/output interface circuits

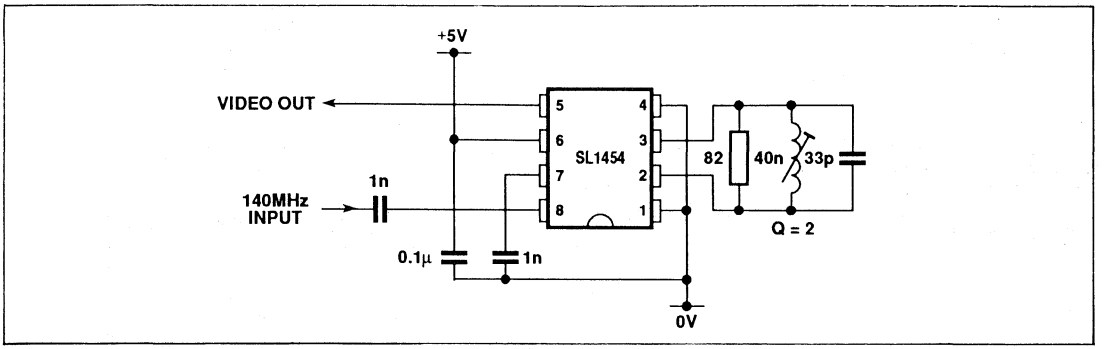


Fig.4 Typical application for 140MHz

APPLICATION NOTES

The SL1454 FM demodulator has a very simple application with very low external component count. This is demonstrated by the applications circuit diagram Fig.4, but as with most integrated circuits, particularly those working at high frequencies, some attention to good RF layout techniques and correct component selection will ensure optimum results.

A good layout can usually be ensured by the simple precaution of keeping all components close to the SL1454, maintaining short lead lengths and ensuring a good low impedance ground plane. Double sided board layout enables these objectives to be easily met, but is not essential for satisfactory operation. All coupling and decoupling capacitors should be chosen for low impedance characteristics at high frequencies. A fairly stable component should be selected for the quadrature coil tuning capacitor to prevent excessive drift. The power supply decouplng capacitor from pin 6 to ground should be 0.1μF minimum, but the input coupling and decoupling values can be smaller, about 1nF being adequate.

The only remaining components to be selected are those forming the quadrature circuit on pins 2 and 3 and some care in the determination of values for these is required if optimum performance is to be obtained.

Choose suitable values for L and C to resonate at the intermediate frequency you are applying to the device using:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

The value of C should be greater than 15pF to prevent stray capacitance effects introducing errors and distortion of the demodulation S curve, but the use of very large capacitances with small inductance values will lower the impedance of the tuned circuit at the required Q value, reducing the drive lead to the demodulator and thereby restrict the video output available.

Once suitable values for L and C have been determined, the working Q for the quadrature circuit should be set, the Q value determining the video output level and bandwidth. Video output is proportional to Q whereas video bandwidth is inversely proportional. The effect of Q variations on video bandwidth and amplitude can be determined from Table 1 and the graphs in Fig.5.

A value for total damping resistor value to obtain the required Q can be calculated from:

$$R = Q2\pi fL$$

The internal 800Ω resistor between pins 2 and 3 must be taken into account when calculating R.

As can be seen from the graphs in Fig.5 for the demodulator to be demodulate a 20MHz peak to peak deviation signal with optimum linearity a very low Q value needs to be chosen (<2). But this has the disadvantage of producing a demodulator with a very low peak to peak video output level.

One way of increasing the linear region of the S curve without reducing the video output level is to incorporate a dual tuned circuit in the quadrature network. This can easily be done by capacitatively coupling another parallel tuned circuit to the normal quadrature tuned circuit.

Fig.6 shows an example of this form of dual tuned circuit, both sections have the same Q factor and the coupling capacitors are chosen to give the best linearity (Linear phase response). Fig.5(b) shows the advantages of the dual tuned circuit. The effect of varying the Q factor of the dual tuned circuit on bandwidth is also described by Table 1.

Example

Design a quadrature circuit to demodulate a 140MHz carrier with 21.4MHz peak to peak deviation, modulated with a 25Hz triangular dispersion waveform of 2MHz peak to peak deviation. The video bandwidth required is 9MHz.

Choose L = 40nH
then C = 32.309pF (nearest preferred value 33pF)

The next value to choose is the Q factor. As dispersion is employed linearity over the full 21.4MHz range needs to be optimised. The graphs in Fig.5 show that either a single tuned circuit with a Q of 2, or a dual tuned circuit with a Q of 3 is adequate. The dual tuned circuit has the advantage that the peak to peak video output is larger than that of the single tuned circuit, but extra components are required. Both circuits have a larger video bandwidth than the required 9MHz. The value of the damping resistor for the required Q is calculated below:

For $Q = 2$

$$\text{Total } R = Q2\pi fL$$
$$= 2 \times 2 \times \pi \times 140 \times 10^6 \times 0.04 \times 10^{-6}$$
$$= 70.3717\Omega$$

allowing for the internal 800Ω resistance between pins 2 and 3 (see Fig.3), the external resistance should be 77.1Ω, choose 82Ω.

For $Q = 3$

Total $R = Q2\pi fL$

$= 3 \times 2 \times \pi \times 140 \times 10^6 \times 0.04 \times 10^{-6}$

$= 105.56\Omega$

allowing for the internal 800Ω resistance, the external resistance should be 121.5Ω, choose 120Ω.

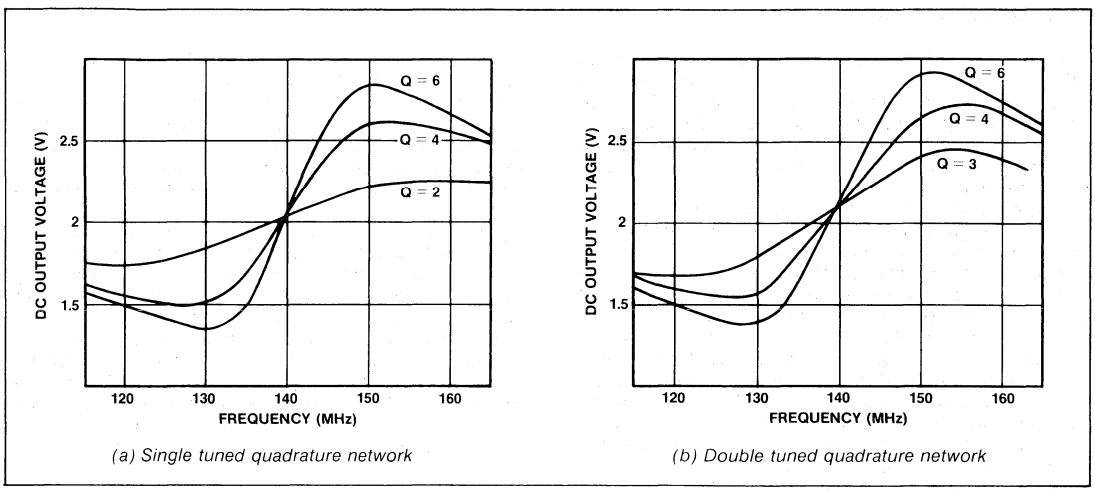
When using a dual tuned circuit the value of coupling capacitor is dependent on the Q factor. Table 2 give a guide to the values needed for best linearity.

Q	BANDWIDTH
6	10MHz
4	11MHz
2	12MHz

Table 1

Q	COUPLING CAPACITOR
6	3.9pF
4	5.6pF
3	10pF

Table 2



(a) Single tuned quadrature network

(b) Double tuned quadrature network

Fig.5 Output voltage v frequency

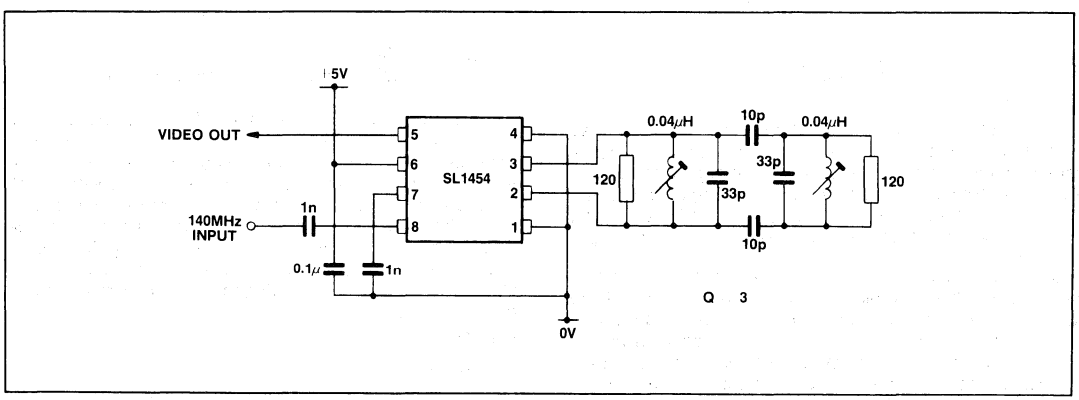


Fig.6 Example of double tuned quadrature circuit

2036-1.0

SL1455

WIDEBAND FM DEMODULATOR WITH THRESHOLD EXTENSION

The SL1455 is a wideband FM demodulator with threshold extension. It is intended for use in satellite receivers with an IF between 300MHz and 700MHz. The device features electrostatic protection on all pins.

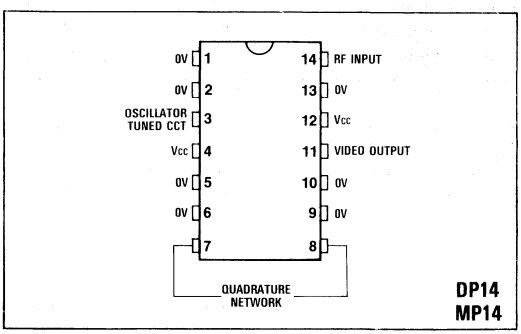


Fig.1 Pin connections (top view)

FEATURES

- 7dB Noise Threshold Obtainable
- Low External Component Count
- Negligible Differential Gain and Phase Error
- Wide Operating Frequency Range 300 to 700MHz
- Demodulates FM Signals with up to 28MHz Pk to Pk Deviation

APPLICATIONS

- DBS Receivers
- Wideband Data Communications Demodulator

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**-10° C to 80° C**
Supply voltage	7V
Storage temperature range	-55° C to 125° C

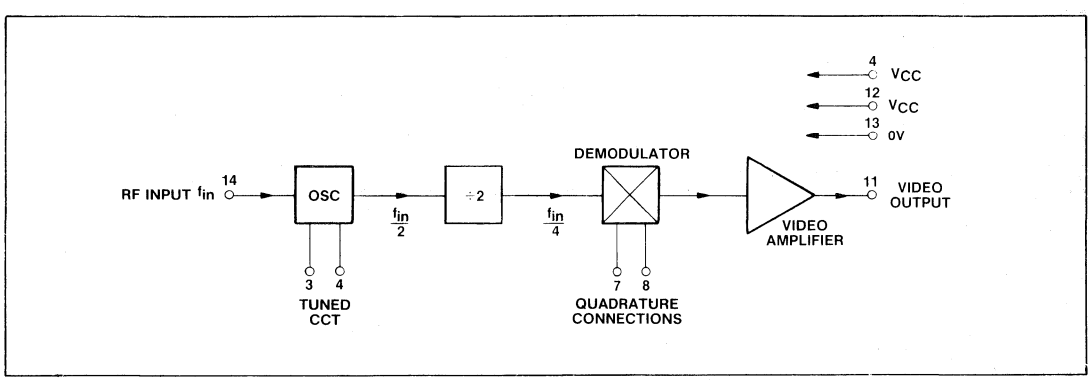


Fig. 2 Block diagram of SL1455

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25° C V_{CC} = 4.5V - 5.5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	12,4	4.5	5	5.5	V	
Supply current	12,4	25	30	35	mA	
Differential gain			<±1		%	Δf = 21.4MHz p-p. Demodulated staircase referred to input staircase before modulation
Differential phase			<±1		Deg	Demodulated colour bar waveform referred to waveform before modulation
IF range		300	610	700	MHz	
Input level	14		22	400	mV rms	
Noise threshold			7		dB	See Note 1
Output level	11		1.3		V pk to pk	21.4MHz pk to pk deviation
Intermodulation products	11		-60		dB	See Note 2
Video bandwidth			10		MHz	

NOTES
1. All parameters from Noise threshold to Video bandwidth are determined by the application circuit. These results were gained with the circuit in Fig.3.
2. Signal 1 4.433MHz : Deviation = 21.4MHz pk-pk
   Signal 2 6MHz : Deviation = 3MHz pk-pk (PAL and Sound Subcarriers)

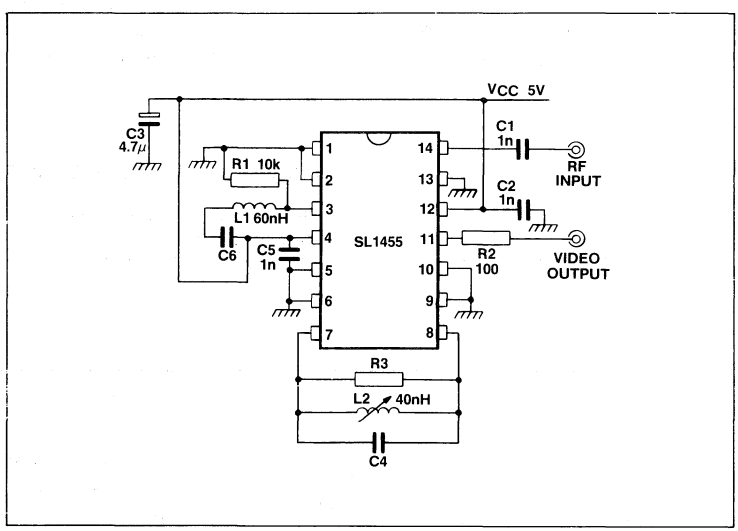


Fig.3 Typical application, 612MHz threshold extended demodulator

Section 3
DBS TV Signal Decoding (MAC)

2211-1.0

MV1710

MAC VIDEO CIRCUIT

The MV1710 is the video circuit for the Nordic VLSI C/D/D2 MAC packet receiver chipset.

The MV1710 video circuit receives the digital MAC vision signal from an 8 bit, 20.25MHz, A/D converter. The vision signal is decompressed and descrambled according to the EBU standard, [ref.1]. Frame and line synchronising signals are received from the MV1720 Control Chip.

The MV1710 is programmable through a configuration chain, which is set up by the microcomputer. The programmable items are scrambling method, descrambling control word, pan constant, output rate, relative output delay and blanking level.

The video output consists of 8 bit digital luminance and UV colour difference signals at frequencies of 13.5MHz and 6.75MHz respectively.

FEATURES

- Double or Single Cut Line Rotation Descrambling
- 4:3 or 16:9 Aspect Ratio
- Separate Sync and Blanking Signals
- Programmable Through the Configuration Chain

ABSOLUTE MAXIMUM RATINGS

(Referenced to V_{SS})

DC Supply voltage V_{DD}	-0.3V to +7V
Input voltage	-0.3V to V_{DD} +0.3V
Storage temperature range	-65°C to +150°C
Ambient operating temperature	0°C to +70°C
Lead temperature	240°C
DC Input Current	±10mA

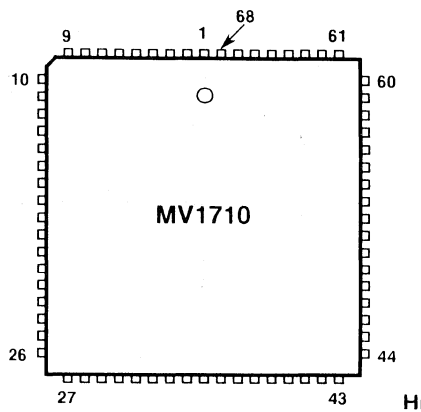
DESCRIPTION OF SIMPLIFIED BLOCK DIAGRAM (FIG.2)

Descrambler

The descrambler controls the video RAM write address calculation. The calculation can be done in three different ways, depending on the content of the VCONF field in the configuration chain. The cases are: no scrambling, double cut scrambling and single cut scrambling. In the scrambling case, the control word is read from the configuration chain register into a PRBS generator and the cut points calculated. Together with a sample counter, this is sufficient to set the RAM write enable for luminance and chrominance at the correct time interval in each line.

Write controller

The write controller administrates which RAM to write to in each line.



Pin	Function	Pin	Function
1	U7	35	VBLANK
2	V_{SS}	36	V_{SS}
3	U3	37	BLACKSTRB
4	U2	38	CDATAIN
5	V_{DD}	39	V_{DD}
6	V0	40	CSTRB
7	V1	41	EFCNT
8	V_{SS}	42	F
9	V4	43	V_{SS}
10	V5	44	L
11	V6	45	FS
12	V7	46	CUTBIT
13	V_{SS}	47	CLK2
14	V3	48	V_{SS}
15	V2	49	CKL13
16	V_{DD}	50	CDATAOUT
17	VIDEO0	51	V_{DD}
18	VIDEO1	52	Y0
19	V_{SS}	53	Y1
20	VIDEO2	54	V_{SS}
21	VIDEO3	55	Y7
22	VIDEO4	56	Y6
23	VIDEO5	57	Y5
24	V_{SS}	58	Y4
25	VIDEO6	59	V_{SS}
26	VIDEO7	60	Y3
27	V_{DD}	61	Y2
28	CLK1	62	V_{DD}
29	V_{SS}	63	U0
30	COMPSYNC	64	U1
31	LUMEN	65	V_{SS}
32	COLEN	66	U4
33	V_{DD}	67	U5
34	HBLANK	68	U6

Fig.1 Pin connections - top view

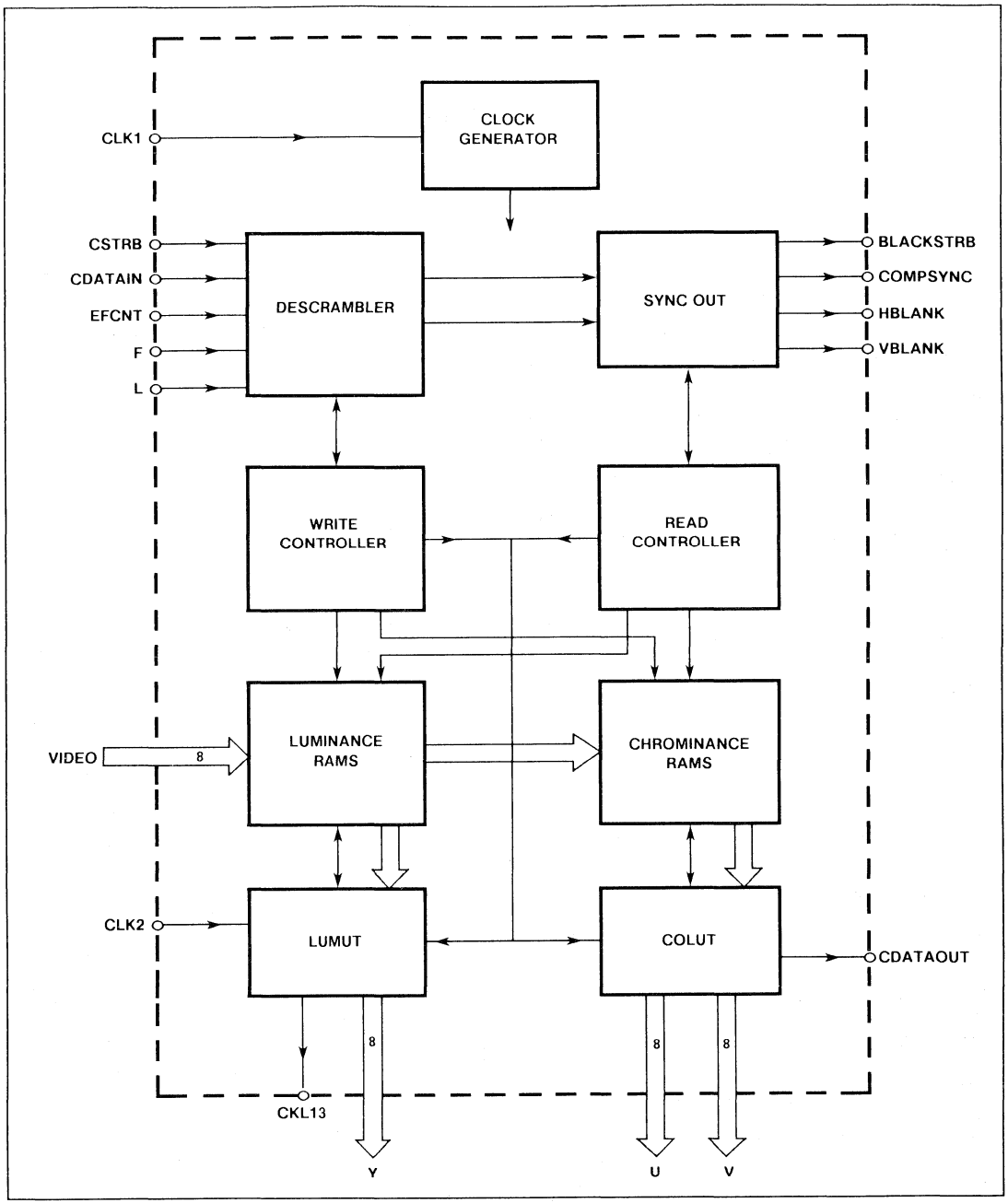


Fig.2 Simplified block diagram for MV1710 MAC video chip

DESCRIPTION (continued)

Read controller

The read controller administrates which RAM to read from in each line. Each RAM is read from address 0 to end within a line period. If the pan option is set, reading is started at a variable address, and only 3/4 of the line is read out.

Luminance RAMS

Two RAMS are included, each capable of storing one line of luminance (697 bytes). During a line, input video is written to one RAM, and output Y is read from the other RAM. In the next line, the first RAM is read and the second RAM is written. This procedure is repeated for each two lines.

Lumut

Lumut controls the Y luminance output. Two options exist:

Y at 13.5MHz, 4:3 aspect ratio picture.
The 13.5MHz may be generated internally or provided by the CLK2 input pin.
Y at 10.125MHz, 16:9 aspect ratio picture.

See Table 2.

Chrominance RAMS

Four chrominance RAMS are included, each capable of storing one line of chrominance (349 bytes). During a line, input video is written to one RAM and output U and V is read from the other three RAMS, one colour component directly, and the other component averaged from the two other RAMS. This procedure is repeated for each four lines.

Colut

Colut controls the U and V colour output. U and V are transmitted on alternate lines, and the missing U or V line is reconstructed by calculating the average between previous and following lines. U is received on odd lines and V on even lines.

The two options are:
U, V at 6.75MHz, 4:3 aspect ratio picture.
U, V at 5.0625MHz, 16:9 aspect ratio picture.

See Table 2.

Sync Out

Sync out generates the following synchronising signals:
BLACKSTRB, a strobe signal for the black level reference.
COMPOSITE SYNC, a negative line pulse for each line, and 5 field pulses and equalising pulses for change of field. See Fig. 3.
H BLANK, horizontal blanking signal.
V BLANK, vertical blanking signal.

REFERENCES

1. MAC packet family specifications EBU No. Tech 3258-E
2. CCIR report 624-2, Characteristics of Television Systems, Geneva 1982

CONFIGURATION CHAIN

Configuration data (CDATA) are shifted into and through the chip when the CSTRB signal is high, and are kept in the chip when CSTRB is low. No shifting is allowed in the first line of each frame. The configuration data are sent (LSB first) by the micro computer via the MV1720. The proper configuration data must be present at the first line of each frame. The configuration may then be changed at each frame. After synchronisation the correct configuration will be set at the first change of frame. In the case of a scrambled picture, the correct frame count must be known for each frame. Normally only the MSB (most significant bit) of the frame count is sent to MV1710. To avoid waiting for EFCNT to change after power up or change of channel, it is possible to put the frame count into the configuration chain register, to be able to start in an arbitrary frame.

The organisation of the configuration bits in the shift register is shown in Table 1. The configuration data are INC, YBLK, OUTC. PAN, LDEL, CDEL, CW, FCNT, TB and VCONF, with a total length of 13 bytes = 104 bits. They are explained as follows.

INC : 2 bits used to signal the use of the CLK2 input pin.
: 00 CLK2 is not used.
: 01 CLK2 is a 13.5MHz one phase clock. In this case, this clock is used instead of the default internal clock to generate the Y output.
: 10 CLK2 is a 40.5MHz One phase clock. This provides a safer way to generate the internal two phase 13.5MHz clock.

YBLK : 8 Bits black level for Y (luminance) in the horizontal blanking interval. YBLK should be set to the black level of the vision ADC.

OUTC : 2 bits to signal the output configuration. Values are :
: 00 Y 13.5MHz (or 10.125MHz in case of ALTERNATIVE ASPECT ratio)
: 01 For Test Purposes only.
: 10 and 11 should not be used
See Table II.

PAN : A 7-bit sample number between 0 and 86 used to indicate the starting sample for a 4:3 window in a 16:9 picture. There are 349 colour samples in a 16:9 picture of which 262 colour samples are required for the 4:3 picture. For a central picture the PAN number should be 43. PAN may be updated every frame. The starting sample for the luminance data is obtained internally by doubling the PAN number.
See Table 2.

LDEL : A programmable start which is applied to the LUMINANCE (Y) signal relative to the COMPSYNC signal output to compensate for any propagation delay of the LUMINANCE filter.

LDEL	Delay (μs)	LDEL	Delay (μs)
0	0.000	8	0.790
1	0.099	9	0.887
2	0.196	10	0.988
3	0.296	11	1.086
4	0.395	12	1.185
5	0.494	13	1.284
6	0.593	14	1.385
7	0.691	15	1.481

CDEL : A programmable start which is applied to the CHROMINANCE signals (U & V) relative to the LUMINANCE (Y) signal to compensate for differences in the propagation delay of these signals

CDEL	Delay (ns)	
0	-98.8	(Y filter delay > U / V filter delay)
1	-49.4	
2	0.0	
3	49.4	(Y filter delay < U / V filter delay)
4	98.8	
5	148.1	
6	197.5	
7	246.9	

EXAMPLE : If the LUMINANCE filter delay is 0.5μs and the CHROMINANCE filter delay is 0.6μs, then LDEL should be set to 5 and CDEL to 4. The effect of this is that Y will be advanced 0.494μs relative to SYNC, and U/V will be advanced 0.0988μs relative Y, so that both Y, U and V will be in phase with the SYNC after the filter. The function of LDEL and CDEL is easily observed on the screen, with increasing value of LDEL the picture is moved to the left, and with increasing value of CDEL, the colours will move to the left relative to a black/white picture.

Byte #	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	YBLK5	YBLK4	YBLK3	YBLK2	YBLK1	YBLK0	INC1	INC0
1	PAN3	PAN2	PAN1	PAN0	OUTC1	OUTC0	YBLK7	YBLK6
2	CDEL0	LDEL3	LDEL2	LDEL1	LDE10	PAN6	PAN5	PAN4
3	CW05	CW04	CW03	CW02	CW01	CW00	CDEL2	CDEL1
4	CW13	CW12	CW11	CW10	CW09	CW08	CW07	CW06
5	CW21	CW20	CW19	CW18	CW17	CW16	CW15	CW14
6	CW29	CW28	CW27	CW26	CW25	CW24	CW23	CW22
7	CW37	CW36	CW35	CW34	CW33	CW32	CW31	CW30
8	CW45	CW44	CW43	CW42	CW41	CW40	CW39	CW38
9	CW53	CW52	CW51	CW50	CW49	CW48	CW47	CW46
10	FCNT1	FCNT0	CW59	CW58	CW57	CW56	CW55	CW54
11	TB1	TB0	NEWFC	FCNT6	FCNT5	FCNT4	FCNT3	FCNT2
12	VCONF7	VCONF6	VCONF5	VCONF4	VCONF3	VCONF2	VCONF1	VCONF0

Table 1 Configuration chain inside MV1710. Note that INC0 is transmitted first, and VCONF7 last.

CW : 60 bit control word for video descrambling. In the case of free access scrambling, (VCONF bit 2 = 0), the correct control word (60 * 1) must be provided by the microcomputer. See Ref 1, page 201.

FCNT : 7 bit frame count
Bit 6-0 : The 7 LSB's of frame count. Valid only if NEWFC = 1. Together with EFCNT, the full frame count can be constructed.

NEWFC : New frame count
1 : Used to preset the frame count to an initial value that will be valid for the next frame. This is recommended after power on or change of channel, to avoid waiting for a descrambled picture. If set, NEWFC will be automatically cleared in the next frame.
0 : Normal operation.

TB : 2 bits for testing purposes, should be set to 00.

VCONF : Video configuration, see Ref 1, page 145.
The 8 bits are interpreted as follows

Bits 1 & 0
00 : Double cut scrambling
10 : Single cut scrambling
01 : No scrambling

Bit 2 0 : Free Access - Control Word must be supplied by the microprocessor.
1 : Controlled Access - Control Word supplied by the Access Control Module.

Bit 4 0 : Luminance Output at 13.5MHz.
1 : Luminance Output at 10.125MHz. This is intended for reception of a 16:9 picture on a 4:3 receiver. The PAN field in the configuration chain sets the start of the 4:3 picture. See Table 2

Bit 3,6,7 = 0. Bit 5 = 1. This corresponds to a normal compression ratio (CY = 3:2, CU = 3:1) and a normal video active line duration.

Note : When a 16.9 picture is being received, the VCONF4 transmitted in the SI packet will be set to 1. If the receiver can display the full 16.9 picture, the microprocessor must reset VCONF4 in the configuration chain to zero.

PIN DESCRIPTIONS

Symbol	Type	Pin	Description
CLK1	Input	28	20.25MHz one phase master clock
Video 0-7	Input	17,18,20,21 22,23,25,26	Digital Video Data 1296 samples per TV line at a clock frequency of 20.25MHz.
Y 0-7	Output	52,53,55,56 57,58,60,61	Digital Luminance Data. See Note 1
U 0-7	Output	63,64,66,67 68,1,3,4	Digital Chrominance Data. See Note 2
V 0-7	Output	6,7,9,10 11,12,14,15	Digital Chrominance Data. See Note 2
CLK2	Input	47	Auxiliary clock, either set to 0, 13.5MHz or 40.5MHz. Must be signalled via configuration chain INC field.
CKL13	Output	49	13.5MHz clock for Y output. Asymmetrical 2 :1 High : Low.
CDATAIN	Input	38	Configuration data Input. CDATA is strobed by CSTRB.
CDATAOUT	Output	50	Output to the configuration chain. CDATA is strobed by CSTRB.
CSTRB	Output	40	Strobe signal. High when CDATA is valid.
F	Input	42	Frame sync. signal. High for odd numbered frames. See Note 3
L	Input	44	Line sync. signal High for odd numbered lines See Note 3
COMPSYNC	Output	30	Composite line and field synchronising signal according to Ref.2. Derived from 20.25MHz CLK1. See Fig 3
H BLANK	Output	34	Horizontal blanking signal. Low in the line blanking interval between samples 1-212 and again between samples 1266-1296. Blanking period = 243 samples = 12μs.
VBLANK	Output	35	Vertical blanking signal. Low in the field blanking interval ie. sample 1237 line 310 to sample 183 line 336, and again between sample 589 line 623 to sample 831 line 23 in the next field. Blanking period = 25 lines + 243 samples = 1612μs.
BLACKSTRB	Output	37	Black level reference strobe in lines 23 and 335. High from samples 591 to 1284 in both lines in the unscrambled case, cut point dependent otherwise.
EFCNT	Output	41	MSB of internal frame count (FCNT). Toggles in bit 3 in line 625 every 128th frame.
FS	Input	45	Function select. Used for test purposes, must be tied to GND for normal use.
CUTBIT		46	Used for test purposes, should be left unconnected.
COLEN		32	Used for test purposes, should be left unconnected.
LUMEN		31	Used for test purposes, should be left unconnected.
V_{DD}		5,16,27,33, 39,51,62	System power +5V power supply. All pins must be connected.
V_{SS}		2,8,13,19, 24,29,36,43, 48,54,59,65	System ground : 0V. All pins must be connected

NOTES
1. For the remainder of the line Y is set to YBLK (from the configuration data). In the unscrambled case with no delay compensation (LDEL = 0), the Video input samples 590-1286 (697 Y samples) will be placed in the interval 10.77-62.4μs
2. For the remainder of the line U and V will output the value 128 only MSB high.
3 For F and L, transition takes place on rising edge of video sample 1, See Fig. 4.

Table	VCON F4	Picture	Window	Samples / Line	Sample frequency MHz
Luminance	0	4:3	4:3	697	13.5
	1	16:9	4:3	523	10.125
	0	16:9	16:9	697	13.5
Chrominance	0	4:3	4:3	349	6.75
	1	16:9	4:3	262	5.0625
	0	16:9	16:9	349	6.75

Table 2. Digital luminance and chrominance format details

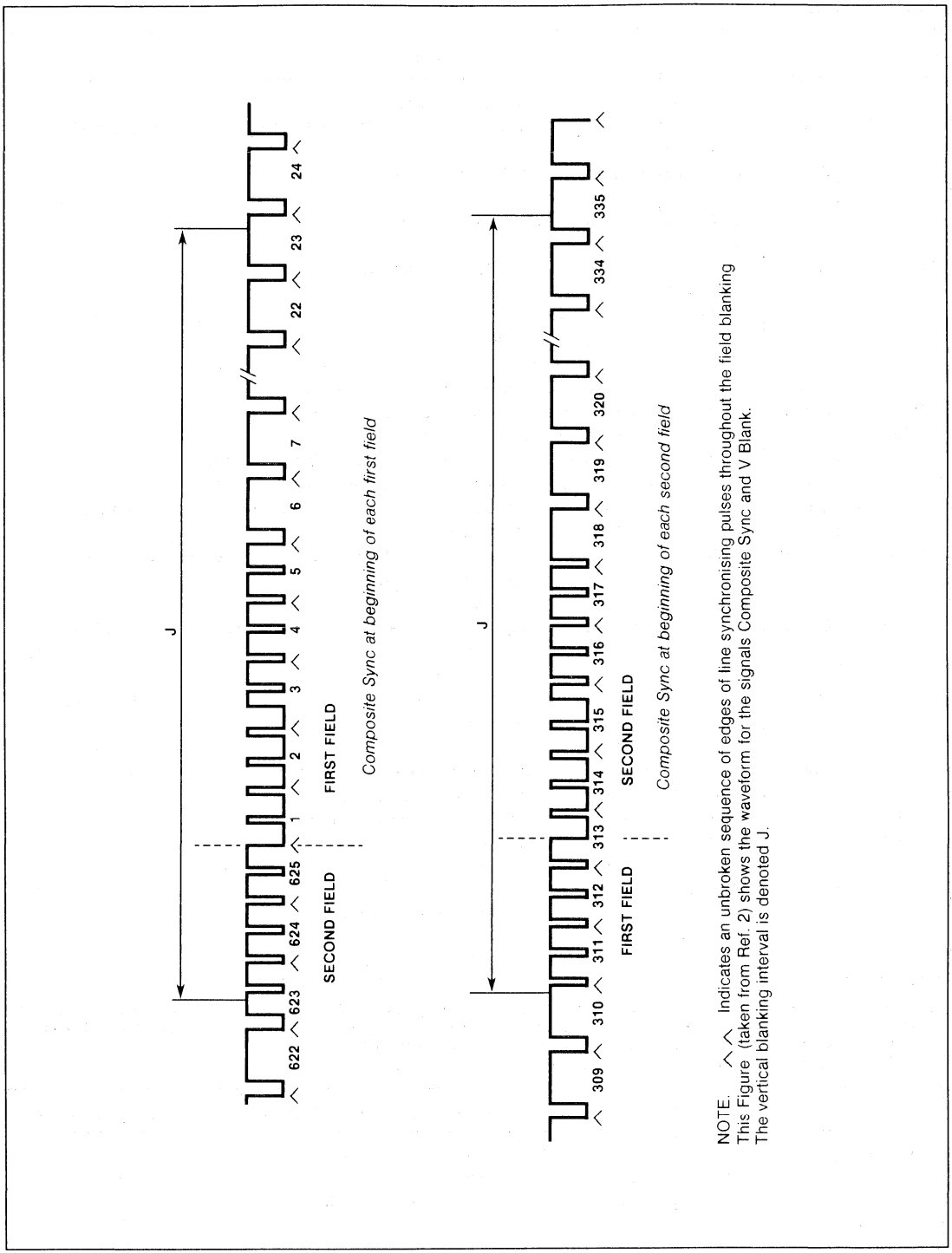


Fig.3 Details of field synchronising waveform

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 0°C +70°C, V_{DD} = +5V ±5%

Characteristic		Value			Units	Conditions
		Min	Typ	Max		
DC Characteristics						
All Inputs	V_{IL}	V_{SS}		1.2	V	
	V_{IH}	3.4		V_{DD}	V	
	I_{IL}			-10	µA	V_{IN} = 0V
	I_{IH}			10	µA	V_{IN} = V_{DD}
All Outputs	V_{OL}			0.4	V	I_{OL} = 4mA
	V_{OH}	V_{DD}-0.4			V	I_{OH} = -2mA
	I_{OS}					V_{DD} = Max. for 1 second max.
		48		192	mA	V_O = V_{DD}
		-24		-96	mA	V_O = 0V
AC Characteristics						
CLK1 frequency		1		21	MHz	
CLK2 frequency				42	MHz	
Setup time (all inputs)		5			ns	See Note 1
VIDEO <7..0> hold time		8.5			ns	See Note 2
CDATAIN hold time		8.0			ns	See Note 2
EFCNT, F, L hold time		8.5			ns	See Note 2
FS hold time		6.5			ns	See Note 2
CSTRB hold time		6.5			ns	See Note 2
CDATAOUT delay				32	ns	See Note 3
Y <7..0> delay				35	ns	See Note 3
Y <7..0> delay				7	ns	See Note 4
U <7..0> delay				31	ns	See Note 3
V <7..0> delay				31	ns	See Note 3
BLACKSTRB delay				30	ns	See Note 3
COMPSYNC delay				32	ns	See Note 3
HBLANK, VBLANK delay				31	ns	See Note 3

NOTES
1. This Figure is valid for all data inputs relative to the positive edge of CLK1. See discussion for specs on the CLK2 input below.
2. All hold times are specified relative to the positive edge of CLK1. See Fig 5.
3. Delays are specified relative to the positive edge of CLK1 at 50pF load. See Fig 5.
4. This delay is specified relative to the positive edge of CKL13. See Fig 6.

AC CHARACTERISTICS OF THE CLK2 INPUT

When CLK2 is at 40.5MHz, the active (negative) edge of CLK2 must avoid a 10ns window that starts at the active (positive) edge of CLK1.
When CLK2 is at 13.5MHz. it must be manually tuned to clock Y at 'safe' samples. This tuning will require that the initial phase of CLK2 is controlled by the LUMEN output, and that CLK2 may be adjusted continously with respect to the CLK1 phase,

AC CHARACTERISTICS OF THE CKL13 INPUT

When CKL13 is generated from CLK1, the edges of CKL13 will alternately be generated from the positive and negative edge of CLK1. The delay from the active CLK1 edge to the corresponding CKL13 edge is maximum 50ns at 50pF load. See Fig 6.
Otherwise CKL13 will have a maximum delay of 28ns from the CLK2 input. When CLK2 is 40.5MHz, CKL13 = CLK2/3. If CLK2 is 13.5MHz, CKL13 = CLK2.

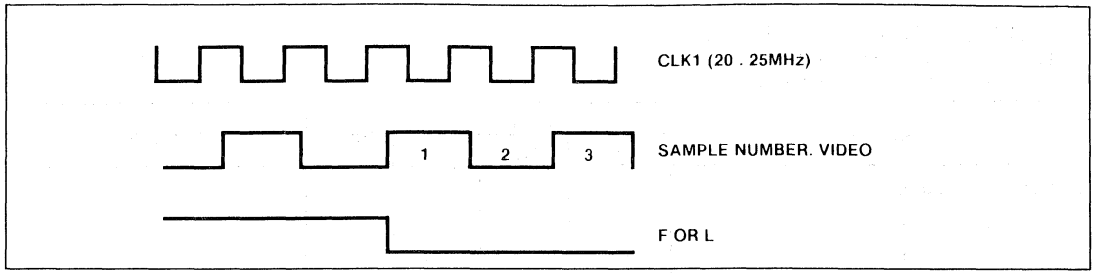
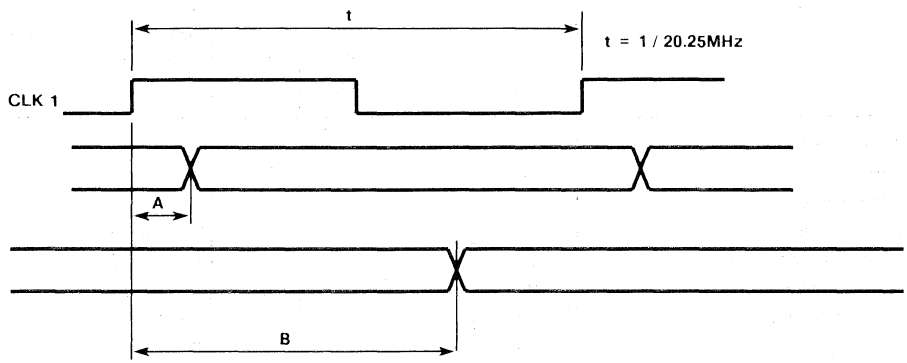
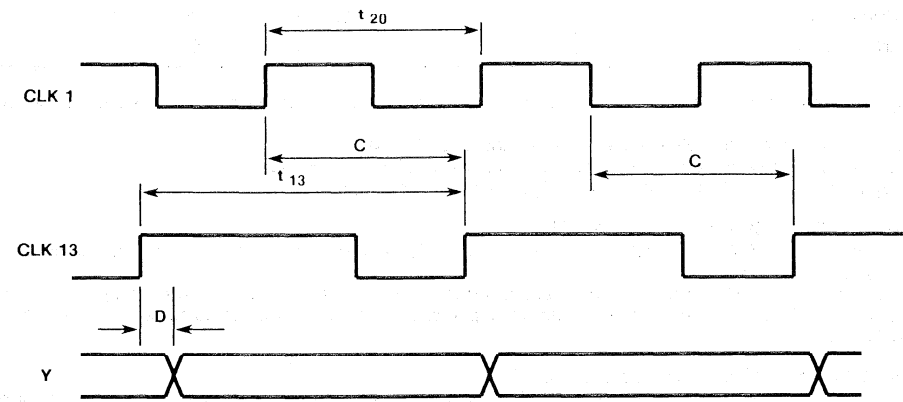


Fig.4 Timing diagram (see AC characteristics for details)



A = Mininum hold time for inputs CSTRB, CDATAIN, EFCNT,F, L, FS, VIDEO <7..0>
B = Maximum output delay for outputs CDATAOUT, BLACKSTRB, COMPSYNC, HBLANK, VBLANK
U <7..0>, V <7..0> AND Y <7..0> AT 20.25MHz OR 10.125MHz (values in AC characteristics table)

Fig.5 Input timing diagram



t_{20} = 1 / 20.25MHz
t_{13} = 1.5 t_{20}
C : OUTPUT DELAY FOR CKL 13
D : OUTPUT DELAY FOR Y AT 13.5MHz
(values in AC characteristics table)

Fig.6 Output timing diagram

2212-1.0

MV1720

MAC CONTROL CIRCUIT

The main functions of the MV1720 for the Nordic VLSI C/D/D2 MAC packet receiver are to decode the bit-stream from the demodulator, and to serve as an interface between the receiver microcomputer and the chip set.

The MV1720 synchronises on the frame structure by recognising line and frame sync, and generates timing signals which control the operation of other modules. Data is spectrum descrambled, and data in the selected bursts is de-interleaved and formed into full packets. Packet headers and optionally the data part are corrected and routed to a common output for sound and data.

SI packets (addr 0), SMM, CMM or AUX packets can also be routed to a separate packet buffer which can be read from the receiver microcomputer. CMM address recognition is supported. Golay encoded packets are decoded, corrected and optionally compressed before they are stored in the packet buffer.

The MV1720 has a general purpose microprocessor interface that is compatible with most microprocessors or microcomputers. The data rate is controlled by the microcomputer and can be up to 2Mbyte/sec.

Line 625 is decoded and majority voted for repeated and static data fields. The resultant data is output as a special 'packet' with separate strobe signals. This packet can also be read via the packet buffer.

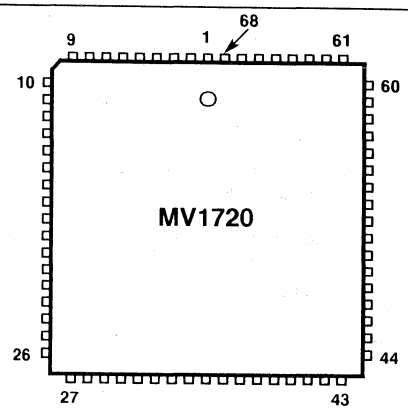
FEATURES

- Programmable Sync Acquisition and Generation
- De-interleaving of Two Independent Subframes
- Hardware Golay Decoding and Correction for CMM, SMM and SI Packets (Programmable)
- Programmable Packet Address Selection
- Programmable SMM Packet Selection
- Programmable CMM Packets Selection with Unique Customer Address and Shared Address (according to the EBU Spec) (Ref.1)
- Programmable CMM Packet Selection with Collective Address and Entire Audience (Proposed EBU Spec Extension) (Ref. 2)
- High-Speed Microprocessor Interface supporting most Microprocessors or Microcomputers

ABSOLUTE MAXIMUM RATINGS

(Referenced to V_{SS})

DC Supply voltage V_{DD}	-0.3V to +7V
Input voltage	-0.3V to V_{DD} +0.3V
Storage temperature range	-65°C to +150°C
Ambient operating temperature	0°C to +70°C
Lead temperature	240°C
DC Input current	±10mA



HP68

Pin	Function	Pin	Function
1	V_{SS}	35	$\overline{CE}$
2	V_{DD}	36	V_{SS}
3	FS2	37	MCD4
4	FS1	38	MCD5
5	RESET	39	V_{DD}
6	DATAIN	40	MCD6
7	CLK1	41	MCD7
8	V_{SS}	42	TEST
9	CDATAOUT	43	TEST
10	TEST	44	TEST
11	TEST	45	TEST
12	CSTRB	46	RS
13	V_{DD}	47	MCLK
14	CLKPLL	48	IRQ
15	CLAMP	49	VAL
16	CDATAIN	50	PDATA
17	L	51	V_{SS}
18	F	52	SPINF
19	TEST	53	SFRO
20	LSYNC	54	V_{DD}
21	V_{SS}	55	PACKST
22	CLKD 2	56	PACKDT
23	$\overline{RD}$	57	V_{SS}
24	$\overline{WR}$	58	SIV
25	TEST	59	TEST
26	TEST	60	TEST
27	TEST	61	TEST
28	TEST	62	SB2
29	V_{SS}	63	SB1
30	MCD0	64	TTV
31	MCD1	65	DISD
32	MCD2	66	DATAOUT
33	V_{DD}	67	ML625
34	MCD3	68	EFCNT

Fig.1 Pin connections - top view

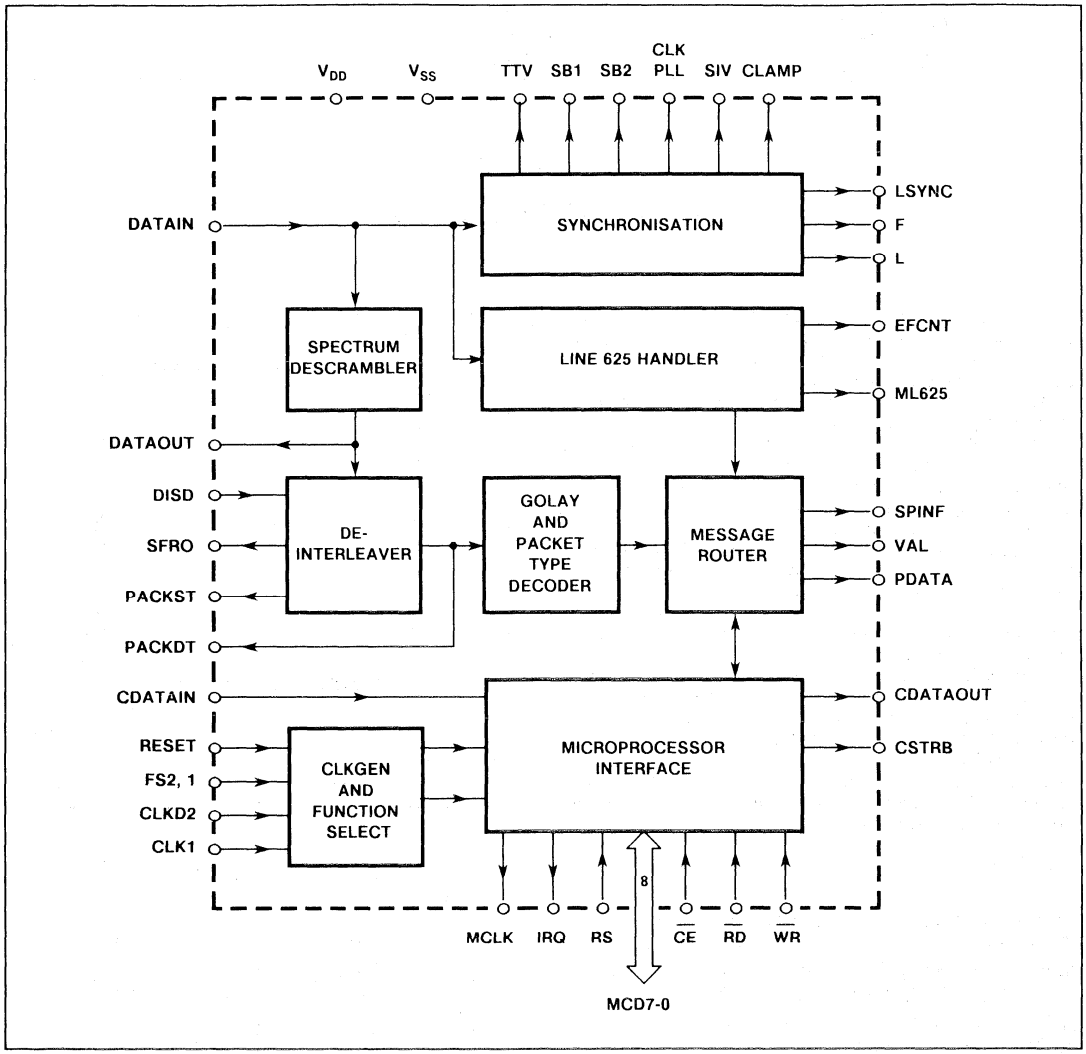


Fig.2 Simplified block diagram for MV1720 MAC packet control chip

PIN DESCRIPTIONS

Symbol	Type	Pin	Description
DATAIN	Input	6	Serial Data from the digital demodulator.
CLK 1	Input	7	20.25MHz one-phase master clock.
CLKD 2	Input	22	10.125MHz one-phase clock signal used for D2 MAC reception.
DATAOUT	Output	66	Spectrum descrambler data.
PACKDT	Output	56	De-interleaved Data. Not Golay decoded. Always 20.25 Mbit/s (even in D2 MAC).
PACKST	Output	55	High when PACKDT contains valid data (751 bits)
SFRO	Output	53	High when PACKDT has data from subframe #2.
CDATAOUT	Output	9	Output to the configutation chain. CDATA is strobed by CSTRB.
V_{DD}		2,13,33 39,54	System Power: +5V power supply. All pins must be connected
V_{SS}		1,8,21,29, 36,51,57	System ground: 0V. All pins must be connected.

PIN DESCRIPTIONS (continued)

Symbol	Type	Pin	Description
CSTRB	Output	12	Strobe signal. High when CDATA is valid. Duration 8 clocks.
CDATAIN	Input	16	Configuration data input. For diagnostic purposes, tie to V_{SS} if not used.
PDATA	Output	50	Packet data (sound/data/line 625 'packet7). 20.25Mbit/s descrambled, de-interleaved and decoded/corrected data.
VAL	Output	49	Indicates every packet header on PDATA. Duration 13 clocks (PA,CI,SFRI).
ML625	Output	67	Indicates line 625 'packet' on PDATA. Duration 741 clocks.
SPINF	Output	52	Special information. Active when SI, CMM, SMM or line 625 'packet' are available on PDATA. Duration 741 clocks.
EFCNT	Output	68	MSB of internal frame count (FCNT). Toggles in bit 3 in line 625 every 128th frame.
RESET	Input	5	Power up reset, used to initialise the MV1720. Sets all internal registers to zero.
F	Output	18	Frame sync. signal. HIGH for odd numbered frames.
L	Output	17	Line sync. signal HIGH for odd numbered lines.
CLKPLL	Output	14	Sample strobe. Active from sample 1 to start of CLAMP. Always active during syncronisation and line 625.
LSYNC	Output	20	Sample strobe. Active for 64 samples after detection of LSW (Line Sync Word).
SB1	Output	63	Sample strobe. Start and stop is programmable. Active only in lines 1-623. Strobes data from subframe #1 into de-interleaver.
SB2	Output	62	Sample strobe. Start and stop is programmable. Active only in lines 1-623. Strobes data from subframe #2 is into de-interleaver.
DISD	Input	65	Disable de-interleaver. Tie to GND for normal operation.
TTV	Output	64	Line strobe. Two intervals are programmable. Only active for sample 230 to 1294. Can be used with teletext in field blanking interval.
SIV	Output	58	Sample strobe. Active when UDT , SDF and RDF fields in line 625 is appearing on DATAIN.
CLAMP	Output	15	Sample strobe. Start and stop is programmable. Active only in lines 1-624. Can be used for clamping.
MCD7-0	I/O	41,30,31 32,34,37 38,40,41	8-bit bidirectional databus controlled with $\overline{CE}$, $\overline{WR}$ and $\overline{RD}$.
$\overline{WR}$	Input	24	Write strobe from microprocessor used to write data into MV1720.
$\overline{RD}$	Input	23	Read strobe from microprocessor used to read data out from MV1720
$\overline{CE}$	Input	35	Chip Enable from microprocessor.
RS	Input	46	Register select from microprocessor 0: Data registers 1: Command or Status
IRQ	Output	48	Interrupt to microprocessor when a selected packet arrives in packet buffer. Polarity programmable active low/high.
MCLK	Output	47	5.0625MHz square wave output signal. Can be used as microprocessor clock.
FS2,FS1	Input	3 , 4	Function select inputs. Used for test purposes must be tied to GND for normal use.
TEST	Output	10,26,27 42,43,44 60,61	No connections must be made to pins marked TEST.

NOTE: All signals are active high except $\overline{CE}$, $\overline{WR}$ and $\overline{RD}$.

DESCRIPTION OF SIMPLIFIED BLOCK DIAGRAM (FIG. 2)

Synchronisation

This module monitors the input data from the receiver, looking for the line sync words (LSW) appearing at the beginning of each line. There are two such alternating words named W1 and W2. The module first looks for 3 consecutive alternating LSWs, and enters 'local sync' when this occurs. Afterwards it expects to find the boundary between an even and odd numbered frame within 1250 lines, i.e. two frame periods.

When searching for the LSW, it will accept 1 bit error before local sync is obtained, after which it switches to accepting 2 bit errors. After entering local sync it may loose 15 consecutive LSWs before sync is assumed to be lost.

When detecting the frame boundary the F and L output signals both change from low to high, and continue to toggle according to the specification. The position where these signals change can be programmed via the microcomputer interface.

This module also generates the signals SB1 and SB2 (flagging two selectable data bursts (subframes) on DATAOUT), SIV (service identification in line 625 on DATAIN), CLAMP (clamp period for video), TTV (lines containing Teletext), and LSYNC (active after each LSW detected).

Spectrum Descrambler

The descrambler contains a 15 bit pseudo-random generator. It starts after LSW is detected in line 1 and runs continuously until line 625 when it is initialised (set to ones).

The DATAIN signal is XOR'd with the output from the generator. This output is available on the DATAOUT pin of the MV1720.

De-Interleaver

This module consists of four 751 bit buffers and a sequencer handling input and output. Each buffer is a 751 x 1 bit RAM. Incoming data arrives in bursts (99 x 2 bits/line for the standard subframes); outgoing data is transmitted as complete packets.

Four buffers enable the MV1720 to de-interleave a continuous stream of data from two independent subframes. It is possible to de-interleave data that only occurs in certain lines, i.e. field blanking by using the DISD input. Output from the de-interleaver is available as PACKDT (packet data), PACKST (packet strobe) and SFRO (subframe origin).

Golay and Packet Type Decoder

This module uses a Meggitt decoder for error correcting the Golay encoded packet header and optionally the data part for selected packets.

To achieve real time operation, a pipelined syndrome register is included. The correctable error patterns are permanently stored in an on chip ROM.

The module removes the 11 bit checksum in the packet header and inserts a bit indicating which of the two selected sub frames is the origin of the packet. The module corrects the Hamming (8,2) PT byte as well.

The resulting error corrected packets are passed on to the Message router.

Messager Router

The Message Router handles all incoming packets, and compares packet addresses and address fields in CMM packets. The microcomputer can select which packets should be transmitted to a buffer in the processor interface.

The selection is done by storing the different addresses in a table in the Message Router and comparing them to appropriate packet fields. This table is updated via the configuration chain. The table contains:

Packet 0 address (permanently stored)		
CMM	packet address	(10 bits)
CMM	packet Unique Customer address	(36 bits)
CMM	packet Shared address	(24 bits)
CMM	packet Collective address	(12 bits)
SMM	packet address	(10 bits)
AUX	packet address	(10 bits)
Line 625	data packet (permanently stored)	

The processor interface can control the priority between the different packets. All packets will be transmitted to the PDATA pin at 20.25Mbit/s. Data in line 625 is converted to a packet with the decimal address 1023 (inserted by the Line 625 Handler).

A strobe signal for the packet headers is provided on a separate pin of the MV1720. This signal (VAL) is high during the first 13 bits (PA, CI, SFRI) of every packet. The format of the data packets on PDATA is shown in Table 2.

The line 625 message is not strobed by the VAL signal. A strobe signal (ML625) is enabled during output of this message. SPINF is enabled during output of packets with packet address 0, CMM, SMM and line 625 "packet"..

Line 625 Handler

This module handles parts of the special data burst in line 625 of each frame; i.e.

UDT - Unified Date Time
SDF - Static Data Frame
RDF - Repeated Data Frame

The first bit of UDT (sequence bit) is checked and any sequence error is flagged in the special line 625 packet. The next four bits of UDT are not processed in any way, just included in the line 625 packet unmodified.

In every fifth line 625 packet, a majority vote of the five last SDFs is included. In the other four packets, the SDF part is not valid. A flag (SDFV) indicates whether SDF is valid or not. The majority voted SDF's are also BCH error checked but not corrected. If the BCH check fails then SDFV is not set.

The five TDMCTLs in line 625 are also majority voted and BCH checked. The result (RDF) is included in the line 625 packet together with an error flag for the BCH check.

The module also contains a flywheel counter for FCNT. This counter is incremented every line 625. The most significant bit of FCNT is available externally as EFCNT. If a valid RDF is received, the received FCNT is loaded into the counter. Loading FCNT will not change EFCNT before next line 625. The format of the line 625 packet is shown in Table 3 and Table 5.

Clock Generator and Function Select

CLK1 is used to generate all internal timing and must always be available. CLKD2 is only for D2 MAC reception.

RESET is used to reset MV1720 to a known state after power up. Sets all internal registers to zero.

FS1 and FS2 are function select inputs used during test and should always be tied to V_{SS}.

Processor Interface

The processor interface is for an external microcomputer. This microcomputer initialises and configures the complete MAC packet chipset, and receives selected information from the packet multiplex together with status information.

This interface is designed to be compatible with a large number of different microprocessors or single chip microcomputers. The interface is shown in Fig. 3.

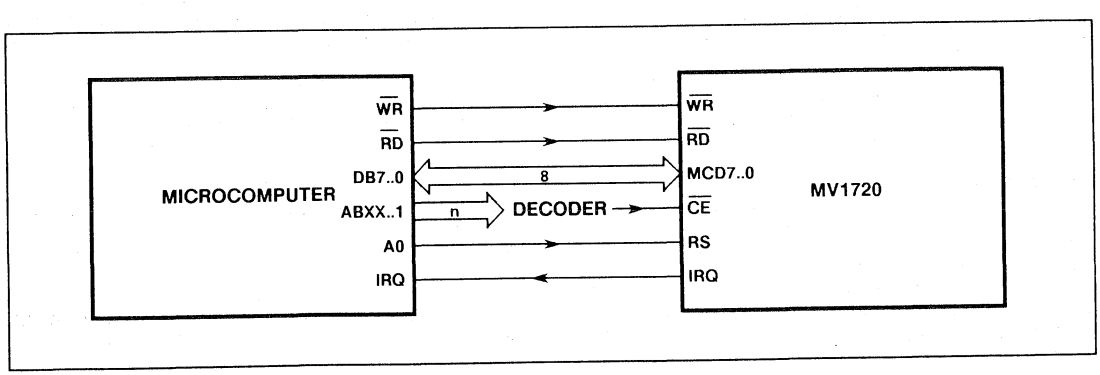


Fig.3 Interface between the MV1720 and a microcomputer

This Interface selects one of four 8 bit registers in the control chip. These are:

- Data input register (read only)
- Data output register (write only)
- Status register (read only)
- Command register (write only)

The control signals $\overline{CE}$ (Chip Enable), RS (Register Select), $\overline{WR}$ and $\overline{RD}$ (WRite and ReaD strobe) select these registers in the following way:

$\overline{CE}$	RS	$\overline{WR}$	$\overline{RD}$	Action
1	X	X	X	No selection
0	X	1	1	No selection
0	X	0	0	Illegal
0	0	0	1	Data Out
0	0	1	0	Data In
0	1	0	1	Command
0	1	1	0	Status

Fig 4 Register selection (X = 0 or 1)

These registers control all interaction between the microcomputer and the MV1720. The complete chip set contains a number of programmable registers, which are addressed indirectly using the four basic registers and the configuration chain.

COMMAND STRUCTURE

The MV1720 supports a set of commands for accessing the various functions. A command consists of a command byte written to the command register followed by zero or more parameters written to the DATA OUT register. The result of the command can be read using the DATA IN register.

The Status register can always be read directly.
The following commands are at present defined.

* Command 00H: Select and read Data packets.
* Command 01H: Configuration chain control.
* Command 10H: MV1720 internal operations.

See Table 9 for a description of the processor interface registers.

Select and Read Data Packets

The processor interface (PIO) can select packets from the PDATA output and store them in a separate buffer. The size of this buffer is 93 bytes (744 bits). The content can then be read by the micro computer via the parallel bus interface.

Packet selection is done by comparing the 10 bit packet address in the packet header simultanously with five 10-bit addresses stored in a table. Three of these values are programmable via the configuration chain, the other two are fixed.

The following packets can be selected:

- CMM packet (programmable address)
- SMM packet (programmable address)
- SI packet (fixed address = 0)
- Aux packet (programmable address)
- Line 625 packet (no address)

When one of the above packets arrives it is routed to the packet buffer and fills it. The buffer is then marked occupied so that a new packet will not overwrite it. The IRQ line is activated to inform the microcomputer.

Golay encoded CMM packets are always corrected. Golay encoded SMM and SI packets and/or Aux packets can individually be corrected by setting two bits in the configuration chain.

The microcomputer reads the status register to examine which packet has arrived. By writing 00H to the Command register the packet buffer is selected and the content of the packet maybe read via the DATA IN register. Each succesive read of the DATA IN register increments a pointer in the packet buffer. After 93 read operations the packet is read. Reading more than 93 bytes yields undefined results.

The buffer is occupied until the micro writes to the DATA OUT register with CLRPTR = 1. This clears the read pointer and signals that the buffer is available for a new packet. It is not neccesary to read the DATA IN register first. This can be used to discard unwanted packets.

Packets may be stopped from entering the buffer by setting some of the mask bits (M625, MAUX, MSMM, MCMM and MPK0) to one.

If the information part (last 90 bytes) of a packet is Golay decoded and corrected, it is possible to remove the 12 check bits for each Golay (23, 12) word after decoding. The information part in the packet buffer is then 45 bytes long, a total of 48 bytes.

This is selected by setting the GOLCOM bit (see internal control). Only packets which are Golay decoded are compressed. The status register indicates the length of the packet (48 or 93 bytes). The PDATA output is not affected by GOLCOM. Tables 6, 7 and 8 show the Golay decoded packet formats.

CMM - Packet Handling

The CMM (Customer Management Message) packets are treated in a special way by the PIO. Normal packets are selected only by the address in the packet header, while the CMM packets use the data area for a sub-address. These subaddresses are stored in a table updated by the configuration chain.

Both the packet address and the subaddress must match before the packet is routed to the packet buffer. There are three different types of subaddresses, each different in length. The selection between these are dependent on the packet type byte at the start of the data area. When decoding the packet type up to two errors are tolerated.

The following cases exist:

Packet Type	Sub Add	Packet Name	
00H	36 - bit	CMM - U	(Unique Customer Address UCA)
F8H	24 - bit	CMM - S	(Shared Customer Address SCA)
C7H	12 - bit	CMM - C	(Collective Customer Add CCA)
3FH	none	CMM - E	(Entire Audience)

Some CMM packets occur very seldom with the correct U, S or C. It is possible to overwrite the packet buffer when a CMM packet arrives.

The EN1 and EN0 bits in the Packet Buffer Control Register selects how overwrite should operate. (see Table 9)

EN1	EN0	Interpretation
0	0	Do not overwrite packet buffer
0	1	Only CMM - U overwrite
1	0	CMM - U or CMM - S overwrite
1	1	CMM - U, CMM - S or CMM - C overwrite

CMM-E can never overwrite the packet buffer. If the buffer is overwritten, it will not be overwritten again. The DATA OUT register with CLRPTR = 1 will release the buffer.

The Status register will indicate that the buffer has been overwritten by setting OVRWRT = 1. PT1 and PT0 then indicate UCA, SCA, CCA or entire audience.

If the microcomputer was reading the packet buffer while the buffer was overwritten by a CMM packet, the reading is inhibited. Reading the DATA IN register does not disturb buffer update in any way. When the update is finished, the IRQ line is activated, and the Status register will indicate buffer overwrite. The **Command Register** must be written with 00H before the CMM packet can be read.

If CMM overwrite is used, the Status register should be read immediately after a packet is read by the micro to determine if the buffer has been overwritten.

CONFIGURATION CHAIN CONTROL

The configuration chain is a long shift register that runs through all of the chips in the MAC packet chip set. This configuration chain must be updated during line 2 to 624; during lines 625 and 1 the information in each chip is stored. The microcomputer has the responsibility that the configuration chain holds relevant data when line 625 arrives.

MV1720 contains two registers that are used to control the configuration chain. These two registers are selected when the **Command Register** is written with 01H.

Configuration Update Register (Data Out)

The configuration chain is updated by simply writing to the configuration chain update register. After the writing is done, 8 bits of configuration data are shifted out. The information is first shifted through the configuration chain inside the MV1720, then through the other chips in the chip set.

The actual length of the configuration chain is dependent on the type and number of chips in the system. The information to the last chip in the system must be written first. The length of the configuration chain inside each chip is always divisible by eight.

Configuration Input Register (Data In)

The output from the last chip in the system can be routed back to the CDATAIN (configuration data input) of the MV1720. This input is internally connected to the configuration input register which can be read with the DATA IN register. The configuration input register is shifted each time the configuration update register is written.

By observing the configuration input register it is possible to monitor both the length and correct operation of the configuration chain.

The use of the configuration input register is optional.

MV1720 INTERNAL OPERATION

When the **Command Register** is written with 02H the DATA OUT and DATA IN register have the following interpretation:

Mode Register (Data Out)

Writing a byte to the DATA OUT register will set certain operational characteristics of the MV1720:

7	6	5	4	3	2	1	0
MBZ	MBZ	FSYNC	GOL COM	MBZ	PKSPC	NIRQ	D2

Bit 7, 6, 3: MBZ - Must be Zero (Reserved)

Bit 5: FSYNC - Force Sync:
0: Automatic line frame sync based on DATATIN
1: Force synchronisation (arbitary)

Bit 4: GOLCOM - Golay Compress
0: Retain check bits after Golay correction
1: Remove check bits in packet buffer

Bit 2: PKSPC - Packet Spacing
0: 14.1 μs minimum packet spacing on PDATA
1: 1.8 μs minimum packet spacing on PDATA

Bit 1: NIRQ - Negate IRQ line
0: IRQ active high
1: IRQ active low

Bit 0: D2 - MAC selection
0: C D MAC (20.25Mbit/s data rate)
1: D2 MAC (10.125Mbit/s data rate)

Bit Error Rate Register (Data In)

The DATA IN register gives the result of the Bit Error Rate counter. This is an 8 bit counter that is incremented each time an error is corrected in the packet header (PH) of each data packet (also dummy packets). The packet header is (23, 12) Golay coded and a maximum of 3 errors can be detected and corrected.

The BER counter is only cleared at power up. The counter wraps around from 0FFH to zero. The microcomputer will have to read the BER counter at regular intervals to calculate the Bit Error Rate. Updating of the BER counter is inhibited while the counter is read.

References:

1. EBU Technical Centre Tech 3258 E. Specification of the System of the MAC packet Family, Oct 1986.
2. Eurocrypt Access Control System for the MAC Packet Family. Proposal for a new part 6 of the EBU specification for the MAC PACKET FAMILY, Oct 1988.

MV1720 Configuration Chain

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	CLMF7	CLMF6	CLMF5	CLMF4	CLMF3	CLMF2	CLMF1	CLMF0
1	CLML4	CLML3	CLML2	CLML1	CLML0	CLMFA	CLMF9	CLMF8
2	SB1F1	SB1F0	CLMLA	CLML9	CLML8	CLML7	CLML6	CLML5
3	SB1F9	SB1F8	SB1F7	SB1F6	SB1F5	SB1F4	SB1F3	SB1F2
4	SB1L6	SB1L5	SB3L4	SB1L3	SB1L2	SB1L1	SB1L0	SB1FA
5	SB2F3	SB2F2	SB2F1	SB2F0	SB1LA	SB1L9	SB1L8	SB1L7
6	SB2L0	SB2FA	SB2F9	SB2F8	SB2F7	SB2F6	SB2F5	SB2F4
7	SB2L8	SB2L7	SB2L6	SB2L5	SB2L4	SB2L3	SB2L2	SB2L1
8	FL4	FL3	FL2	FL1	FL0	TST	SB2LA	SB2L9
9	TTAF7	TTAF6	TTAF5	TTAF4	TTAF3	TTAF2	TTAF1	TTAF0
10	TTAL5	TTAL4	TTAL3	TTAL2	TTAL1	TTAL0	TTAF9	TTAF8
11	TTBF3	TTBF2	TTBF1	TTBF0	TTAL9	TTAL8	TTAL7	TTAL6
12	TTBL1	TTBL0	TTBF9	TTBF8	TTBF7	TTBF6	TTBF5	TTBF4
13	TTBL9	TTBL8	TTBL7	TTBL6	TTBL5	TTBL4	TTBL3	TTBL2
14	AUX7	AUX6	AUX5	AUX4	AUX3	AUX2	AUX1	AUX0
15	SMM5	SMM4	SMM3	SMM2	SMM1	SMM0	AUX9	AUX8
16	CMM3	CMM2	CMM1	CMM0	SMM9	SMM8	SMM7	SMM6
17	SCA1	SCA0	CMM9	CMM8	CMM7	CMM6	CMM5	CMM4
18	SCA9	SCA8	SCA7	SCA6	SCA5	SCA4	SCA3	SCA2
19	SCA17	SCA16	SCA15	SCA14	SCA13	SCA12	SCA11	SCA10
20	UCA1	UCA0	SCA23	SCA22	SCA21	SCA20	SCA19	SCA18
21	UCA9	UCA8	UCA7	UCA6	UCA5	UCA4	UCA3	UCA2
22	UCA17	UCA16	UCA15	UCA14	UCA13	UCA12	UCA11	UCA10
23	UCA25	UCA24	UCA23	UCA22	UCA21	UCA20	UCA19	UCA18
24	UCA33	UCA32	UCA31	UCA30	UCA29	UCA28	UCA27	UCA26
25	CCA5	CCA4	CCA3	CCA2	CCA1	CCA0	UCA35	UCA34
26	SIGOL	AUGOL	CCA11	CCA10	CCA9	CCA8	CCA7	CCA6

Table 1. Content of the configuration chain inside the MV1720. Note that CLMF0 is transmitted first, and SIGOL last

CLMFA. .F0	= First clock period of Clamp	[0-1295]	(11 bits)	
CLMLA. .L0	= Last clock period of Clamp	[0-1295]	(11 bits)	
SB1FA. .1F0	= First clock period of SB1	[0-1295]	(11 bits)	
SB1LA. .1L0	= Last clock period of SB1	[0-1295]	(11 bits)	
SB2FA. .2F0	= First clock period of SB2	[0-1295]	(11 bits)	
SB2LA. .2L0	= Last clock period of SB2	[0-1295]	(11 bits)	
TST	= Factory test mode	[0]	(1 bit)	
FL 4. .0	= Relative position of F and L	[-15, 15]	(5 bits)	(MSB = sign, 4LSBs = amplitude)
TTAF9. .AF0	= First line number with Teletext	[1-625]	(10 bits)	
TTAL9. .AL0	= Last line number with Teletext	[1-625]	(10 bits)	
TTBF9. .BF0	= First line number with Teletext	[1-625]	(10 bits)	
TTBF9. .BL0	= Last line number with Teletext	[1-625]	(10 bits)	
AUX9. .0	= Packet address for AUX message	[0-1023]	(10 bits)	
SMM9. .0	= Packet address for SMM message	[0-1023]	(10 bits)	
CMM9. .0	= Packet address for CMM message	[0-1023]	(10 bits)	
SCA23. .0	= Shared customer address	[0-16M]	(24 bits)	
UCA35. .0	= Unique customer address	[0-64G]	(36 bits)	
CCA11. .0	= Collective customer address	[0-4095]	(12 bits)	
SIGOL	= Golay decode SI and SMM data if SIGOL = 1			
AUGOL	= Golay decode AUX data if AUGOL = 1			

Bit #			
1-10	PA0-PA9	Packet address	(10 bits)
11-12	CI0-CI1	Continuity Index	(2 bits)
13	SFRI	Subframe 1 or 2	(1 bit)
14-21	PT0-PT7	Packet type	(8 bits)
22-741	D000-D719	Data	(720 bits or 90 bytes)

Table 2 Normal packet format on PDATA output

Bit				Bit			
1 - 13	all '1'	PA, SCI and SFRI	(13 bits)	101 - 108	TDC0 - TDC7	TDMCID	(8 bits)
14 - 17	UDT0-UDT3	Unified Date / Time digit	(4 bits)	109 - 118	F10 - F19	FLN1	(10 bits)
18	UDTV	UDT valid	(1 bit)	119 - 128	L10 - L19	LLN1	(10 bits)
19	UUDT	Update UDT	(1 bit)	129 - 138	F20 - F29	FLN2	(10 bits)
20 - 35	CH00 - CH15	CHID	(16 bits)	139 - 148	L20 - L29	LLN2	(10 bits)
36 - 43	SCR0 - SCR7	SDFSCR	(8 bits)	149 - 159	FCP0 - FCP10	FCP	(11bits)
44 - 51	MVS0 - MVS7	MVSCG	(8 bits)	160 - 170	LCP0 - LCP10	LCP	(11 bits)
52 - 71	CF00 - CF19	CAFCNT	(20 bits)	171	LNKS	LINKS	(1 bit)
72 - 76	all '1'	Unassigned	(5 bits)	172 - 185	BR00 - BR13	BCH checksum RDF for	(14 bits)
77 - 90	BS00 - BS13	BCH checksum for SDF	(14 bits)	186	RDFV	RDF valid	(1 bit)
91	SDFV	SDF valid	(1 bit)	187 - 741	all '1'	Unassigned	(555 bits)
92 - 99	FC0 - FC7	FCNT	(8 bits)				
100	UDF	UDF	(1 bit)				

Table 3. Line 625 packet on PDATA

UDTV = 1 : Valid UDT3 - UDT0 data
UDTV = 0 : Chain code error
UUDT = 1 : Last bit in chain code sequence (second marker)
RDFV = 1 : Valid RDF - field (BCH correct after majority voting)
SDFV = 1 : Valid SDF - field (BCH correct after majority voting)
SDFV = 0 : BCH - error or insuffient data for majority voting

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comments
1	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PA : Packet Address
2	'X'	'X'	'X'	SFRI	CI1	CI0	PA9	PA8	CI : Continuity Index
3	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	SFRI : Subframe Index
4	D7	D6	D5	D4	D3	D2	D1	D0	'X' : Random Data
5	D15	D14	D13	D12	D11	D10	D9	D8	PT : Packet Type
	:	:	:	:	:	:	:	:	
	:	:	:	:	:	:	:	:	
93	D719	D718	D717	D716	D715	D714	D713	D712	

Table 4. Format of data packet read via the processor interface

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comments
1	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1' : Logic one
2	'X'	'X'	'X'	'1'	'1'	'1'	'1'	'1'	UDT : Unified Date
3	CH1	CH0	UUDT	UDTV	UDT3	UDT2	UDT1	UDT0	& Time digit
4	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	UDTV : UDT Valid
5	SCR1	SCR0	CH15	CH14	CH13	CH12	CH11	CH10	UUDT : Update UDT
6	MVS1	MVS0	SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	CH : CHID
7	CF1	CF0	MVS7	MVS6	MVS5	MVS4	MVS3	MVS2	SCR : SDFSCR
8	CF9	CF8	CF7	CF6	CF5	CF4	CF3	CF2	MVS : MVSCG
9	CF17	CF16	CF15	CF14	CF13	CF12	CF11	CF10	CF : CAFCNT
10	BS00	'1'	'1'	'1'	'1'	'1'	CF19	CF18	SDFV : Static Data
11	BS08	BS07	BS06	BS05	BS04	BS03	BS02	BS01	Frame Valid
12	FC1	FC0	SDFV	BS13	BS12	BS11	BS10	BS09	FC : FCNT
13	TDC0	UDF	FC7	FC6	FC5	FC4	FC3	FC2	UDF : UDF
14	F10	TDC7	TDC6	TDC5	TDC4	TDC3	TDC2	TDC1	TDC : TDMCID
15	F18	F17	F16	F15	F14	F13	F12	F11	F10-19 : FLN1
16	L16	L15	L14	L13	L12	L11	L10	F19	L10-19 : LLN1
17	F24	F23	F22	F21	F20	L19	L18	L17	F20-29 : FLN2
18	L22	L21	L20	F29	F28	F27	F26	F25	L20-29 : LLN2
19	FC0	L29	L28	L27	L26	L25	L24	L23	FC0-10 : FCP
20	FC8	FC7	FC6	FC5	FC4	FC3	FC2	FC1	LC0-10 : LCP

Table 5 (part). Line 625...

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comments
21	LC5	LC4	LC3	LC2	LC1	LC0	FC10	FC9	LNKS : LINKS
22	BR01	BR00	LNKS	LC10	LC9	LC8	LC7	LC6	RDFV : Repeated Data
23	BR09	BR08	BR07	BR06	BR05	BR04	BR03	BR02	Frame Valid
24	'1'	'1'	'1'	RDFV	BR13	BR12	BR11	BR10	BS : BCH checksum
:	:	:	:	:	:	:	:	:	for SDF
:	:	:	:	:	:	:	:	:	BR : BCH checksum
93	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'	for RDF

Table 5 (continued) Line 625 packet format read via the processor interface. See also Table 3 for descriptions

Bit		
1 - 10	PA0 - PA9	Packet address (10 bits)
11 - 12	CI0 - CI1	Continuity Index (2 bits)
13	SFRI	Subframe 1 or 2 (1 bit)
14 - 21	PT0 - PT7	Corrected packet type (8 bits)
22 - 33	D000 - D011	Corrected data (12 bits)
34 - 44	C000 - C010	Corrected suffix (11 bits)
45	'X'	Not used
46 - 57	D012 - D023	Corrected data (12 bits)
58 - 68	C000 - C010	Corrected suffix (11 bits)
69 - 717	'X'	Not used
:		
:		
718 - 729	D355 - D359	Corrected data (12 bits)
730 - 740	C000 - C010	Corrected suffix (11 bits)
741	'X'	Not used

Table 6 Golay decoded packet on PDATA output pin. The GOLCOM bit does not change the format on PDATA

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comments
1	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PA : Packet Address
2	'X'	'X'	'X'	SFRI	CI1	CI0	PA9	PA8	CI : Continuity Index
3	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	SFRI : Subframe Index
4	D7	D6	D5	D4	D3	D2	D1	D0	'X' : Not used
5	C3	C2	C1	C0	D11	D10	D9	D8	PT : Packet type
6	'X'	C10	C9	C8	C7	C6	C5	C4	D : Corrected data
7	D19	D18	D17	D16	D15	D14	D13	D12	C : Corrected suffix
8	C3	C2	C1	C0	D23	D22	D21	D20	
9	'X'	C10	C9	C8	C7	C6	C5	C4	
:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	
91	D355	D354	D353	D352	D351	D350	D349	D348	
92	C3	C2	C1	C0	D359	D358	D357	D356	
93	'X'	C10	C9	C8	C7	C6	C5	C4	

Table 7 Golay decoded packet read via the processor interface when the GOLCOM bit is not set

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Comments
1	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PA : Packet Address
2	'X'	'X'	'X'	SFRI	CI1	CI0	PA9	PA8	CI : Continuity Index
3	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	SFRI : Subframe Index
4	D7	D6	D5	D4	D3	D2	D1	D0	'X' : Not used
5	D15	D14	D13	D12	D11	D10	D9	D8	PT : Packet type
:	:	:	:	:	:	:	:	:	D : Data
:	:	:	:	:	:	:	:	:	
47		D359	D358	D357	D356	D355	D354	D353	D352

Table 8 Golay decoded packet read via the processor interface when the GOLCOM bit is set. Note different length

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
$T_{amb} = 0°C$ to $70°C$, $V_{DD} = 5V \pm 5\%$

Characteristic		Pin	Value			Units	Conditions
			Min	Typ	Max		
DC CHARACTERISTICS							
All Inputs	V_{IL}		V_{SS}		1.2	V	
	V_{IH}		3.4		V_{DD}	V	
	I_{IL}				-10	µA	V_{IN} = 0V
	I_{IH}				10	µA	V_{IN} = V_{DD}
All Outputs	V_{OL}				0.4	V	I_{OL} = 1 mA
	V_{OH}		V_{DD}- 0.4			V	I_{OH} = -2 mA
	I_{OS}						V_{DD} = Max. 1 sec Max.
			24		96	mA	V_O = V_{DD}
			-72		48	mA	V_O = 0V
AC CHARACTERISTICS							
CLK1 frequency			1		21	MHz	
Setup time (all inputs)			5			ns	See note 1
RD width			150			ns	
WR width			100			ns	
WR cycle time			400			ns	
Hold time CDATAIN, CSTRB			8.5			ns	See note 2
CDATAOUT					32	ns	See note 3
RESET width			25			µs	See note 4

NOTES
1 This figure is valid for all Data inputs relative to the positive edge of CLK1.
2 All hold times are specified relative to the positive edge of CLK1.
3 Delays are specified relative to the positive edge of CLK1 at 50pF load.
4 Delay is specified after V_{DD} and CLK1 are stable. CLK1 must be running at 20.25MHz.

COMMAND REGISTER

7	6	5	4	3	2	1	0
MBZ	MBZ	MBZ	MBZ	MBZ	MBZ	CMD1	CMD0

MBZ MUST BE ZERO (RESERVED)

00 - COMMAND 00_H
01 - COMMAND 01_H
10 - COMMAND 02_H
11 - RESERVED

STATUS REGISTER

7	6	5	4	3	2	1	0
INT	PKT COM	OVR-WRT	PT1	PT0	PK2	PK1	PK0

0 - IRQ PASSIVE
1 - IRQ ACTIVE

0 - DATA PART NOT GOLAY DECODED
1 - GOLAY DECODED DATA PART
PACKET BUFFER IS 48 BYTES IF GOLCOM = 1
IN MODE REGISTER

00 - PT = 00_H
01 - PT = $F8_H$
10 - PT = $C7_H$
11 - PT = $3F_H$

000 - RESERVED
001 - RESERVED
010 - AUX PACKET
011 - PACKET 0
100 - SMM PACKET
101 - CMM PACKET
110 - RESERVED
111 - LINE 625 PACKET

0 - BUFFER NOT OVERWRITTEN
1 - BUFFER OVERWRITTEN BY CMM MESSAGE

DATA IN REGISTER

PACKET BUFFER REGISTER

COMMAND 00_H

7	6	5	4	3	2	1	0
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

BYTE ADDRESS IS AUTOMATICALLY INCREMENTED

DATA OUT REGISTER

PACKET BUFFER CONTROL REGISTER

COMMAND 00_H

7	6	5	4	3	2	1	0
CLR PTR	EN1	EN0	M625	MAUX	MSMM	MCMM	MPK0

0 - NORMAL
1 - CLEAR READ - PTR
IN PACKET BUFFER
(RELEASE BUFFER)

0 - ENABLE PACKET
1 - MASK (DISABLE) PACKET
FOR ENTERING PACKET BUFFER

00 - DONT OVERWRITE BUFFER
WITH CMM - PACKETS
01 - ONLY CMM - U OVERWRITE
10 - CMM - U-S OVERWRITE
11 - CMM - U-S - C OVERWRITE

-U = UNIQUE CUSTOMER ADDRESS
-S = SHARED ADDRESS
-C = COLLECTIVE ADDRESS

Table 10 Processor interface registers (part1)

DATA IN REGISTER
CONFIGURATION INPUT REGISTER

COMMAND 01_H	7	6	5	4	3	2	1	0
	CNI7	CNI6	CNI5	CNI4	CNI3	CNI2	CNI1	CNI0

DATA OUT REGISTER
CONFIGURATION UPDATE REGISTER

COMMAND 01_H	7	6	5	4	3	2	1	0
	CNO7	CNO6	CNO5	CNO4	CNO3	CNO2	CNO1	CNO0

DATA IN REGISTER
BIT ERROR REGISTER

COMMAND 02_H	7	6	5	4	3	2	1	0
	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

COUNTER IS INCREMENTED BY BIT ERRORS
DETECTED DURING PACKET HEADER

DATA OUT REGISTER
MODE REGISTER

COMMAND 02_H	7	6	5	4	3	2	1	0
	MBZ	MBZ	F SYNC	GOL COM	MBZ	PK SPC	NIRQ	D2

0 : AUTOMATIC SYNC FROM DATAIN
1 : FORCE SYNC

0 - NORMAL OPERATION
1 - COMPRESS GOLAY CODED PACKETS IN PACKET BUFFER

0 - 14.1 µs MIN PCKT SPACING
1 - 1.8 µs PCKT SPACING

MBZ - MUST BE ZERO (RESERVED)

0 - IRQ ACTIVE HIGH
1 - IRQ ACTIVE LOW

0 - C/D MAC
1 - D2 MAC

Table 10 Processor interface registers (part2)

MV1732

MAC SOUND CIRCUIT

The MV1732 is the sound circuit for the Nordic VLSI C/D/D2 MAC Packet receiver chipset.

The MV1732 receives packets of data from the MV1720 control chip. Packets for the desired sound service and Interpretation Block (BI) packets are recognised and processed. The configuration of the sound is automatically controlled by information in the BI packet. Descrambling of sound and scale factor extraction is done before the packet is stored in an external DRAM. The RAM is a buffer which helps to adjust the varying packet arrivals to a regular output sample frequency. The samples are read from the RAM into the MV1732 for further processing. Errors are detected and corrected before they are forwarded to external chips for error concealment, digital filtering and D/A conversion. A microcomputer supplies the MV1732 with the control word for descrambling, packet address etc. via the MV1720 and configuration chain.

FEATURES

- Simultaneous Processing of Two Independent Sound Services
- Digital Mixing of Main Sound and Commentary
- Digital Attenuation, Muting of each Sound Service
- Linear and Companded Sound Decoding
- First or Second Level Error Correction
- Stereo, Mono, High Quality and Medium Quality Sound
- BI Packets Processed in Hardware on Chip
- Indicates News Flash to Controlling Microprocessor
- Conditional or Free Access Sound
- Several MV1732s (and MV1733s) can be used in Parallel
- Hardware and Software Compatible with SAA1732
- Can use either DRAM or SRAM for External Packet Buffer
- I²S Sound Bus Output

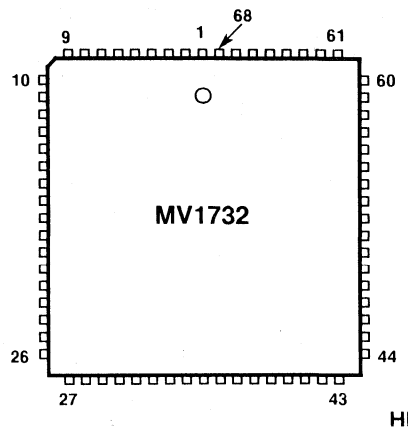
ASSOCIATED DEVICES

SL1700, MV1710, MV1720, MV1733, MV1745

DESCRIPTION OF SIMPLIFIED BLOCK DIAGRAM

Packet Control

The packet control module, provides for packet reception at 20.25Mbit/s and timing for further packet processing. Each incoming packet has a header with a 10 bit address, one bit indicating in which subframe it is located, and two bits used as a continuity index. The packet header of each packet is compared with the contents of the configuration chain, and packets which match address and subframe are extracted. The continuity index is checked and packet loss is flagged.



Pin	Function	Pin	Function
1	CLAB2	35	ADDR9
2	WSAB2	36	OE
3	4OCLK1	37	V_{DD}
4	EFAB1	38	ADDR8
5	V_{DD}	39	ADDR7
6	DAAB1	40	ADDR6
7	CLAB1	41	V_{SS}
8	WSAB1	42	ADDR5
9	PURST	43	ADDR4
10	EFCNT	44	ADDR3
11	V_{DD}	45	ADDR2
12	CLK1	46	V_{SS}
13	VSS	47	ADDR1
14	CDATAIN	48	ADDR0
15	CSTRB	49	IRQ
16	DATA7	50	WE
17	SIV	51	V_{DD}
18	SIC	52	MIXI
19	DATA6	53	CDATAOUT
20	D / S	54	V_{SS}
21	DATA5	55	RESIRQ
22	V_{DD}	56	NFI
23	DATA4	57	COMEN
24	DATA3	58	XC2
25	VAL	59	X22
26	PDATA	60	X12
27	DATA2	61	V_{DD}
28	DATA1	62	XC1
29	V_{SS}	63	X21
30	DATA0	64	X11
31	RAS/ADDR12	65	4OCLK2
32	W/ADDR11	66	V_{SS}
33	V_{SS}	67	EFAB2
34	CAS/ADDR10	68	DAAB2

Fig.1 Pin connections - top view

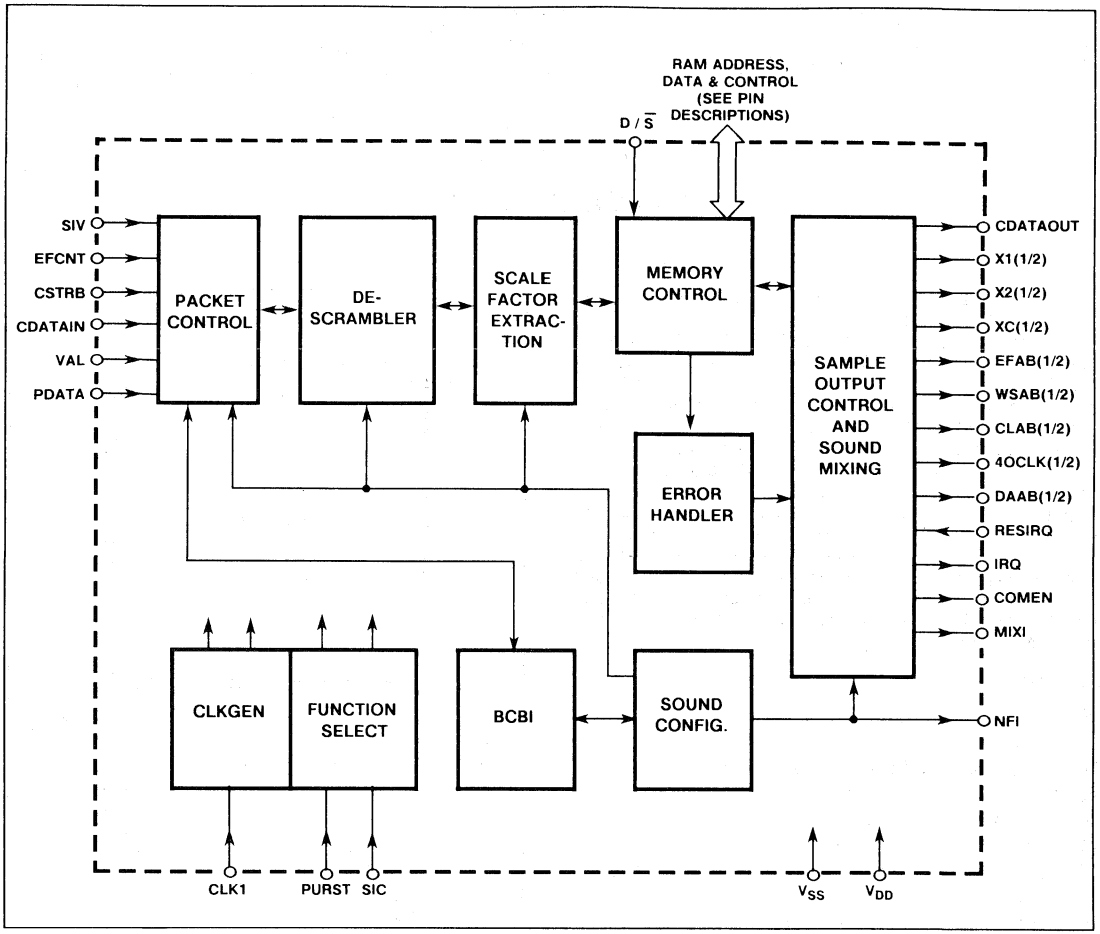


Fig.2 Simplified Block diagram for MV1732 MAC sound chip

PIN DESCRIPTIONS

Symbol	Type	Pin	Description
V_{DD}	Supply	5,11,22,37, 51,61	Power Supply +5V. All pins must be connected.
V_{SS}	Supply	13,29,33,41, 46,54,66	Power Supply 0V. All pins must be connected.
CLAB (1/2)	Output	7,1	Output clock 2.048MHz. Sound service 1 and 2.
WSAB (1/2)	Output	8,2	Word select. 0 = left sample, 1 = right sample. Sound service 1 and 2
40CLK (1/2)	Output	3,65	Output clock 8.192MHz. Sound service 1 and 2.
EFAB (1/2)	Output	4,67	Error Flags. Active high indicates bit errors in the sample. Sound service 1 and 2.
DAAB (1/2)	Output	6,68	Sound samples. 16-bit serial sound data where the two LSBs are always Zero. Sound service 1 and 2.
PURST	Input	9	Power Up & Reset. Sets all internal registers to Zero.
EFCNT	Input	10	MSB of internal 8-Bit frame count (FCNT). Toggles in bit 3 in line 625 every 128th frame. Generated by MV1720.
CLK1	Input	12	20.25MHz single-phase master clock.

PIN DESCRIPTIONS (continued)

Symbol	Type	Pin	Description
CDATAIN	Input	14	Configuration chain Input.
CSTRB	Input	15	Strobe signal; when high the configuration data are shifted into the configuration chain.
DATA0-DATA7	I/O	30,28,27, 24,23,21,19,16	Input/Output of sound data to/from buffer RAM. In DRAM mode only D0 to D3 are used.
SIV	Input	17	Sample strobe. Active for UDT, SDF and RDF fields in line 625. Generated by MV1720.
SIC	Input	18	For test purposes only. MUST be connected to PURST.
D / $\overline{S}$	Input	20	Controls whether the MV1732 uses external DRAM or SRAM, (1 = Dram, 0 = SRAM). This pin on the SAA1732 is a V_{SS} supply pin, so plugging the MV1732 into an SAA1732 application automatically configures the MV1732 to correctly use SRAM.
VAL	Input	25	Indicates every packet header on PDATA. Duration 13 clocks. Generated by MV1720.
PDATA	Input	26	Packet data (sound/data/line 625 'packet') 20.25 Mbits/s spectrum descrambled, de-interleaved and decoded corrected data.
$\overline{RAS}$	Output	31	Row address strobe. Latches the row address on the falling edge. Used in DRAM mode only, in SRAM mode this pin is ADDR 12.
$\overline{W}$	Output	32	Write enable pin. Selects read or write modes ($\overline{W}$ = 0 is write mode). Used in DRAM mode only, in SRAM mode this pin is ADDR11.
$\overline{CAS}$	Output	34	Column Address strobe. Latches the column address on the falling edge. Used in DRAM mode only; in SRAM mode this pin is ADDR 10.
ADDR0-ADDR12	Output	48,47,45, 44,43,42, 40,39,38 35,34,32,31	Address pins for external RAM In DRAM mode only ADDR 0 to ADDR 7 are used.
$\overline{OE}$	Output	37	Output enable signal for static RAM.
IRQ	Output	49	Sound chip mix interrupt request.
$\overline{WE}$	Output	50	Write Enable signal for static RAM.
MIXI	Output	52	Mixing intended. Bit 4 byte 2 in BI block in sound service 2.
CDATAOUT	Output	53	Configuration chain output.
RESIRQ	Input	55	External reset for the IRQ signal.
NFI	Output	56	News flash indication, logical OR for sound services (bit 3, byte 1 BI block).
COMEN	Output	57	Indicates Channel 2 fade in if the signal is high.
XC (1/2)	Output	62,58	Oscillator frequency control. sound service 1 & 2.
X1 (1/2)	Input	64,60	Inputs crystal oscillator, sound service 1 & 2.
X2 (1/2)	Output	63,59	Outputs crystal oscillator, sound service 1 & 2.

BCBI

The BCBI module processes the packet type byte (PT), and determines whether it is a BI, Sound Coding Block (BC1 or BC2) packet. This module also stores changes from BC1 to BC2 and vice versa, and indicates new sound configuration when three packets are received after the change has occurred. The two sound services are handled independently.

Sound Configuration

The sound configuration block handles BI packets. The structuring bytes are error checked (Hamming protection), and if correct, the Bytes 1 and 2 are majority voted over the 5 repetitions. The current sound configuration is updated each time a BI packet is accepted. A new sound configuration is updated when three BC packets are received after a change BC1 to BC2, or BC2 to BC1.

Descrambler

The descrambler handles the two different sound services independently, and synchronisation can be achieved at the start of new frames.

It supports the three different levels of access control described in the MAC standard. (ref .1)

Free access, unscrambled:
The sound data is unchanged.

Free access, scrambled:
The sound data is descrambled with a local control word stored in the receiver.

Conditional access, scrambled:
The sound data is descrambled with a control word from the conditional access system.

The signal EFCNT is the MSB in a frame counter, and it is used to re-synchronise the descrambler. The other bits may be supplied by the configuration chain, to assure fast recovery after change of channel or power up.

The signal SIV starts an update of the descrambling system for each frame.

The control word for descrambling is provided by the configuration chain.

Scale Factor Extraction

The scale factor is extracted by majority decision logic. Nine samples are evaluated for each bit in the scale factor as described in the EBU specification (ref. 1). The control information intended for high speed switching is also extracted.

Memory Block

The external memory can either be DRAM or SRAM controlled by D / $\overline{S}$ (pin 20).

In DRAM mode the MV1732 can interface to either a 4x16K DRAM or a 4x64K DRAM. The MV1732 generates the address, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ signals. Writing is done in page mode. There are a minimum of 256 refresh cycles per 4ms.

In SRAM mode the MV1732 interfaces to an 8x8K SRAM generating $\overline{OE}$ and $\overline{WE}$ signals.

The number of packets in the RAM varies the sample output frequency slightly to maintain the buffer between 14 and 20 packets. A maximum of 32 packets can be stored per sound service.

Errors such as packet loss, full buffer and empty buffer are handled to minimise sound distortion. The parity bit is restored according to the scale factor and Control Information Bits (CIB) before the sound samples are sent to the error handler.

Error Handler

The Error Handler receives data from Memory Control and checks for errors. Four types of checks are done according to the data format:

Range checking (and if possible correction) according to scale factor and coding method (linear/companded).

Parity check (first level protection) for linear and companded data.

Hamming code check with single bit error correction for linear and companded data (second level protection).

Final range checking according to scale factor and coding method.

If non-correctable errors are detected, the sample is flagged for concealment.

In addition the Error Handler does Range Limiting (for linear coding) and Range Expansion (for companded coding) before data is presented to the Sample Output Control Module.

Sample Output Control

The block contains an oscillator and output buffer for each of the two sound services, and a sound mixing unit. The sound mixing unit makes it possible to mix main sound in channel 1 and commentary sound in channel 2. The resulting sound is output on sound service 1 pins.

When the FMIX bit is turned off, the control information for the sound mixing received in the BI packets is used. If a change in the sound mixing conditions occur an interrupt request (IRQ) is generated.

The polarity and reset of the IRQ is controlled by the configuration chain. IRQ can be reset by the bit IRE in the configuration chain, or by the external signal RESIRQ.

The direction flag COMEN indicates the fade up/down direction. COMEN = 1 is fade up commentary sound.

The channel 1 attenuation is controlled by the configuration chain bits X (9..0). The channel 2 attenuation by bits Y (9..0).

The pin MIXI is controlled by the Commentary channel BI packet and indicates when mixing is intended.

The bit MIX in the configuration chain selects if mixing is required or not.

If the bit FMIX in the configuration chain is turned on, the samples from both services are scaled and mixed independent of the BI packet information and the MIX bit.

The frequency of the oscillator controls the sample output rate. In order to maintain the sample storage in the RAM between 14 and 20 packets, the oscillator frequency is shifted slightly (± 150ppm).

A frequency determining network, consisting of an 8.192MHz crystal and three capacitors connected to X1, X2 and XC, See Fig 3. Frequency control is exercised by pulsing XC.

The output pins DAAB, EFAB, CLAB, and WSAB are designed to match the Philips SAA7220 chip. This chip performs error concealment and filtering.

The error flag indicates unreliable sample data.

Each sample is expanded from 14 to 16 bits by inserting zeros in the two LSB's. The sample output frequency is always 32kHz.

When the B1 packet defines medium quality sound with 16kHz sample frequency, every second sample is supplied from a digital oversampling filter in Sound Channel 2 and output on Sound Service 2 pins. If only one SAA7220 is used Channel 2 Sound can be output on Sound Service 1 pins by enabling the FMIX bit in the configuration chain.

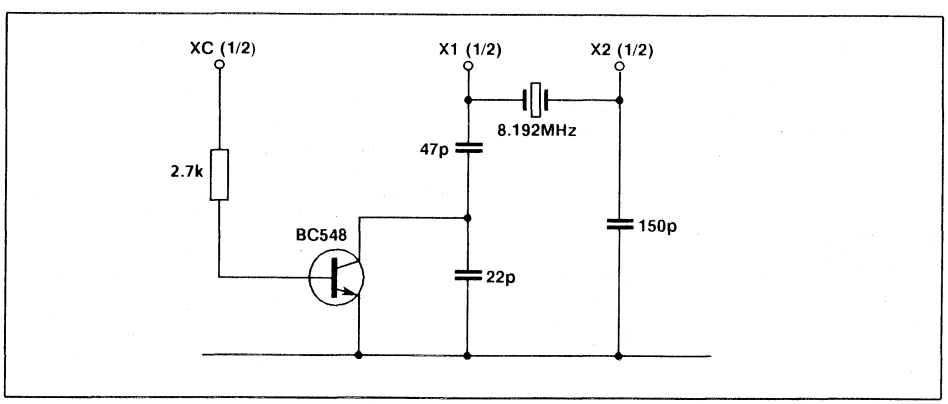


Fig.3 Crystal oscillator circuit.

THE CONFIGURATION CHAIN

The configuration chain is effectively a long shift register running through all circuits which are to be configured from the microcomputer.

Several function blocks of the MV1732 are controlled by the configuration chain. The packet control block needs the packet addresses and indication of which subframe (or both) to select packets from. In addition one bit per sound service is used for muting until a stable state is reached after change of sound service, or after power up.

The configuration chain also provides control words for descrambling. The two services can be descrambled independently.

In addition, the seven least significant bits of the frame count (FCNT), and one bit (NEWFC) indicating update of the frame count after a change of service or power up, are placed in the configuration chain.

The sound mixing can be turned on and off, and the mixing levels for both sound services are controlled independently.

The configuration chain may be updated from the microprocessor at any time except in line 625 and line 1.

The configuration data is clocked into the chain when CSTRB is high, otherwise the contents of each register stage is stored.

Configuration Chain Update

After power up or change of service the corresponding control word, CW, for descrambling should be transmitted to the configuration chain as soon as a valid control word is available, together with the 7 LSBs of the frame count FCNT (the MSB is provided by EFCNT). If the control bit NEWFC = 1, the descrambling control word will be updated in the first line 625 (SIV = 1). If NEWFC = 0, the descrambling control word will be updated when EFCNT changes from '1' to '0' in the next line 625. Thus, in a stable state it is not necessary to provide the CW every frame.

After power up or change of sevice, new address and subframe indication should be provided at the same time as the new CW and FCNT. Packets will be stopped until the new sound configuration is stable. A new address is indicated in the configuration chain by setting NAD low for one or more frames, and then high again indicating a stable address. After acceptance of a BI packet with the new address, the new BI configuration is applied. After the initialization is completed the sound packets are enabled for further processing. When NAD is low the sound is muted.

The contents of the configuration chain for the sound chip is shown in Table 1. Bytes 0 to 2 cover the sound mix. Bytes 3 to 13 cover sound service 2, while bytes 14 to 24 cover sound service 1.

Sound mix :

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Y3	Y2	Y1	Y0	MIX	IRE	IP0	FMIX ← LSB Sent First
1	X1	X0	Y9	Y8	Y7	Y6	Y5	Y4
2	X9	X8	X7	X6	X5	X4	X3	X2

Sound service 2:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	NEWFC	F6	F5	F4	F3	F2	F1	F0
4	CW7	CW6	CW5	CW4	CW3	CW2	CW1	CW0
5	CW15	CW14	CW13	CW12	CW11	CW10	CW9	CW8
6	CW23	CW22	CW21	CW20	CW19	CW18	CW17	CW16
7	CW31	CW30	CW29	CW28	CW27	CW26	CW25	CW24
8	CW39	CW38	CW37	CW36	CW35	CW34	CW33	CW32
9	CW47	CW46	CW45	CW44	CW43	CW42	CW41	CW40
10	CW55	CW54	CW53	CW52	CW51	CW50	CW49	CW48
11	X	X	X	X	CW59	CW58	CW57	CW56
12	PA6	PA5	PA4	PA3	PA2	PA1	PA0	NAD
13	X	X	X	L12	L11	PA9	PA8	PA7

Sound service 1:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
14	NEWFC	F6	F5	F4	F3	F2	F1	F0
15	CW7	CW6	CW5	CW4	CW3	CW2	CW1	CW0
16	CW15	CW14	CW13	CW12	CW11	VW10	CW9	CW8
17	CW23	CW22	CW21	CW20	CW19	CW18	CW17	CW16
18	CW31	CW30	CW29	CW28	CW27	CW26	CW25	CW24
19	CW39	CW38	CW37	CW36	CW35	CW34	CW33	CW32
20	CW47	CW46	CW45	CW44	CW43	CW42	CW41	CW40
21	CW55	CW54	CW53	CW52	CW51	CW50	CW49	CW48
22	X	X	X	X	CW59	CW58	CW57	CW56
23	PA6	PA5	PA4	PA3	PA2	PA1	PA0	NAD
24	X	X	X	L12	L11	PA9	PA8	PA7

Table1 (part 1) Contents of the configuration chain for the MV1732 sound chip

Where :

MIX	Sound mixing 0 : Mixing not required 1 : Mixing required	FMIX	Force mixing 0 : Normal sound mixing controlled by BI packet and MIX bit. 1 : Sound services 1 & 2 will be mixed independent of the BI packet information.
IRE	Reset interrupt request 1 : reset IRQ		
IPO	Interrupt polarity 0 : IRQ active low 1 : IRQ active high		
X	(9..0) andY (9..0) Main Sound and Commentary Sound mixing levels. All hex values between 200 and 0 may be used to obtain intermediate values of attenuation.		

NOTE: The attenuators only work when the chip is in Mixing mode.

X (9..0) and Y (9..0) value in hex and the resulting attenuation in dB.

Value	dB	Value	dB	Value	dB
200	0	073	13	01A	26
1C8	1	066	14	017	27
197	2	05B	15	014	28
16A	3	051	16	012	29
143	4	048	17	010	30
120	5	040	18	00E	31
101	6	039	19	00C	32
0E5	7	033	20	00B	33
0CC	8	02E	21	00A	34
0B6	9	029	22	009	35
0A2	10	024	23	008	36
090	11	020	24	000	OFF
081	12	01D	25		

CW0	-	CW59	Control word, CW for descrambling
F0	-	F6	The seven least significant bits of the frame counter, FCNT
NEWFC			New frame count for descrambling sent (see text)
L12		L11	Selection of the sound service in the subframes
X		1	Subframe 1 only
1		0	Subframe 2 only
0		0	Both subframes
NAD			New address indication (see text) Sound Muted when NAD is low.
PA0	-	PA9	Packet address
X			Don't care bits

Table 1 (continued) Details of configured chain for the MV1732 sound chip

PA0	-	PA9	Packet address, 10 bits
CI0	-	CI1	Continuity index, 2 bits
SFRI			Subframe 1 or 2, 1 bit 0 : Subframe 1 1 : Subframe 2
PT0	-	PT7	Packet type byte, 1 byte (BI1, BI2, BC1, BC2)
D0	-	D719	Sound/control bits, 720 bits

Table2. Packet format on PDATA pin

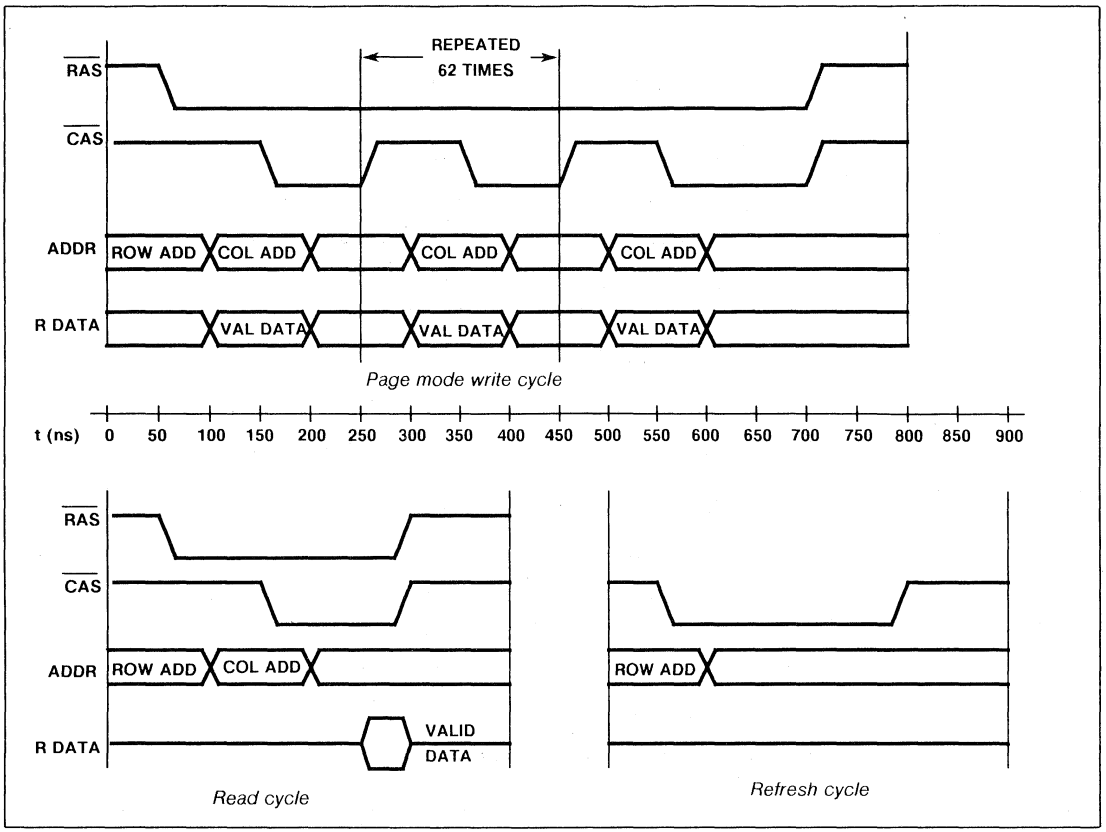


Fig.4 DRAM Signals

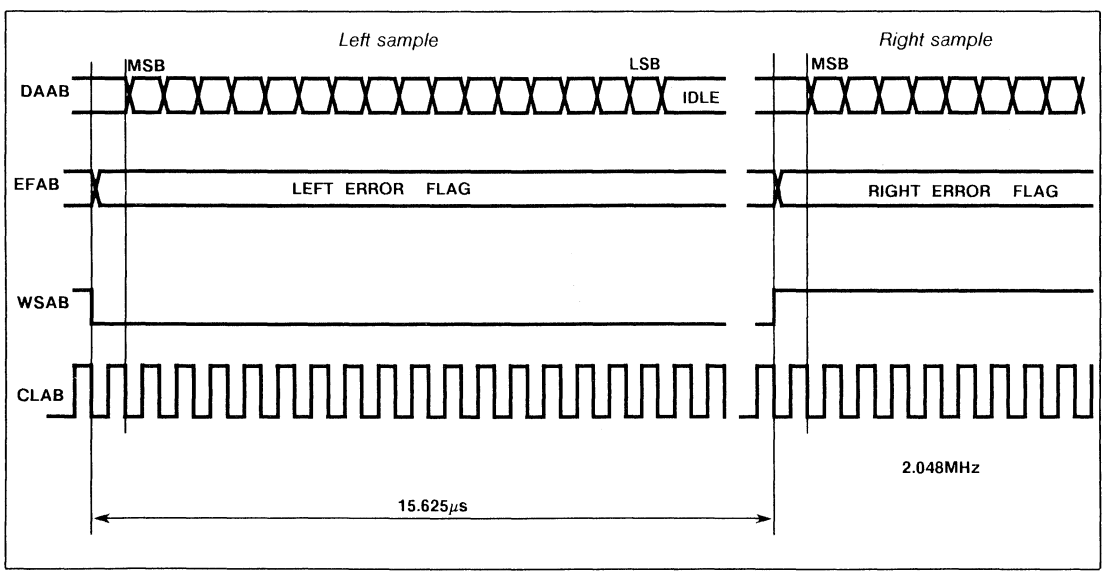


Fig. 5 Sample data output waveforms, I^2S bus

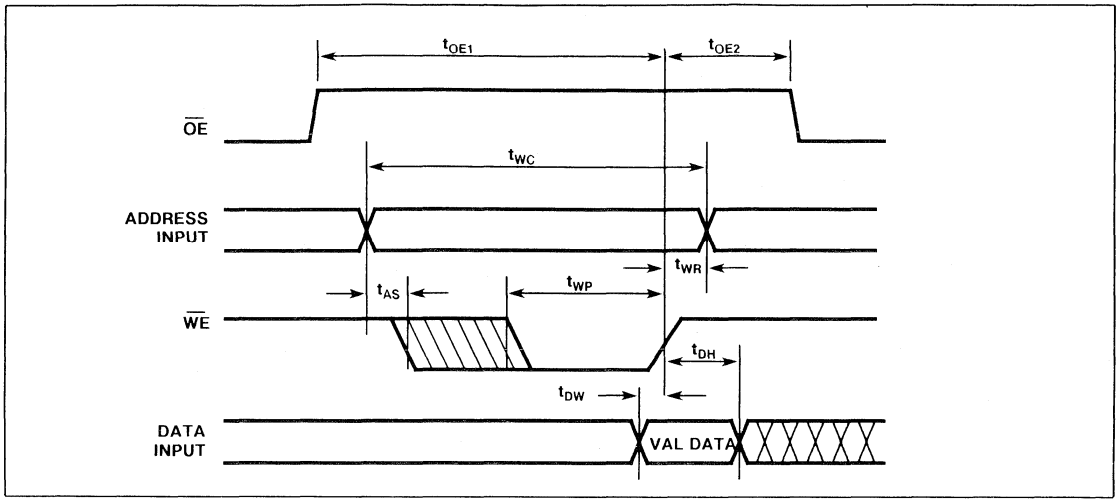


Fig.6 Write cycle $\overline{WE}$ controlled for SRAM

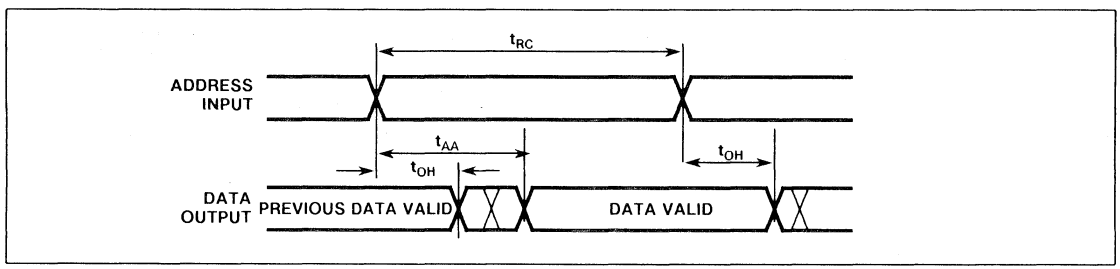


Fig.7 Read cycle (address access) for SRAM

DELAYS ON THE SRAM SIGNALS

Write pulse width	t_{WP}	min 48ns	max 52ns
Address set up time	t_{AS}	min 45ns	
Write recovery time	t_{WR}	min 45ns	
Write cycle time	t_{WC}	min150ns	
Data to write time overlap	t_{DW}	min 45ns	
Data hold from write time	t_{DH}	min 45ns	
Read cycle time	t_{RC}	min 200ns	
Output hold time	t_{OH}	min 0ns	
Address access time	t_{AA}	max 100ns	
$\overline{OE}$ setup time	t_{OE1}	min 295ns	
$\overline{OE}$ hold time	t_{OE2}	min 95ns	

REF. 1.

MAC packet family specifications
EBU No tech 3258-e

ABSOLUTE MAXIMUM RATINGS

(Reference to V_{SS})

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	Tstg	-30	+125	C
Operating Ambient Temp.	Tamb	0	+70	C
Supply Voltage (all supplies)	Vdd	-0.3	+6.5	V
Input Voltage (any input)	VImax	-0.3	V_{DD} + 0.5	V
Output Voltage (any output)	VOmax	-0.3	V_{DD} + 0.5	V
DC input or output diode current	IIOK		+/-20	mA
Output Current (each output)	Iomax		+/-10	mA
Electrostatic Handling (Mil-STD 883C)	Vstat	-2000	+2000	V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0 °C to + 70°C, V_{DD} = 4.75V to + 5.25V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Low input voltage		V_{SS}		1.2	V	
High input voltage		3.4		V_{DD}	V	
Low output voltage				0.4	V	I_{OL} = 4mA
High output voltage		V_{DD}-0.4			V	I_{OH} = -4mA
Output short circuit current		24		96	mA	V_O = V_{DD}
		-12		-48	mA	V_O = V_{SS}
Clock 1 frequency		1		21	MHz	
Oscillator frequency HIGH		8.192		+150ppm	MHz	XC = Low
LOW		8.192		-150ppm	MHz	XC = High
Crystal tolerance		8.192		±30ppm	MHz	

MV1745

MAC TELETEXT CIRCUIT

The MV1745 is a Teletext interface chip for the Nordic VLSI C/D/D2 MAC packet receiver chipset.

The MV1745 is a Teletext decoder capable of decoding VBI and MAC packet Teletext. Packet data is received from the MV1720 control chip. Packets for the desired teletext service are recognised, optionally golay decoded, descrambled and passed to the MV1815 terrestrial Teletext chip.

FEATURES

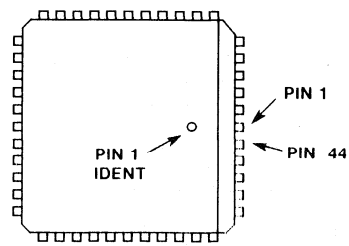
- 44 pin Quad Flatpack and Quad J-Lead Packages
- Packet Address Selection
- Hardware Golay Decoding and Correction for MAC Packets
- Hardware Descrambling
- Allows the Selection of PAL VBI MAC VBI or MAC Packet Text under Software Control
- MAC Packet/VBI Converted to Terrestrial Teletext Standard
- Direct Interface to Terrestrial Teletext device MV1815
- High Degree of Compatibility with SAA1750

ABSOLUTE MAXIMUM RATINGS

SDC supply voltage V_{DD}	-0.3 to +7V
Input voltage	-0.3 to V_{DD} +0.3V (referenced to VSS)
Storage temperature range	-65 to +150°C
Ambient operating temperature	0 to +70°C
Lead temperature	240°C

ASSOCIATED PRODUCTS

SL1700, MV1710, MV1720, MV1732, MV1733 and MV1815



HP44
GP44

Pin	Function	Pin	Function
1	MODE	23	$\overline{\text{MACCS}}$
2	EXT / $\overline{\text{INT}}$	24	$\overline{\text{TCS}}$
3	N/C	25	SAND
4	CLK1	26	TTDMX
5	CDATAOUT	27	TTCMX
6	RESET	28	V_{SS}
7	V_{DD}	29	V_{DD}
8	TEST	30	LDSW
9	CDATAIN	31	SORCS
10	CSTRB	32	$\overline{\text{STTV}}$
11	VBIDAT	33	$\overline{\text{LDSW}}$
12	TTV	34	N/C
13	SIV	35	N/C
14	PDATA	36	N/C
15	VAL	37	N/C
16	EFCNT	38	N/C
17	V_{SS}	39	V_{SS}
18	PALTTD	40	V_{DD}
19	PALTTC	41	N/C
20	$\overline{\text{PALTTC}}$	42	N/C
21	M/$\overline{\text{P}}$	43	N/C
22	PALCS	44	N/C

Fig.1 Pin connections

Note
Pins 18,19,20,22,24,25,30 and 31 are not used with MV1815 application and should be left open circuit.

PIN DESCRIPTIONS

Symbol	Type	Pin	Description
V_{DD}	Supply	7,29,40	System Power: +5V, all pins must be connected.
V_{SS}	Supply	17,28,39	System Ground: 0V, all pins must be connected.
MODE	Input	1	Input to Control the MV1745 interface to teletext chip. HIGH for MV1815 or LOW for ECCT.
EXT / $\overline{INT}$	Output	2	Output connected to EXT/$\overline{INT}$ of the MV1815. When HIGH the MV1815 accepts data and sync from an external source (MAC mode), when LOW the MV1815 uses its data slicer and clock PLL (PAL mode). Programmed by setting M1 bit in the configuration chain or by M / $\overline{P}$ if M2 = 1.
CLK1	Input	4	20.25MHz One Phase master clock. Buffered from SC20M on the SL1700.
CDATAOUT	Output	5	Configuration chain output. Connect to CDATAIN of the next device.
RESET	Input	6	Active HIGH Power up Reset, used to initialise the MV1745. Sets all internal registers to zero.
TEST	Input	8	Test Input. Must be tied to V_{SS} for normal operation.
CDATAIN	Input	9	Configuration chain input from previous CDATAOUT.
CSTRB	Input	10	Strobe Signal from CSTRB on the MV1720. When high, the configuration data is shifted along the configuration chain.
VBIDAT	Input	11	Data from DOUT on the SL1700, source for VBI MAC teletext.
TTV	Input	12	Strobe from TTV on the MV1720, indicates valid VBI data. High from sample 230 to 1294 inclusive.
SIV	Input	13	Sample Strobe, from SIV on the MV1720. Active for UDT, SDF, RDF fields in line 625. Used to latch over data in the configuration chain.
PDATA	Input	14	Packet Data (sound/data/line 625 'packet') from PDATA on the MV1720. 20.25MBits/s spectrum descrambled, deinterleaved and decoded corrected data.
VAL	Input	15	Indicates every Packet Header on PDATA. From VAL on the MV1720. Duration 13 clocks.
EFCNT	Input	16	MSB of Internal Frame (FCNT), from EFCNT on the MV1720. Toggles in bit 3 of line 625 every 128th frame.
PALTTD	Input	18	PAL Teletext Data Input for ECCT mode. Accepts AC coupled sliced data from SAA5231 at 6.9MBits/s. The input is clamped to VSS between 4μs line time, so input data must be guaranteed LOW during this time. In MV1815 mode the input is ignored.
PALTTC	Input	19	Input and output of single inverter. With external biasing resistor, input accepts low level teletext clock from SAA5231 for switching between PAL and MAC teletext sorces. (See Fig. 2.)
$\overline{PALTTC}$	Output	20	
M/$\overline{P}$	Input	21	Input pin controlling the selection of MAC (input high) or PAL (input low) text sources. The effect of this pin can be disabled from the configuration chain, the text source is then controlled by the chain only.
PALCS	Input	22	PAL Composite Sync Input (active HIGH sync pulses). Accepts separate sync from SAA5231 for switching.
$\overline{MACCS}$	Input	23	MAC Composite Sync Level (active LOW sync pulses), from MAC decoder.
$\overline{TCS}$	Input	24	Text Composite Sync (active LOW sync pulse) input from SAA5343 which provides non-inverted sync in text only display modes. It is open circuit in applications using the SAA9041. (See Figs. 3 and 5.)
SAND	Input	25	Sandcastle pulse input. This is a Schmitt trigger input, used to detect the negative edge of the sandcastle pulse from the text decoder, at line time 1.5μ. This input provides horizontial timing references for two reasons. In MAC case, the timing reference is used to time the presentation of the text rows to the decoder, while in the PAL case it is used to time the clamp on the PALTTD input. See Fig. 4.

PIN DESCRIPTIONS

Symbol	Type	Pin	Description
TTDMX	Output	26	Teletext Data output. This comprises a complete line 45 bytes as defined in WST Fig. 2. -ref 2. This includes bytes 1 and 2 clock run in, then byte 3 framing code (27 hex), then bytes 4 and 5 magazine and packet address, followed by 40 bytes of teletext data. This output is low between 4μs and 8μs line time or compatable with SAA5243/9041 teletext decoders. (See Fig. 2.) In ECCT mode data starts to be outputs 8.5μs after negative line sync pulse edge. Data rate is 6.75MBits/s. In MV1815 mode when the text source is PAL, this output goes high impedance.
TTCMX	I/O	27	In ECCT mode, this pin is an output. It used to output the teletext clock. Data on TTDMX is clocked out of the MV1745 on the negative edge of this clock at 6.75MHz. In MV1815 mode, this pin is an input, Teletext data is clocked out of the MV1745 by a 6.9375MHz clock provided by the MV1815 (pin XCK4). Data on TTDMX is clocked out of the MV1745 on the negative edge of this clock. (See Fig. 5.)
LDSW	Output	30	Load Switch output. Open drain N-channel output which switches a load to ground from the SAA5231 $\overline{\text{STTV}}$ pin. This allows MAC composite sync to be switched in as the reference for the display clock PLL. In this case LDSW will be high impedance.
SORCS	Output	31	Source Composite Sync output (active HIGH sync pulse), derived from the currently selected broadcast input. Used to provide the vertical acquisition timing to the text decoder. Connect to the VCS input of the SAA5243 or the VSA input of DTB SAA9041. (See Figs. 3 and 5)
$\overline{\text{STTV}}$	Output	32	Composite Sync output (active LOW sync pulses) In ECCT mode it provides either text or broadcast sync to TV timebase, controlled by the $\overline{\text{TCS}}$ input. In MV1815 mode it provides syncs to the SYNCIO pin. (See Fig. 4.) In MV1815 mode when the text source is PAL, this output goes high impedance.
$\overline{\text{LDSW}}$	Output	33	Inverted Load Switch output with CMOS level

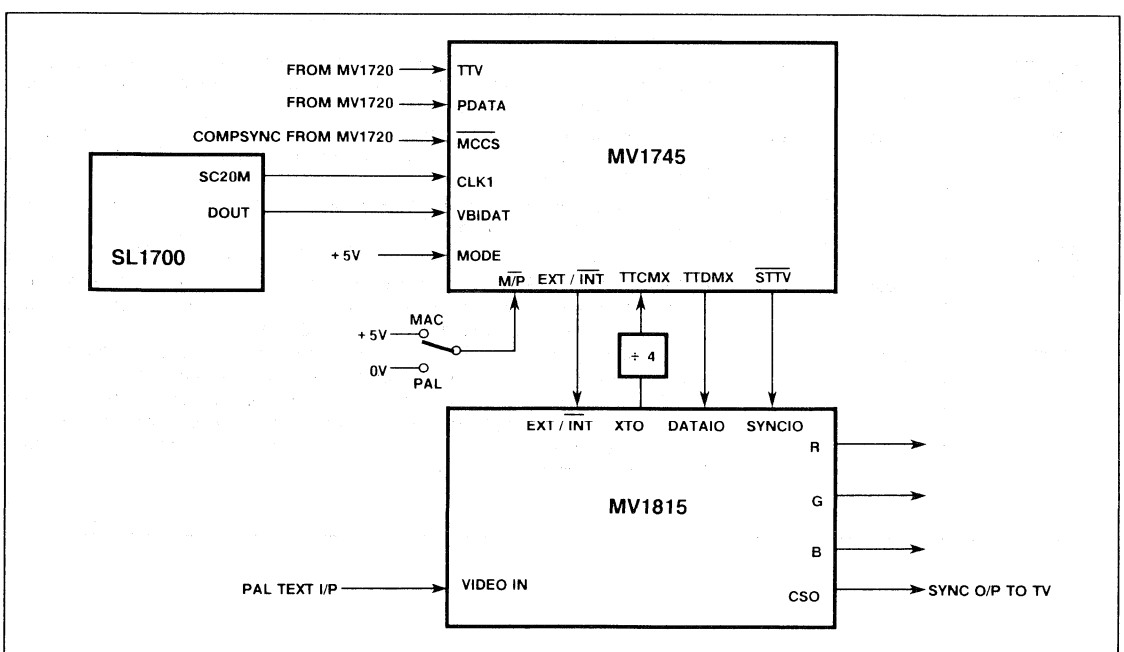


Fig.2 MV1745 interface to MV1815

MAC Packet Receiver

The packet header control provides for packet reception and timing for packet processing. Packet data arrives serially at 20.25MBits/s on pin PDATA from the MAC control chip. As default in the MAC system, LSB is transmitted first. The packet data format is shown in table.1

The total packet length is 751 bits. The packet header, bits 0-12, is flagged by VAL.

The packet address of each packet is compared with the target address of the configuration chain, and packets which match address and sub-frame indication are forward to the descrambling block. The PT-byte is Hamming decoded.

Both D and D2 MAC packet teletext can be recovered.

PA4	PA3	PA2	PA1	PA0 ←Sent first			
SFRI	CI1	CI0	PA9	PA8	PA7	PA6	PA5
PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0
CB81	CB71	CB61	CB51	CB41	CB31	CB21	CB11
ROW1							
CB82	CB72	CB62	CB52	CB42	CB32	CB22	CB12
ROW 2							

Table.1 Packet format of the data stream on PDATA pin.

Where:

PA0-PA9	-	Packet address.
PT0-PT7	-	Packet type byte.
B11-CB81	-	Control byte 1.
B12-CB82	-	Control byte 2.
CI10-CI1	-	Continuity index.
SFRI	-	Sub-frame index.
ROW 1	-	2 bytes magazine and ROW - address + 40 character bytes + 2 bytes CRC.
ROW 2	-	2 bytes magazine and ROW - address + 40 character bytes + 2 bytes CRC.

Descambler

The packet type byte in the packet header contains access control information for the descambling system all three different levels of access control described in the MAC standard are supported. Legal values of the PT byte are:

- 00 : Unscrambled; the text data is forwarded unchanged
- C7 : Scrambled free access; the text data is descrambled with a local control word stored in the receiver
- F8 : Scrambled controlled access; the text data is descrambled with a regenerated control word from the encryption system
- 3F : Unused

The control word for descrambling is provided by the configuration chain.
It is possible to switch from unscrambled to scrambled packets in the same frame, but it is not possible to switch between scrambled free access and scrambled controlled access in the same frame, as this last operation would require an additional descrambler.

The descrambler can operate on a teletext service placed in one sub-frame. It can also operate on a teletext service placed in two sub-frames if the following conditions are true:

The sub-frames must have the same width.
The following packets can not have the same position in both sub-frames.
The teletext data in both sub-frames must be scrambled with the same control word.

An eight bit frame counter is maintained on chip for deriving the initialisation word. The signal EFCNT is the most significant bit of the frame counter. The counter is preset by a transition in EFCNT and incremented every frame by SIV.

The frame counter may be loaded by the configuration chain, to assure fast recovery after a change of channel or power-up.

Golay Decoder

The Golay decoder receives MAC packet bodies (all header and PT byte) from the descrambler. Packet test services can be transmitted at two different levels of error protection. The TP bit in the configuration chain determines whether first or second protection (Golay) is transmitted.

At the first level of protection, two text lines (teletext data blocks) are transmitted per MAC packet. The format of a text line is:

One control byte, two MAAG bytes, 40 data bytes and two CRC bytes.

The control byte and the two CRC bytes are ignored, and two lines, each 42 bytes long, are forwarded to the output buffer.

At the second level of protection, one text line is transmitted per MAC packet. The packet now consists of only one text line, but with 30 golay words of 12 bits inserted. The Golay decoder is able to correct up to three errors in the 12 information bits of each Golay word (24,12)

The control byte and the two CRC bytes of the teletext data block are removed; only the teletext packet (42 bytes) is sent to the output buffer.

D2 MAC VBI Interface

This port is provided to permit acquisition teletext at 10.125MBits/s from D2 MAC transmissions. It accepts data directly from the MAC decoder data demodulator on the VBIDAT pin. A strobe signal on the TTV pin marks the interval (samples 532 - 1292) of lines that may contain teletext. The format of a text line is: Two clock run-in bytes, one framing code byte, The MRAG bytes and 40 data bytes, which gives a total of 360 bits.

The run-in bytes are ignored but the framing code is checked. The teletext line is acepted if the framing code equals the binary number 11100100 (left hand bit received first) (ref.2) When a framing code is accepted, the two MRAG bytes and 40 data bytes are forwarded to the output buffer, otherwise the line is skipped.

Output Buffer

The output buffer stores the complete teletext line of 45 bytes and clocks then out at 6.7375MHz in the MV1816 mode and 6.75MHz in the ECCT mode. In both cases the clock run-in and framing code are added to the teletext data. The format of a text line is :

Two clock run-in bytes, one framing code byte, two MRAG byte and 40 data bytes, which gives a total of 360 bits.

The Configuration Chain

The configuration chain is effectively a long shift register running through all circuits which are to be configured from the MAC microcomputer Several function blocks of the MV1745 are controlled by the configuration chain. The packet control block needs the packet address and an identifcation of which sub-frame (or both) to select packets from. The configuration chain also provide control words for descrambling.

In addition, the seven least significant bits of the frames count (FCNT) and one bit (NEWFC) including update of the frame count after a change of service or power up, are placed in the configuration chain.The configuration chain maybe updated from the microprocessor at any time except in line 625 and line 1. The configuration data is clocked into the chain when CSTRB is high, otherwise the contents of each register stage is stored.

Byte	Bit 7	Bit 6	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	NEWFC	F5	F5	F3	F2	F1	F0
1	CW7	CW6	CW5	CW3	CW2	CW1	CW0
2	CW15	CW14	CW13	CW11	CW10	CW9	CW8
3	CW23	CW22	CW21	CW19	CW18	CW17	CW16
4	CW31	CW30	CW29	CW27	CW26	CW25	CW24
5	CW39	CW38	CW37	CW35	CW34	CW33	CW32
6	CW47	CW46	CW45	CW43	CW42	CW41	CW40
7	CW55	CW54	CW53	CW51	CW50	CW49	CW48
8	EN	X	X	CW59	CW58	CW57	CW56
9	PA7	PA6	PA5	PA3	PA2	PA1	PA0
10	GOL	M0	M1	L1	L2	PA9	PA8

Table.2 Contents of the configuration chain for MV1745. Note that F0 is transmitted first and GOL last.

NEWFC - New frame count for descrambling.
F0-F6 - The 7 least significant bits of the frame count.
CW0-CW59 - Control word for descrambling.
EN - Enable MAC text acquisition.
(0 - acquisition disabled, TTDMX = 0)
(1-acquisition enabled, TTDMX carries data)
PA0-PA9 - Packet address.
GOL - Golay decoder packet if GOL = 1.

M0 - Type of teletext input.
- 0 - VBI.
- 1 - packet.

M1 - Teletext source, controls output EXT / INT to MV1816.
- 0 - PAL (terrestrial).
- 1 - MAC.

M2 - Enable M/P instead of M1.
(0 gives PAL/MAC selection to bit M).
(1 gives PAL/MAC selection accoding to pin M/P).

L2 - L1 - Selection of sub-frame.
0 - 0 - Both sub-frasmes.
X - 1 - Sub-frame 1 only.
1 - 0 - Sub-frame 2 only.

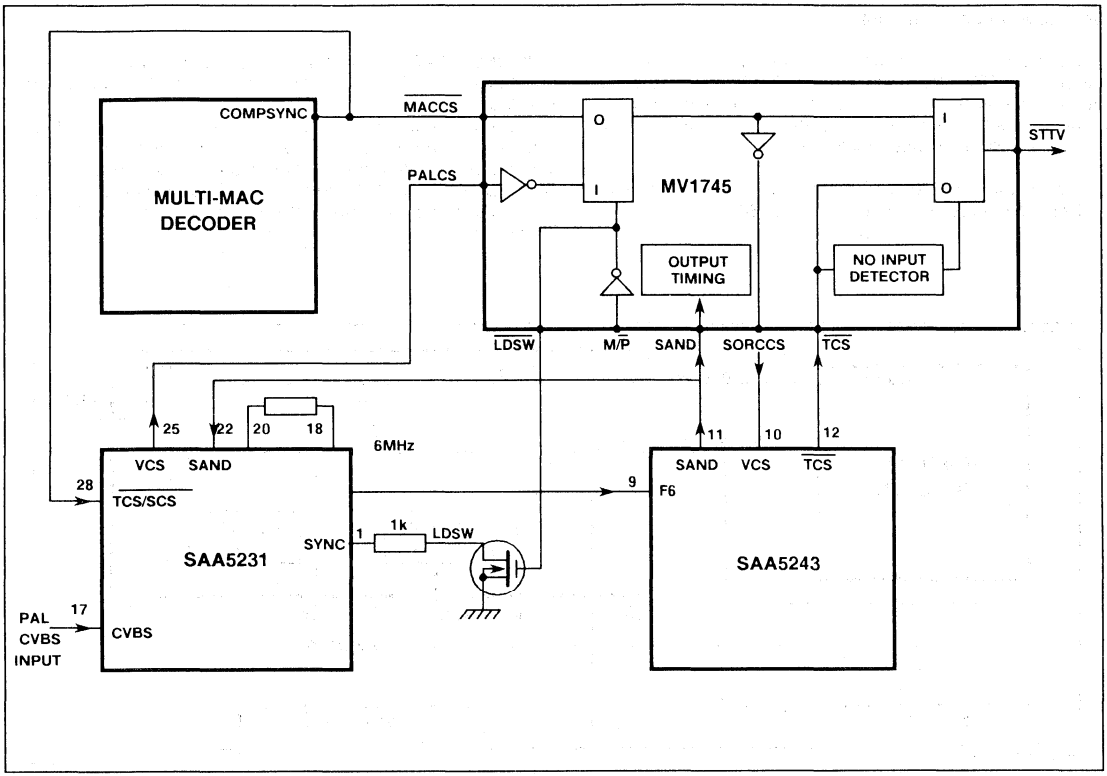


Fig.3 MV1745 Sync System with SAA5243

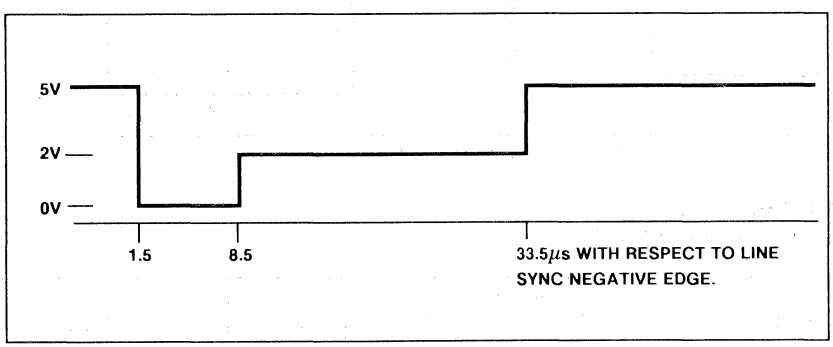


Fig.4 Sandcastle Waveform

Configuration chain update

After power up or change of service the corresponding control word, CW , for descrambling should be transmitted in the configuration chain as soon as a valid control word is available, together with the 7 LSB's of the frrame count FCNT (the MSB is provided by EFCNT)

If you control bit NEWFC = 1, the descrambling control word will be updated in the first line 625 (SIV = 1)

If NEWFC = 0, the descrambling control word will be updated when EFCNT changes from '1' to '0' in the next line 625

Thus, in a stable state it is not necessary to provide the CW every frame. After power up or change of service, new address and sub-frame indication should be provided at the same as the new CW and FCNT. The contents of the configiration chain for the MV1745 teletext chip are shown in Table.2

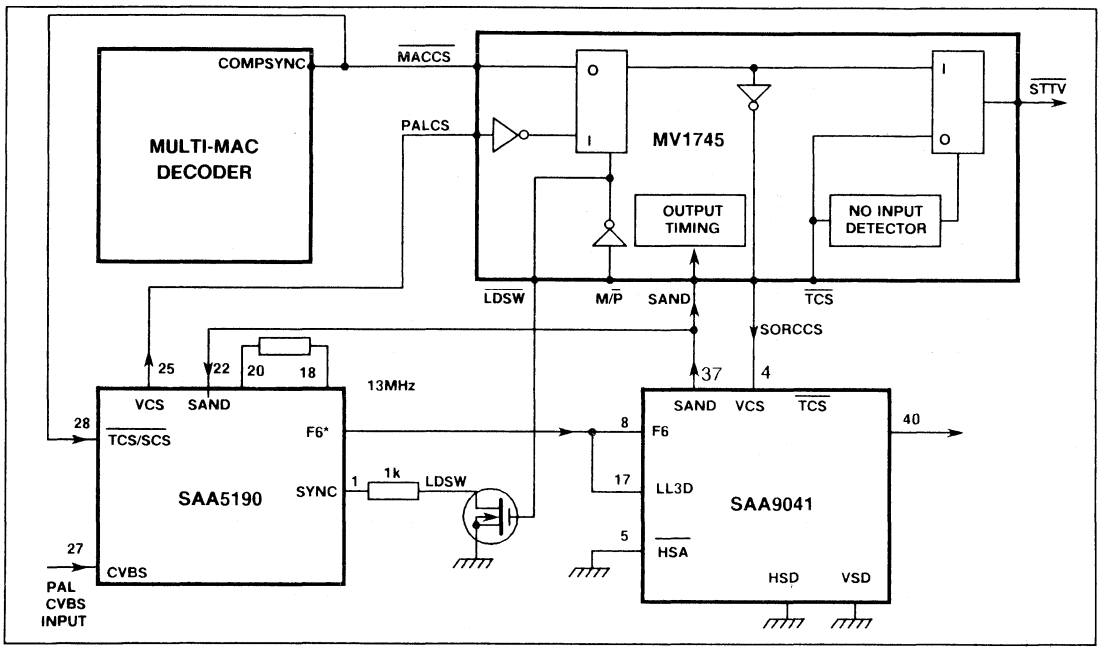


Fig.5 MV1745 Sync System with SAA9041

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 0°C to +70°C, V_{DD} = +4.75 to +5.25V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Low input voltage	V_{SS}		1.2	V	
High input voltage	3.4		V_{DD}	V	
Low output voltage			0.4	V	I_{OL} = 10mA
High output voltage	V_{DD}-0.4			V	I_{OH} = -10mA
Clock 1 frequecy	1		21	MHz	

SL1700

MAC SIGNAL INPUT PROCESSOR AND DATA RECOVERY CIRCUIT

The SL1700 is a signal input processor and data recovery circuit for use in multistandard (D/D2/CMAC) MAC decoders. The SL1700 incorporates a video buffer with AGC and grey level clamping, an adaptive data slicer, and a 20.25MHz phase locked fundamental crystal oscillator. The output from the oscillator is buffered and divided to provide clock outputs of 20.25MHz and 10.125MHz.

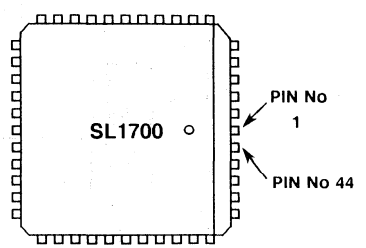
Associated GEC Plessey Semiconductors devices are MV1710, MV1720, MV1732, MV1733, MV1745, SP973T8, MV95338, VP101.

FEATURES

- Data and Clock Recovery for C/D/D2MAC Decoders
- Crystal Oscillator at 20.25MHz
- Video Amplifier with 6dB AGC Range
- Generates Voltage Reference Levels for the SP973T8 Video ADC
- Binary or Duo-binary Data Slicing
- 20.25MB/s and 10.125MB/s Data Rate
- Buffered System Clock with Outputs of 20.25MHz and 10.125MHz
- 44-pin 'J' lead Plastic Chip Carrier Package

ABSOLUTE MAXIMUM RATINGS

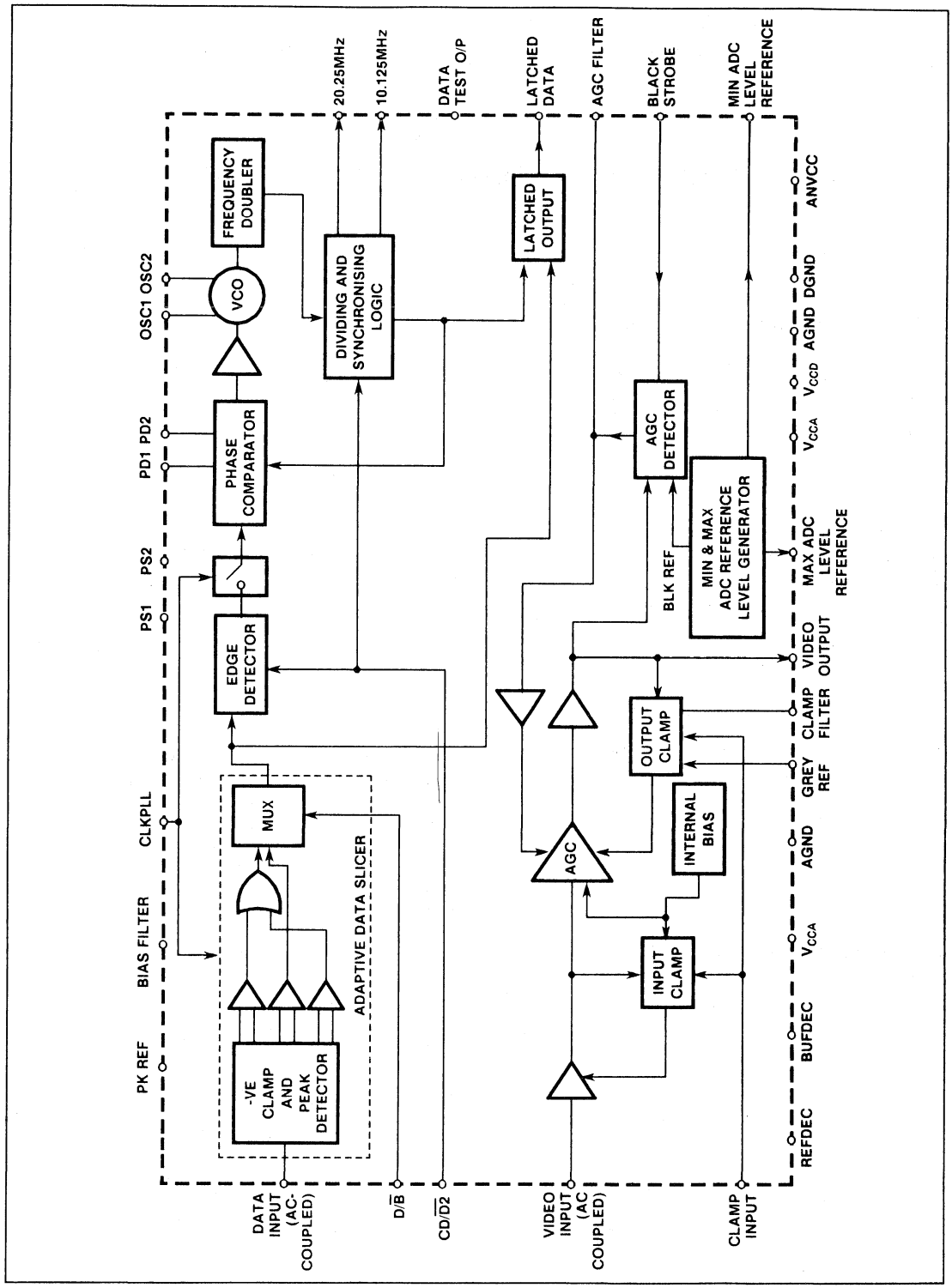
Analog supply voltage V_{CCA}	-0.3 to +12V
Digital supply voltage V_{CCD}	-0.3 to +6.5V
Storage temperature range	-55 to +125°C
Operating temperature range	0 to +70°C



HP44

Pin No.	Description	Pin No.	Description
1	OSC2	23	10MHz
2	N/C	24	20MHz
3	OSC1	25	CLAMP INPUT
4	ANALOG GND	26	BIAS FILTER
5	PD1	27	V_{CCA}(+10V)
6	PD2	28	VIDEO IN
7	N/C	29	N/C
8	PS1	30	DATA TEST O/P
9	PS2	31	O/P CLAMP FILTER
10	N/C	32	AGC FILTER
11	CD / $\overline{D2}$	33	GREY REF
12	D / $\overline{B}$	34	BLK STRB
13	N/C	35	N/C
14	DATA IN	36	N/C
15	PK REF	37	VIDEO OUT
16	REFDEC	38	ANALOG GND
17	ANVCC	39	N/C
18	N/C	40	ADC MIN. REF
19	V_{CCA}(+10V)	41	ADC MAX. REF
20	LATCHED DATA	42	N/C
21	CLK PLL	43	DIGITAL GND
22	V_{CCD}(+5V)	44	BUF DEC

Fig.1 Pin connections - top view
NOTE: N/C = No Internal Connection



Simplified block diagram of SL1700

FUNCTIONAL DESCRIPTION

The SL1700 provides the recovery of digital data, binary or duo-binary, and cancels the energy dispersal modulation. It also incorporates video processing with grey level clamping and AGC. The crystal oscillator is phase locked to the incoming data.

Data Slicer

The circuit incorporates an adaptive data slicer. The clamp circuits operate directly on the peak to peak excursions of the data input. The capacitors connected to the DATA and PK REF pins store the min and max data signal levels respectively. The data slicer operates at a 50% level for binary (D/$\overline{B}$ low) and at nominal 25% and 75% levels for duo-binary (D/$\overline{B}$ high).

Video Amplifier

The aim of the video circuitry is to pre-condition the MAC video signal (to a nominal level of 1.6Vp-p and 3.3V grey level) which is then input to the system ADC. The AGC circuitry utilises the internally generated black level reference. After the MAC control chip (MV1720) has achieved lock, correctly positioned CLAMP pulses are supplied to the SL1700 from the MV1720 and BLKSTRB pulses are supplied from the MV1710.

The CLAMP pulse gates the video clamp circuits when grey level occurs in the video waveform. Similarly, BLKSTRB gates the video AGC circuit when black level occurs in the video signal. The video amplifer is non-inverting with a minimum AGC range of 6dB.

ADC Minimum and Maximum Level References

Both minimum and maximum level references are generated on-chip. These references are used to drive each end of the external video ADC potential divider chain. The most suitable ADC for MAC is the SP973T8. The divider chain of the SP973T8 is centre tapped to provide a grey level reference used by the video clamp circuits. The black level reference (derived from the minimum level) is inset internally by approximately 15% to reduce the probability of clipping the video signal in the presence of overshoot.

Oscillator and Phase Comparator

A 20.252MHz crystal oscillator is connected to pin 1. A transition detector ensures that the oscillator is correctly phase locked to the incoming data stream which, via dividers and buffers provides the 20.25MHz and 10.125MHz system clock outputs.

Data Recovery

The latched data is re-synchronised with respect to the selected clock output (either 20.25MHz or 10.125MHz by means of the CD/$\overline{D2}$ input) as shown in Fig. 3. This ensures that adequate setup and hold times are available for the MV1720 control chip. The data output changes on the falling edge of the clock and is latched into the MV1720 on the rising edge of the clock.

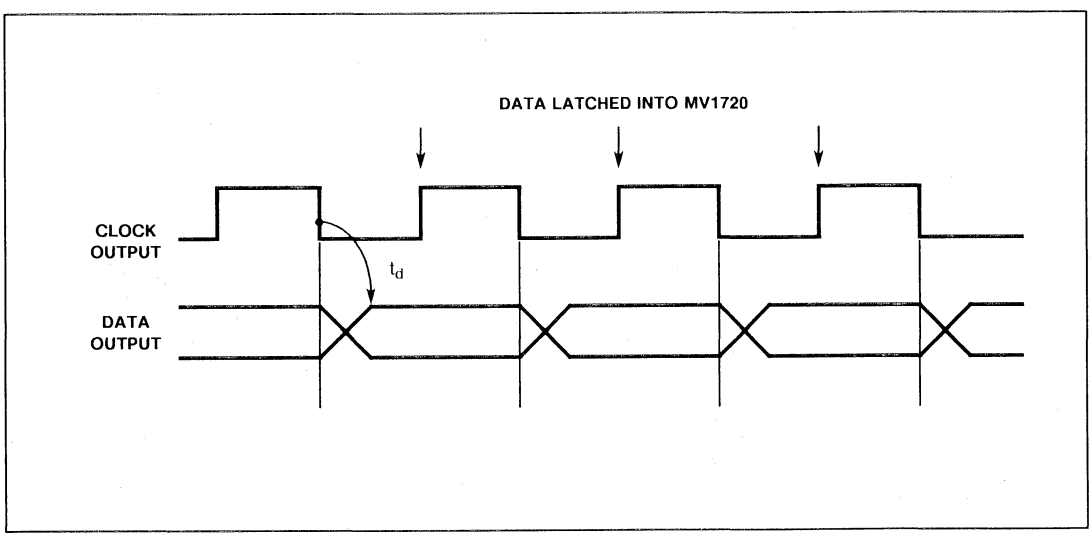


Fig.3 Data sampling

ELECTRICAL CHARACTERISTICS

Test Conditions (unless other wise stated)

T_{amb} = 25°C, V_{CCA} = 10V ± 5% on pins 27,19. V_{CCD} = 5V ± 5% on pin 22

Characteristic	Pins	Symbol	Value			Units	Conditions
			Min.	Typ.	Max.		
Total analog supply current	27,19	I_{CCA}			90	mA	Inputs and outputs floating
Digital supply current	43	I_{CCD}			63	mA	
CD/D2 input	11	I_{IH}			± 10	µA	$V_{IH} = V_{CCD}$, V_{IL} = 0V
		I_{IL}		-1.08	-1.54	mA	
BLK STRB input and CLAMP input	34,25	I_{IH}		583	833	µA	
		I_{IL}			± 10	µA	
CLK PLL input	21	I_{IH}		7.5	11	µA	
		I_{IL}			± 10	µA	
D/B input	12	I_{IH}		-43	-61	µA	
		I_{IL}		-575	-821	µA	
TTL outputs	23,24, 20,30	V_{OH}	V_{CCD}-1V			V	I_{OH} = -5.0µA
		V_{OL}			0.5	V	I_{OL} = 1.6mA
Data input voltage (p-p)	14	V_D			1.2	V	
		Input Z	1			MΩ	
Video input voltage (p-p)	28	V_V	0.44		1.2	V	
		Input Z	1			MΩ	
Grey level input voltage (p-p)	33	V_G		3.3		V	
ADC max. ref O/P	41	V_W		4	4.3	V	I_{source} = 8mA Max. measured at DC
ADC min. ref O/P	40	V_B	2.0	2.3		V	I_{sink} = 8mA Max. measured at DC
Video Output	37						C_{LOAD} = 40pF
Amplitude (p-p)				1.4		V	
Source Z					20	Ω	
AGC range			6	8.9		dB	V_{IN} = 0.44Vp-p
Max. gain (Note 1)				3.2			V_{IN} = 1.2Vp-p
Min. gain (Note 1)				1.2			V_G = 3.3V
TILT (Note 2)				0.1			V_{IN} = 0.6Vp-p
Integral LIN (Note 3)				1			
VCO							See Table 1
Temperature coefficient		Δfo/ΔT		-2.3		ppm/°C	Note 4
VCO gain		KO		7		ppm/mV	Note 5
Phase Locked Loop							See Table 1
Total capture range				300		ppm	Note 6
Total hold range				600		ppm	Note 6
Clock output to data valid		t_d		10		ns	Measured from mid point on active edge of clock to mid point of data edge.
Rise time	20,	t_r		7		ns	10-90% C_{LOAD} = 15pF
Fall time	23,24	t_f		5		ns	90-10% C_{LOAD} = 15pF

NOTES

1. The gain is measured between VIDEO IN and VIDEO OUT with grey reference input = 3.3V.
2. Tilt refers to the degree of droop during one line period of a constant white level which is specified as a percentage of the black to white swing. Tilt is measured at VIDEO OUT.
3. Integral LIN is the peak deviation from a linear ramp between black and white during one line period and is specified as a percentage of the black to white magnitude.
4. The specified temperature coefficient includes the crystal, load capacitor and device effects.
5. Measured using a 20.252MHz series resonant crystal.
6. Measured with loop filter as shown in Fig. 4 on pins 4 and 5 with 1Vp-p MAC composite signal applied to the data input using the mid grey pattern from a Schlumberger SI7765 MAC signal generator, DMAC selected and CLKPLL held high.

Parameter	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Series Resonant						
fs = 20.2520MHz						No Load Cap
Series resistance at resonance			10		Ω	
Motional L				2	mH	
Motional C				0.06	F	

Table 1 Crystal specification

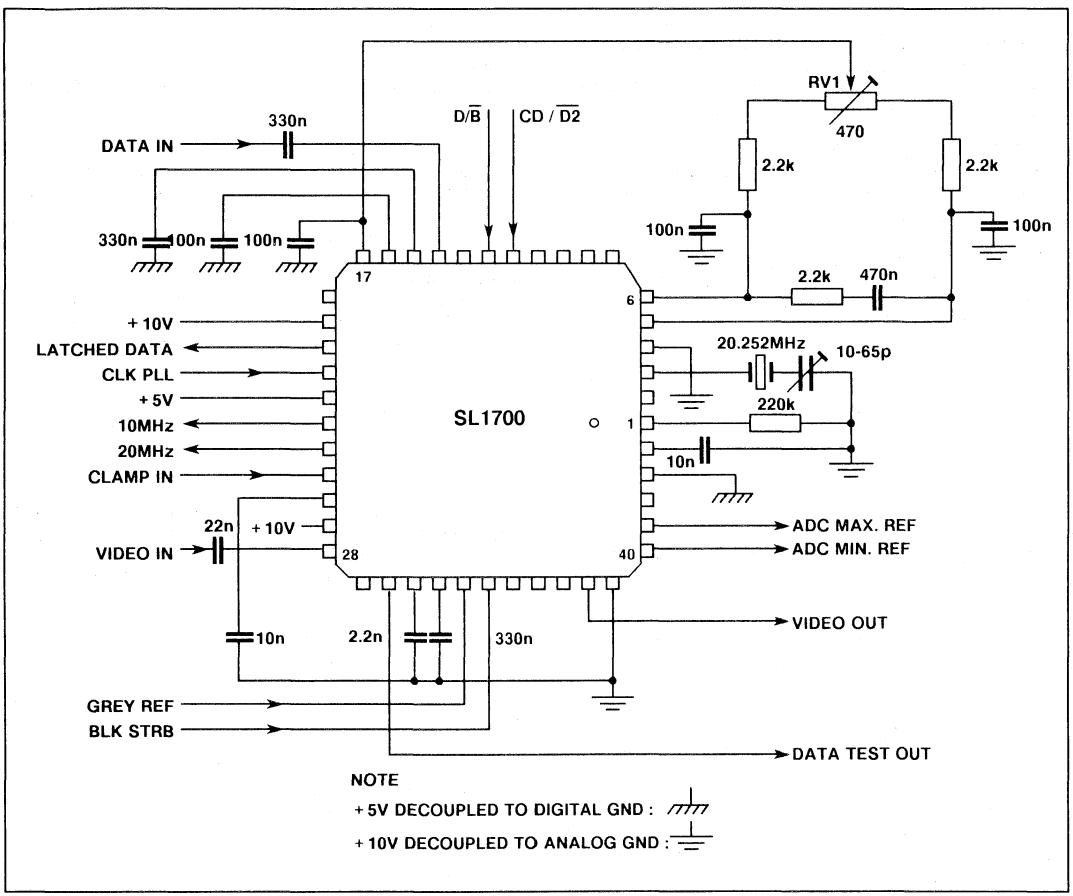


Fig.4 SL1700 test circuit

APPLICATION NOTES

Power Supplies
Pins 19 and 27 are the analog V_{CC} pins (10V ± 5%) and pin 22 the digital V_{CC} pin (5V ± 5%). Pins 4,38 are the analog GND pins and pin 43 the digital GND. Separate analog and digital ground planes should be used, with the analog circuitry decoupled to the analog GNDs.

Voltage Controlled Oscillator (Pin 3)
The oscillator is designed to operate with a series fundamental resonant crystal. The crystal specification is detailed in Table 1.

To adjust the free running frequency of the oscillator, first short pins 5 and 6 together and adjust the trimmer capacitor for a frequency of 20.253MHz. Remove short on pins 5 and 6, then short together pins 8 and 9 and adjust RV1 (shown in Fig, 4) for a frequency of 20.253MHz.

PHASE SHIFT (Pins 8 and 9)
These pins should be shorted together when setting up the free running frequency of the oscillator no components are connected to these pins.

PHASE DETECTOR (Pins 5 and 6)
A low pass filter is connected at pins 5 and 6. Selection of the filter components will determine the capture and hold in range of the phase locked loop.

CD/D2 (Pin 11)
This TTL input is set high for CMAC or DMAC (20.25MBS) and low for D2MAC (10.0125MBS) operation.

D/B (Pin 12)
This TTL input is set high for duo-binary operation and low for binary operation.

Data In (Pin 14)
The MAC input signal is AC coupled to this pin via a 330nF capacitor.

PK REF (Pin 15)
A 330nF capacitor should be connected from PK REF to digital GND. The capacitor is required for the MAC data clamp circuitry.

Latched Data (Pin 20)
The latched data is TTL compatible using a totem pole output circuit.

CLKPLL (Pin 21)
The CLK PLL pulse from the MV1720 gates the PLL and the adaptive data slicer so that both sections of the SL1700 are active only during the data packet portion of the MAC signal.

10MHz Output (Pin 23)
The 10MHz system clock is TTL and CMOS compatible.

20MHz Output (Pin 24)
The 20MHz system clock is TTL and CMOS compatible.

ANVCC (Pin 17)
A decoupling capacitor from this pin to analog GND is required to decouple the on chip regulated supply a 100nF capacitor should be used.

REFDEC (Pin 16)
A decoupling capacitor from this an to analog GND is required to decouple the on chip reference generator. A 100nF capacitor should be used.

Clamp Input (Pin 25)
When clamp input is high, the SL1700 clamps the video to the grey level. See the MV1720 data sheet for timing information.

Video In (Pin 28)
The MAC input signal is AC coupled to this pin, via a 22nF capacitor with a minimum p-p value of 600mV.

Clamp Filter (Pin 31)
A 2.2nF capacitor should be connected from this pin to analog ground.

AGC Filter (Pin 32)
A 22nF capacitor should be connected from this pin to analog ground. This capacitor holds the video AGC levels between samples. It is recommended that a low leakage ceramic capacitor is used.

ADC Minimum Level Reference (Pin 40)
A buffered reference voltage (2.3V min) is provided for the SP973T8 ADC potential divider chain. This reference voltage is also used internally by the video AGC circuitry.

BLKSTRB (Pin 34)
When BLKSTRB is high, the SL1700 enables the AGC detector. See the MV1710 data sheet for timing information.

Video Output (Pin 37)
The signal output at pin 37 is an amplified version of the signal input at pin 28. The grey level of the video output is controlled by the grey level reference input at pin 33. The amplitude is controlled (via the AGC loop) by the internally generated black reference.

Grey Reference Input (Pin 33)
A reference voltage (3.3V nom) as derived from the ADC potential divider chain provides the reference to which the video output clamp adjusts the DC level of the MAC signal output.

ADC Maximum Reference (Pin 41)
A buffered reference voltage (4.3V max) is provided for the SP973T8 ADC potential divider chain.

BIAS FILTER (Pin 26)
A decoupling capacitor from this pin to analog GND is required to decouple the on-chip bias generator. A 10nF capacitor should be used.

BUF DEC (PIN44)
A decoupling capacitor from this pin to analog GND is required to decouple the supply to the oscillator circuit. A 10nF capacitor should be used.

DATA TEST OUTPUT (Pin 30)
This is a test pin providing access to the unlatched data output. The pin is TTL compatble using a totem pole output circuit.

MV95308

30MHz 8-BIT CMOS VIDEO DAC

The MV95308 is a CMOS 8-bit, 30MHz Digital to Analog converter, designed for use in both video graphics and general digital television applications.

A very low external component count has been achieved by including the loop amplifer and reference voltage source on chip.

The device contains a data input register and registered video controls (BLANK, REFWHITE, OVERBRT and SYNC). These control inputs and associated internal circuitry allows the MV95308 to be used in video graphics systems by providing the necessary video pedestal levels. The STRDAC input allows the video pedestals to be disabled in conventional DAC applications.

This device is capable of directly driving 75Ω lines with standard RS-343A or RS-170 video levels, using the appropriate R_{SET} external resistor.

Pull up resistors have been added to tie all unused control inputs into their inactive (High) states.

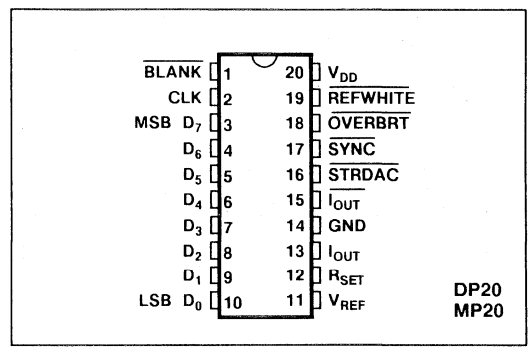


Fig.1 Pin connections - top view

FEATURES

- Low Power Consumption(180mW Typ)
- 30MHz Pipeline Operation
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- RS-343A/RS-170 Compatible Levels
- On Chip Reference Voltage Source
- Guaranteed Monotonic
- Drives 75Ω Loads Directly
- Single 5V Power Supply

APPLICATIONS

- Data Conversion (general)
- Computer Graphics
- Waveform Synthesis
- Consumer TV
- Instrumentation

ORDERING INFORMATION

MV95308 CDP (Commercial - Plastic DIL Package)
MV95308 CMP (Commercial - Miniature Plastic DIL Package)

ABSOLUTE MAXIMUM RATINGS (Reference to GND)

DC Supply Voltage, V_{DD}	-0.3V to +7V
Digital Input Voltage	-0.3V to V_{DD} +0.3V
Analog Output Short Circuit Duration	Indefinite
Ambient Operating Temperature	0°C to +70°C
Storage Temperature Range	-55°C to +125°C

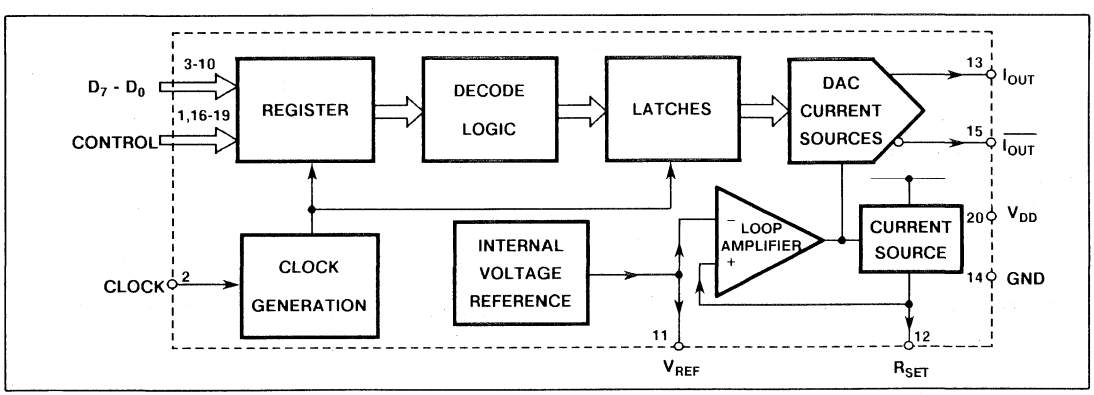


Fig.2 Block diagram of MV95308

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
As specified in recommended operating conditions. Full temperature range = 0 to 70°C

DC CHARACTERISTICS

Characteristic	Symbol	Temp (°C)	Value			Units	Conditions
			Min	Typ	Max		
Resolution		Full	8			Bits	
Integral Linearity Error	INL	25		±0.5		LSB	
		Full			±1	LSB	
Differential Linearity Error	DNL	25		±0.5		LSB	
		Full			±1	LSB	
Gain Error		25		±1%	±5%	%	Of Full Scale
Analog Output							
Grey scale Current range		25		8.8		mA	75Ω Singly Terminated Load R_{SET} = 1.8kΩ (Graphics Mode)
				255		LSB	
10% Over Bright Level Relative to White Level		25	26	27	28	LSB	
				10		IRE	
White Level Relative to Blank Level		25	275	276	277	LSB	
				100		IRE	
Black Level Relative to Blank Level		25	20	21	22	LSB	
				7.5		IRE	
White Level Relative to Black Level		25		255		LSB	
				92.5		IRE	
Blank Level		25	107	111	115	LSB	
				40		IRE	
Sync Level		25		0		LSB	
LSB Size	LSB	25		2.58		mV	
Output Compliance	V_{OC}	25	-0.3		+1.5	V	
DIGITAL INPUTS							
High Level I/P Voltage	V_{IH}	25	3		V_{DD} +0.3	V	
Low Level I/P Voltage	V_{IL}	25	GND -0.3		1.2	V	
High level I/P Current	I_{IH}	25			+1	µA	
Low Level I/P Current	I_{IL}	25			-1	µA	
Internal Voltage Reference (V_{REF})	V_{REF}	25	0.95	1.0	1.05	V	
		Full	0.90		1.10	V	
V_{REF} Temperature Coefficient				40		ppm/°C	

AC CHARACTERISTICS (Refer to Fig. 3)

Characteristic	Symbol	Temp (°C)	Value			Units	Conditions
			Min	Typ	Max		
Max Clock Rate	f_{MAX}	Full	30			MHz	Maximum Guaranteed Freq.
Clock High Time	t_{CLKH}	25	10			ns	
Clock Low Time	t_{CLKL}	25	10			ns	
Data and Control Setup Time	t_{SU}	25	8			ns	
Data and Control hold Time	t_H	25	2			ns	
Analog Output Delay	t_{DLY}	25		10		ns	
Analog Output Rise/Fall Time	t_{RF}	25		3	6	ns	
Analog Output Settling Time	t_S	25		15		ns	
Glitch Energy		25		100		pV-sec	
V_{DD} Supply Current	IDD	25		30		mA	fc = 15MHz
				36		mA	fc = 30MHz

THERMAL CHARACTERISTICS

Thermal Resistance	DP	MP	
Chip to Case θ_{jc}	20	30	°C/W
Chip to Ambient θ_{jA}	75	93	°C/W

RECOMMENDED OPERATING CONDITIONS

R_{LOAD} (I_{OUT} and I_{OUT})	75Ω
V_{DD}	5.0V ±0.5V
R_{SET} (Graphics Applications)	1.8kΩ
R_{SET} (Straight DAC Applications)	1.2kΩ

CIRCUIT DESCRIPTION

As illustrated in the function block diagram, Fig. 2, the MV95308 contains an 8-bit D-to-A converter, input registers, a loop amplifier and a voltage reference.

On the falling edge of each clock cycle, as shown in Fig. 3, eight data bits are latched into the device and passed to the 8 bit D-to-A converter. Also latched on the falling edge of the clock signal, the $\overline{SYNC}$ and $\overline{BLANK}$ inputs add the necessary weighted currents to the analog outputs to produce the required output levels for use in video applications. Table 1 details how the $\overline{SYNC}$, $\overline{BLANK}$, $\overline{REFWHITE}$ and $\overline{OVERBRT}$ inputs modify the DAC output levels.

To obtain a high data throughput rate, the decoding logic of the MV95308 is fully pipelined. This introduces a one clock cycle delay between the latching of the input data and the resultant DAC output.

It also ensures synchronisation of the internal data and a minimal output glitch energy.

The DAC employed by the MV95308 eliminates the need for precision component ratios by using a segmented architecture in which equal weight bit currents are either routed to I_{OUT} or $\overline{I_{OUT}}$. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed.

The MV95308 eliminates the need for an external voltage reference by providing a nominally 1.0V reference on chip. An on-chip loop amplifier also provides stability of the full scale output current against power supply and temperature variations. The full scale output current is set by an external resistor R_{SET}. By adjustment of this value it is possible to implement RS-343A or RS-170 video levels as explained in the application notes.

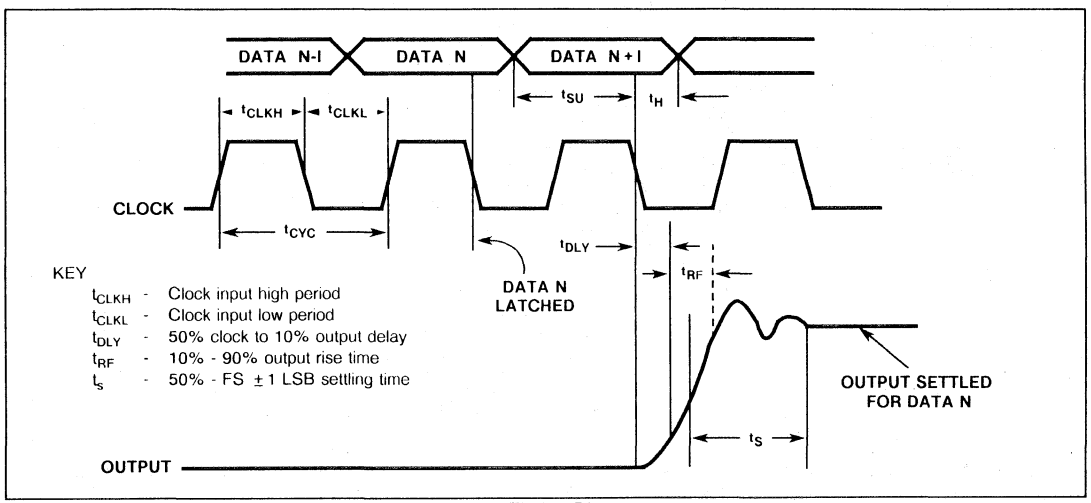


Fig.3 Timing Diagram

Description	$\overline{STRDAC}$	$\overline{SYNC}$	$\overline{BLANK}$	$\overline{REFWHITE}$	$\overline{OVERBRT}$	INPUT DATA	I_{OUT} (LSB)
REFWHITE + 10%	1	1	1	0	0	×	414
REFWHITE	1	1	1	0	1	×	387
FULL WHITE	1	1	1	1	1	$FF	387
OVERBRIGHT	1	1	1	1	0	DATA	DATA + 132 + 27
FULL BLACK	1	1	1	1	1	$00	132
BLANK	1	1	0	×	×	×	111
DATA-SYNC	1	0	1	1	1	DATA	DATA + 21
SYNC	1	0	0	×	×	×	0
STRDAC MODE	0	×	1	1	×	DATA	DATA

Table 1: Video Output Truth Table

PIN DESCRIPTIONS

Pin	Name	Description
2	CLK	**The clock input.** The falling edge of the clock latches the $\overline{\text{DATA}}$, $\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$, $\overline{\text{OVERBRT}}$ and $\overline{\text{REFWHITE}}$ inputs into the logic pipeline. The decoded data will be latched into the DAC output 1 clock cycle later. The clock frequency determines the update rate of the DAC output.
3-10	D_7-D_0	**The data inputs.** D_0 is the least significant bit (LSB). The coding is in straight binary only.
13,15	I_{OUT}, $\overline{I_{OUT}}$	**The current output and it's complement.** These are the high impedance current source outputs of the DAC capable of driving a 75Ω load up to a voltage of 1.5V.
14	GND	**Analog ground for the DAC.**
20	V_{DD}	**Analog power for the DAC.**
11	V_{REF}	**The output of the internal voltage reference generator.** This output is nominally 1V, and should be decoupled with a 10nF capacitor.
12	R_{SET}	**The full scale adjust control.** The R_{SET} resistor is connected from this pin to ground. An internal loop amplifier adjusts a reference current flowing through the R_{SET} resistor so that the voltage across the resistor is equal to the V_{REF} voltage. This reference current has a weighting equal to 16 LSB's.
1	$\overline{\text{BLANK}}$	**The composite blank control input.** A logical zero on this input removes the Black pedestal from the I_{OUT} output, whilst forcing the internal data to the DAC to $00. This input is latched on the clock falling edge and will override the $\overline{\text{REFWHITE}}$ and $\overline{\text{OVERBRT}}$ inputs. The Black pedestal is 7.5 IRE units (actually 21 LSB's). If left open circuit this input is internally tied high.
17	$\overline{\text{SYNC}}$	**The composite sync control input.** A logical zero on this input removes the Blank pedestal from the I_{OUT} output. The Blank pedestal is nominally 40 IRE units (actually 111 LSB's). The $\overline{\text{SYNC}}$ input does not override any of the other control lines. This input is latched on the clock falling edge. If left open circuit this input is internally tied high.
19	$\overline{\text{REFWHITE}}$	**The reference white level control input.** A logical zero on this input overrides the input data, forcing the data to $FF. The $\overline{\text{BLANK}}$ input will override this input. If left open circuit this input is internally tied high.
18	$\overline{\text{OVERBRT}}$	**The 10% overbright control input.** A logical zero on this input switches the Overbright pedestal into the I_{OUT} output. The Overbright pedestal is 10 IRE units (actually 27 LSB's). This input does not override any other input. The $\overline{\text{BLANK}}$ input overrides this input. If left open circuit this input is internally tied high.
16	$\overline{\text{STRDAC}}$	**The straight DAC control input.** A logical zero on this input causes the Black, Blank and Overbright pedestals to be disabled, removing them from both I_{OUT} and $\overline{I_{OUT}}$. This allows the DAC contribution to the output to be extended to a full 1 Volt. To obtain this extra DAC range, it is necessary to reduce the R_{SET} resistor value, see application notes. The $\overline{\text{BLANK}}$ and $\overline{\text{REFWHITE}}$ inputs may still be used to force the input data to $00 or $FF respectively. With the $\overline{\text{STRDAC}}$ pin held low the output current can be calculated from: Output current = Data × 1 LSB Where 1 LSB = $\frac{V_{REF}}{16 \times R_{SET}}$ Full scale = 255 LSB V_{REF} = 1.0V typ. The exact value of 1 LSB must be calculated from the full scale output. If left open circuit this input is internally tied high and the device will be configured for video graphics. In this mode the output current can be calculated from: Output current = (DATA + 21 + 111) × 1 LSB V_{REF} = 1.0V typ.

APPLICATIONS INFORMATION

RS-343A and RS-170 Video Generation

For generation of RS-343A compatible video levels (see Fig. 4) it is recommended that a singly terminated 75Ω load be used with an R_{SET} resistor value of approximately 1.82kΩ.

Similarly for the generation of RS-170 video levels a singly terminated 75Ω load should be used, but in association with an R_{SET} value of approximately 1.29kΩ to provide the increased voltage range.

Non-Video Applications

The MV95308 may be used in non video applications as explained in the pin description for $\overline{STRDAC}$ mode. The relationship between R_{SET} and the full scale output current has been explained previously and for a singly terminated 75Ω load an R_{SET} resistor value of approximately 1.19KΩ should be used.

PCB LAYOUT CONSIDERATIONS

The PCB layout should provide low noise on the MV95308 power and ground lines by shielding the digital inputs and providing adequate decoupling. The PCB should utilise both power and ground planes for best performance, connecting both planes to their respective regular PCB planes through a ferrite bead located as close as possible to the device. For best performance, a 100nF capacitor should be used to decouple the reference and supply pins. Decoupling should take place as close to the device as possible to reduce lead inductance. The digital inputs to the device should be isolated as much as possible from the analog outputs and other analog circuitry and should not overlay the analog ground and power planes.

To reduce noise pickup, long clock lines to the device should be avoided. For best performance the analog output should have a 75Ω load connected to analog ground.

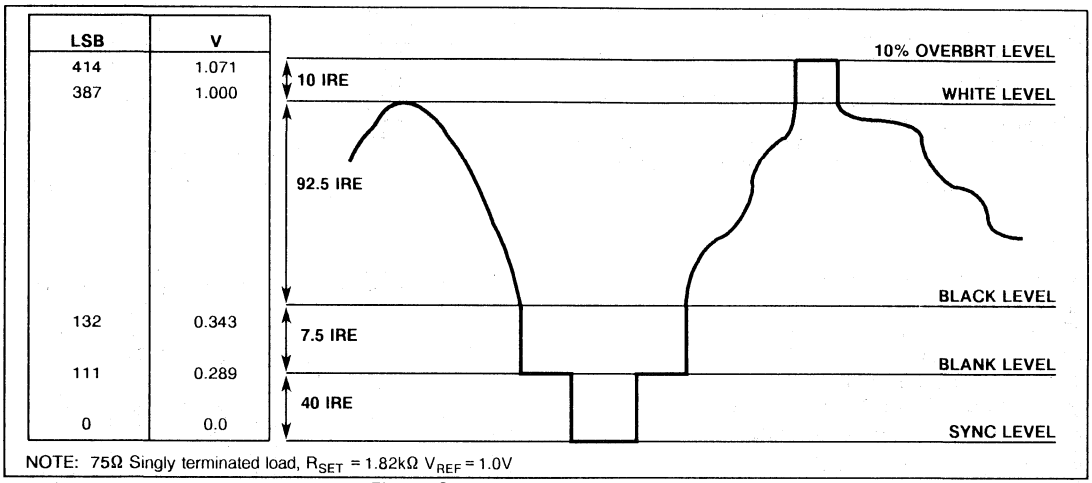


Fig.4. Composite video output waveform

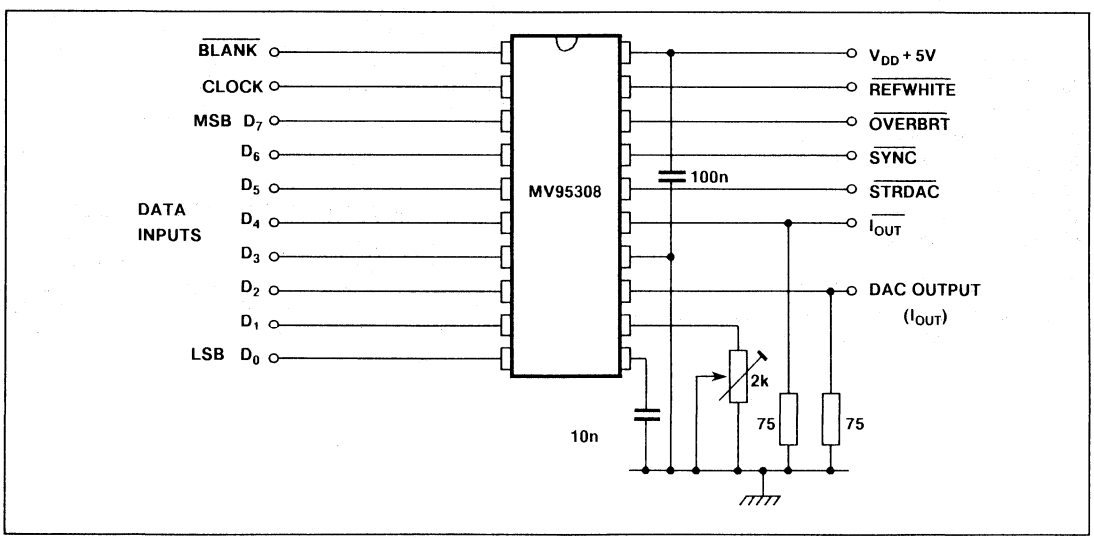


Fig.5 Applications/test board

PRELIMINARY INFORMATION
2421-1.0

MV95338

30MHz TRIPLE 8-BIT CMOS VIDEO DAC

The MV95338 is a CMOS triple 8-bit video DAC designed for use in high resolution television and computer colour graphics.

The device uses video control inputs ($\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$ and REF WHITE) to provide the MV95338 with the video pedestal levels required to generate RS-343A compatible video signals into a doubly-terminated 75Ω load, or alternatively to produce RS-170 video signals across a singly-terminated 75Ω load.

Data and control inputs are fully pipelined to maintain synchronisation between the DAC outputs.

The full scale output current is defined by an on-chip 1.2V reference and a single resistor.

Differential and integral linearity errors of the D-A converters are guaranteed to be a maximum of ± 1LSB over the full operating temperature range.

FEATURES

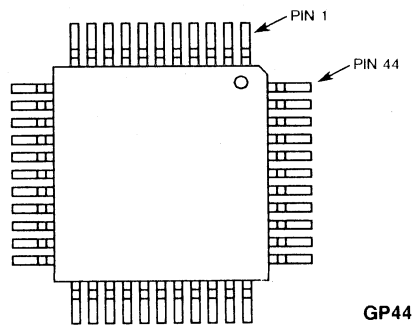
- 30MHz Pipeline Operation
- Triple 8-Bit D-A Converters
- ± 1LSB Differential Linearity Error
- ± 1LSB Integral Linearity Error
- Guaranteed Monotonic
- RS-343A/RS-170 Compatible Levels
- Drives Doubly-Terminated 75Ω Load
- Single 5V Power Supply
- Typical Power Dissipation 500mW
- On-Chip Voltage Reference

APPLICATIONS

- DBS Broadcast Video
- High Resolution TV
- Computer Colour Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction
- Picture-In-Picture

ORDERING INFORMATION

MV95338 C GP (Commercial - Plastic Leaded Chip Carrier, Gullwing formed leads)



Pin	Function	Pin	Function	Pin	Function
1	CLOCK	16	V_{AA}	31	R_5
2	R_0	17	V_{AA}	32	R_4
3	R_1	18	I_{SYNC}	33	B_7
4	R_2	19	IOG	34	B_6
5	R_3	20	IOR	35	B_5
6	G_0	21	IOB	36	B_4
7	G_1	22	$\overline{\text{AGND}}$	37	V_{AA}
8	G_2	23	$\overline{\text{SYNC}}$	38	V_{AA}
9	G_3	24	$\overline{\text{BLANK}}$	39	AGND
10	REF WHITE	25	G_7	40	AGND
11	COMP	26	G_6	41	B_0
12	$V_{REF\ OUT}$	27	G_5	42	B_1
13	FS ADJUST	28	G_4	43	B_2
14	AGND	29	R_7	44	B_3
15	AGND	30	R_6		

Fig.1 Pin connections - top view.

ABSOLUTE MAXIMUM RATINGS (Referenced to AGND)

DC supply voltage, V_{AA}	-0.3V to +7V
Digital input voltage	-0.3V to V_{AA} +0.3V
Analog output short circuit duration	Indefinite
Ambient operating temperature	0°C to +70°C
Storage temperature range	-55°C to +125°C

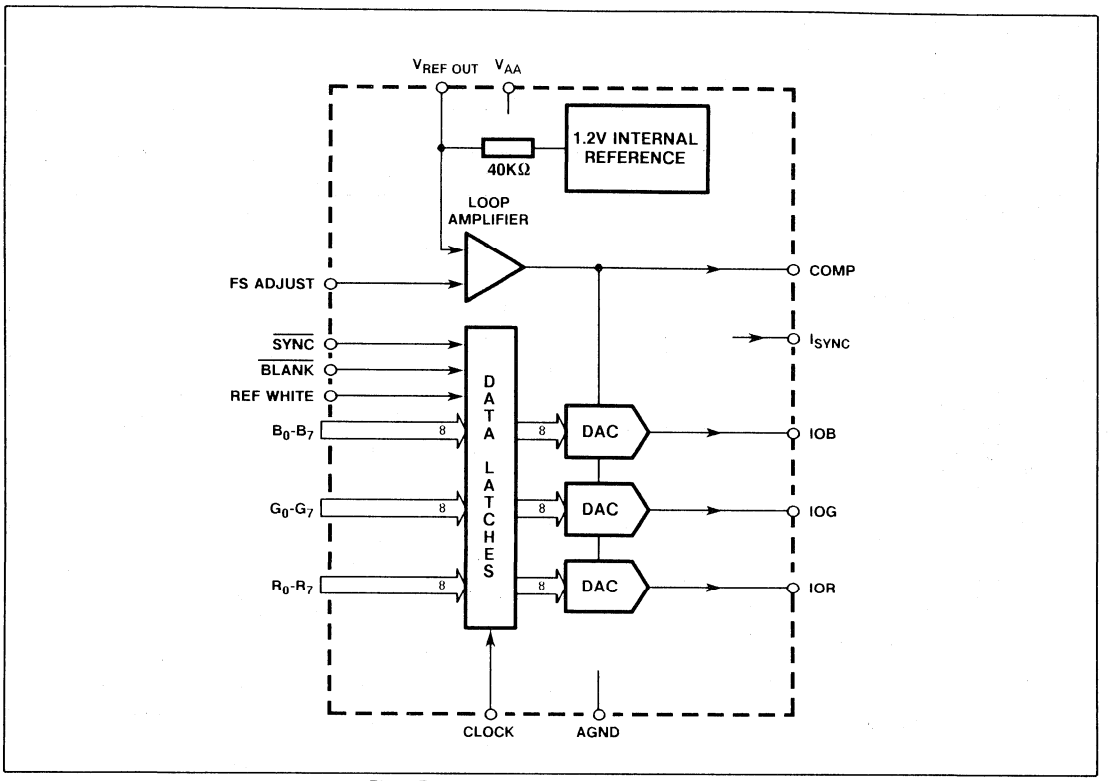


Fig.2 Functional block diagram of MV95338

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_{AA}	4.75	5.00	5.25	V	
Ambient operating temperature	T_{amb}	0		+70	°C	
Output load	R_L		37.5		Ω	For RS-343A compatible output levels
FS ADJUST resistor	R_{SET}		542		Ω	For RS-343A compatible output levels

THERMAL CHARACTERISTICS

	GP
Thermal resistance, chip-to-case θ_{jc}	17 °C/W
Thermal resistance, chip-to-ambient θ_{jA}	50 °C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
As specified in Recommended Operating Conditions

DC CHARACTERISTICS

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Resolution (each DAC)		8			Bits	
Accuracy (each DAC)						
Integral linearity error	INL		±0.3	±1	LSB	
Differential linearity error	DNL		±0.3	±1	LSB	
Grey scale error			±1	±5	% grey scale	
Monotonicity			Guaranteed			
Digital Inputs						
Input high voltage	V_{IH}	3.0		V_{AA} + 0.3	V	Binary coding
Input low voltage	V_{IL}	AGND-0.3		1.2	V	
Input high current	I_{IH}			1	μA	
Input low current	I_{IL}			-1	μA	
Analog Outputs						
Grey scale current range		15		20	mA	
			255		LSB	
Output currents						
White level relative to blank level		17.69	19.06	20.40	mA	RS-343A tolerances assumed
			276		LSB	
White level relative to black level		16.74	17.62	18.50	mA	
			255		LSB	
Black level relative to blank level		0.95	1.44	1.90	mA	
			21		LSB	
Blank level on IOR, IOB		0	5	50	μA	
			0		LSB	
Blank level on IOG		6.29	7.62	8.96	mA	
			111		LSB	
Sync level on IOG		0	5	50	μA	
			0		LSB	
LSB size			69.1		μA	
DAC to DAC matching			2		%	
Output compliance	V_{OC}	-0.5		+1.4	V	
Reference voltage	V_{REFOUT}	1.14	1.20	1.26	V	
Voltage reference temperature coeff.			40		ppm/°C	

AC CHARACTERISTICS

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Max clock rate	f_{max}	30			MHz	
Data and control setup time	t_{SU}	8			ns	
Data and control hold time	t_H	2			ns	
Clock cycle time	t_{CYC}	33.3			ns	
Clock pulse width high time	t_{CLKH}	10			ns	
Clock pulse width low time	t_{CLKL}	10			ns	
Analog output delay	t_{DLY}		10		ns	
Analog output rise/fall time	t_{VRF}		6	9	ns	
Analog output settling time	t_S		15		ns	
Glitch impulse			100		pV-sec	
Analog output skew			0	3	ns	
Pipeline delay		1	1	1	Clock	
V_{AA} supply current	I_{AA}		100	140	mA	At f_{max}, V_{AA} = 5V

CIRCUIT DESCRIPTION

As shown in Fig. 2, the MV95338 contains three 8-bit D-A converters, input latches, internal voltage reference and a loop amplifier.

On the rising edge of each clock cycle (see Fig. 4), 24 bits of colour information (R_0-R_7, G_0-G_7, and B_0-B_7) are latched into the device and presented to the three 8-bit D-A converters. The REF WHITE input, also latched on the rising edge of each clock cycle, and will force the inputs of each D-A converter to $FF.

$\overline{SYNC}$ and $\overline{BLANK}$ are latched on the rising edge of the clock to maintain synchronisation with the colour data. These inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as shown in Fig. 3. Table 1 details how the $\overline{SYNC}$, $\overline{BLANK}$ and REF WHITE inputs modify the output levels.

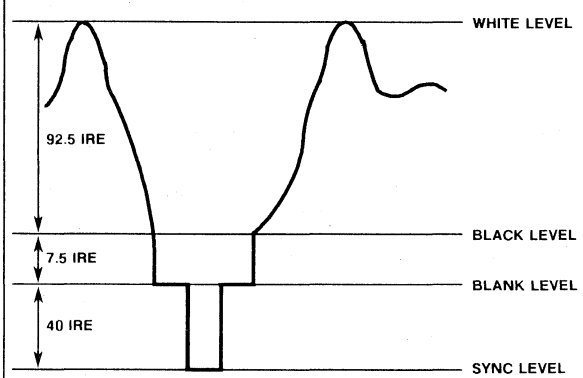
The I_{SYNC} current output is typically connected directly to the IOG output and is used to encode sync information onto the IOG output. If I_{SYNC} is not connected to the IOG output, sync information will not be encoded on the green channel, and the IOR, IOG and IOB outputs will have the same full scale output current.

Full Scale output current is set by an external resistor (R_{SET}) between the FS ADJUST pin and AGND. R_{SET} has a typical value of 542Ω for generation of RS-343A video into a 37.5Ω load.

The D-A converters on the MV95338 use a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifer stabilizes the full scale output current against temperature and power supply variations.

The analog outputs of the MV95338 are capable of directly driving a 37.5Ω load, such as a doubly terminated 75Ω co-axial cable.

Red/Blue		Green	
mA	V	mA	V
19.06	0.714	26.68	1.000
1.44	0.054	9.06	0.340
0.00	0.000	7.62	0.286
		0.000	0.000



NOTE : 75Ω doubly terminated load, R_{SET} = 542Ω, V_{REF} = 1.2V, I_{SYNC} connected to IOG, RS-343A levels assumed

Fig.3 Composite video output waveform

Description	IOG (mA)	IOR/IOB (mA)	REF WHITE	$\overline{SYNC}$	$\overline{BLANK}$	DAC I/P Data
White Level	26.68	19.06	1	1	1	$XX
White Level	26.68	19.06	0	1	1	$FF
Data	Data + 9.06	Data + 1.44	0	1	1	Data
Data-Sync	Data + 1.44	Data + 1.44	0	0	1	Data
Black Level	9.06	1.44	0	1	1	$00
Black-Sync	1.44	1.44	0	0	1	$00
Blank Level	7.62	0	X	1	0	$XX
Sync Level	0	0	X	0	0	$XX

NOTE : Typical with full scale IOG = 26.68mA, R_{SET} = 542Ω, V_{REF} = 1.2V, I_{SYNC} connected to IOG

Table 1 Video output truth table

PIN DESCRIPTIONS

Pin name	Description
$\overline{\text{BLANK}}$	Composite blank control input. A logic '0' forces the IOR, IOG and IOB outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logic zero, the R_0-R_7, G_0-G_7, B_0-B_7, and REF WHITE inputs are ignored.
$\overline{\text{SYNC}}$	Composite sync control input. A logic '0' on this input switches off a 40 IRE current source on the I_{SYNC} output. $\overline{\text{SYNC}}$ does not override any other control or data input, as shown in Table 1; therefore it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
REF WHITE	Reference white control input. A logic '1' on this input forces the IOR, IOG, and IOB outputs to the white level, regardless of the R_0-R_7, G_0-G_7 and B_0-B_7 inputs. It is latched on the rising edge of CLOCK. See Table 1.
R_0-R_7 G_0-G_7 B_0-B_7	Red, Green, and Blue data inputs. R_0, G_0, and B_0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary. Unused inputs should be connected to either the regular PCB power or ground plane.
CLOCK	Clock input. The rising edge of CLOCK latches the R_0-R_7, G_0-G_7, B_0-B_7 $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, and REF WHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated CMOS buffer.
IOR, IOG, IOB	Red, Green and Blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω co-axial cable. All outputs, whether used or not, should have the same output load.
I_{SYNC}	Sync current output. Typically this current output is directly wired to the IOG output, and enables sync information to be encoded onto the green channel. A logic '0' on the $\overline{\text{SYNC}}$ input results in no current being output onto this pin, while a logic '1' results in the following current being output: $I_{SYNC}\ (mA) = 3468 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 111\ LSBs$ If sync information is not required on the green channel, this output may be connected to V_{AA} and the $\overline{\text{SYNC}}$ input tied high, causing the I_{SYNC} current source to be turned off, reducing the power consumption.
FS ADJUST	Full scale adjust control. A resistor (R_{SET}) connected between this pin and AGND controls the magnitude of the full video signal (Fig. 3). The current flowing in the R_{SET} resistor is equal to 32 LSBs. Note that the IRE relationships in Fig. 3 are maintained, regardless of the full scale output current. The relationship between R_{SET} and the full scale current on IOG (assuming I_{SYNC} is connected to IOG) is: $IOG\ (mA) = 12082 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 387\ LSBs$ The full scale output current on IOR and IOB for a given R_{SET} is defined as: $IOR, IOB\ (mA) = 8624 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 276\ LSBs$
COMP	Compensation pin. This pin provides compensation for the internal loop amplifier. A 0.01μF ceramic capacitor must be connected between this pin and the nearest V_{AA} pin. Connecting the capacitor to V_{AA} rather than to AGND provides the highest possible power supply noise rejection.
$V_{REF\ OUT}$	Voltage reference output. The output from an internal reference circuit, providing 1.2V (typical) reference. A 0.1μF ceramic capacitor must be used to decouple this output to V_{AA}.
AGND	Analog ground. All AGND pins must be connected.
V_{AA}	Analog power. All V_{AA} pins must be connected.

APPLICATION NOTES

RS-343A and RS-170 Video Generation

For the generation of RS-343A compatible video levels it is recommended that a doubly terminated 75Ω load be used with an R_{SET} resistor value of a approximately 542Ω.

Similarly for the generation of RS-170 compatible video, it is recommended that a singly terminated 75Ω load be used with an R_{SET} value of about 774Ω. If the MV95338 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75Ω and singly terminated 75Ω loads

If driving a large capacitive load (load RC > $1/20\Pi f_C$) it is recommended that an output buffer with an unloaded gain > 2 be used to drive a doubly terminated 75Ω load.

COMP Resistor

To optimise the settling time of the MV95338, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

Non- Video Applications

The MV95338 may be used in non-video applications by disabling the video specific control inputs. REF WHITE should be logic '0' while $\overline{BLANK}$ and $\overline{SYNC}$ should be a logic '1'. I_{SYNC} should be connected to V_{AA} or AGND. All three outputs will have the same full scale output current.

The relationship between R_{SET} and full scale output current (I_{out}) in this configuration is as follows:

$$I_{out}\,(mA) = 7968 \times \frac{V_{REF}\,(V)}{R_{SET}\,(\Omega)} \equiv 255\ LSBs$$

$$\text{Note that 1 LSB} \equiv \frac{V_{REF}\,(V)}{32 \times R_{SET}\,(\Omega)}$$

With the data inputs at $00, there is a DC offset current (I_{min}) defined as follows:

$$I_{min}\,(mA) = 656 \times \frac{V_{REF}\,(V)}{R_{SET}\,(\Omega)} \equiv 21\ LSBs$$

Therefore, the total full scale output current will be $I_{out} + I_{min}$. The REF WHITE input may optionally be used as a 'force to full scale' control.

TIMING WAVEFORMS

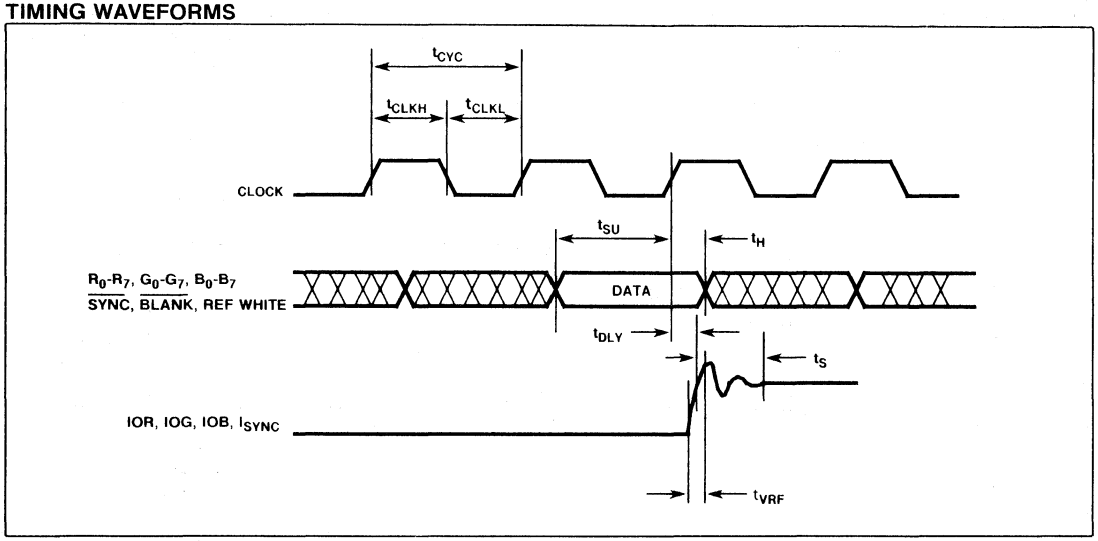


Fig.4 Input/output timing

NOTES

1. Output delay, t_{DLY}, measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.
2. Settling time, t_S, measured from the 50% point of full scale transition to the output remaining within ±1 LSB.
3. Output rise/fall time , t_{VRF}, measured between the 10% and 90% points of full scale transition.

PCB LAYOUT CONSIDERATIONS

To obtain the optimum performance from the MV95338 great care must be taken in the PCB layout to ensure low noise power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling.

Power and Ground Planes

The MV95338 and its associated circuitry should have its own separate power/ground planes, which should be at a single point through ferrite bead. It is important that the regular PCB power and ground planes do not over lay portions of the analog power or ground planes to minimise plane-to-plane noise coupling.

Digital Signal Interconnect

The digital signal lines to the MV95338 should be isolated as much as possible from the analog circuitry. Due to the high clock rates used, the clock lines to the MV95338 should be as short as possible to minimise noise pickup.

Any pull-up resistors used on the digital inputs should be connected to the regular PCB power plane, not to the analog power plane.

Supply Decoupling

Noise on the analog power plane will be further reduced by the use of multiple decoupling capacitors (See Fig. 5.)

Optimum performance is obtained with 0.1µF chip ceramic capacitors placed as close as possible to the VAA pins, with the shortest leads possible to reduce lead inductance.

It should be noted that while the loop amplifier circuitry of the MV95338 will reject power supply noise, this rejection decreases with frequency. Any high frequency noise on the regular supply (such as produced by a switch mode power supplies) must be adequately suppressed, else the designer should consider using a three terminal regulator to supply the analog power plane.

Analog Signal Interconnect

For optimum performance the analog output connectors and source termination resistors should be as close as possible to the MV95338 to minimise noise pickup and reflections due to impedance mismatch. The video output signals should overlay the ground plane and not the analog power plane, to maximise the high frequency power supply rejection.

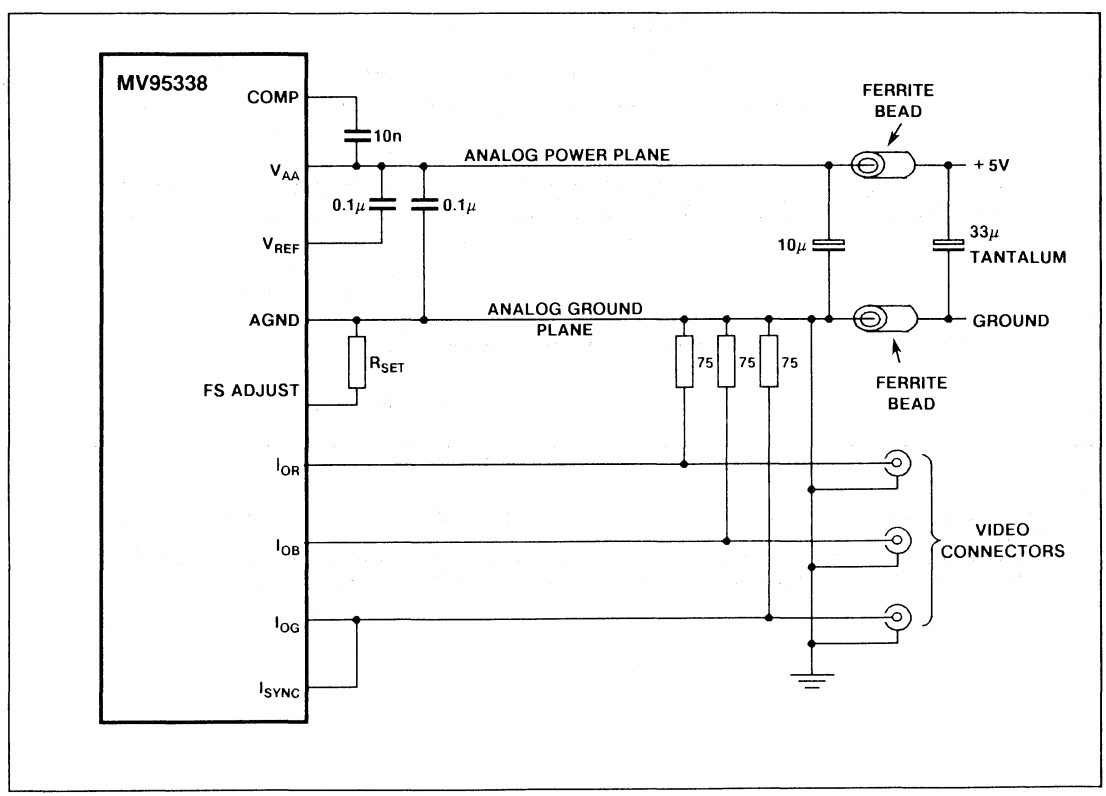


Fig.5 MV95338 Typical Connections

SP973T8

30MHz 8-BIT FLASH ADC (TTL/CMOS OUTPUTS)

The SP973T8 is a wideband, full flash analog- to-digital converter that requires no preceding sample and hold. The device contains a full 8-bit D-type latch which ensures that the 8 TTL/CMOS outputs are accurately registered and have a good data valid time at high clock speeds.

Operating from a single +5 volt supply the device is capable of conversion rates well in excess of 30 MHz and its wideband input allows signals with frequencies up to the Nyquist limit to be digitised with high accuracy. An internal bandgap voltage regulator gives low DC drift over a wide operating temperature range (-40°C to +85°C in DG package).

The SP973T8 is designed for applications where power consumption and package size is at a premium.

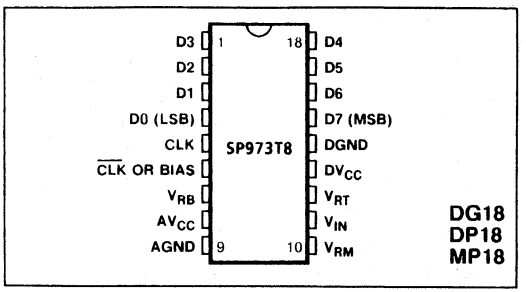


Fig.1 Pin connections - top view

FEATURES

- Flash Converter, No Sample and Hold Required
- Wideband Analog Input 70MHz, 3dB (Typ.)
- Low Power Consumption (600 mW Typ.)
- Latched TTL/CMOS Compatible Outputs
- Wide Operating Temperature Range
- No Missing Codes - Guaranteed
- Designed for Wideband Operation
- Single 5V Supply
- Production Tested at 30MHz

ORDERING INFORMATION

SP973T8 B DG (Industrial - Ceramic DIL package)
SP973T8 C DP (Commercial - Plastic DIL package)
SP973T8 C MP (Commercial - Miniature Plastic DIL package)

APPLICATIONS

- Studio Quality Video
- DBS Broadcast Video
- High Resolution TV
- Nucleonics
- Radar
- Computing

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	7V
Output Current	10mA
Input Voltage, V_{IN}	V_{CC}
Operating Temperature	-40°C to +85°C (BDG)
	0°C to +70°C (CDP/CMP)
Storage Temperature	-65°C to +150°C

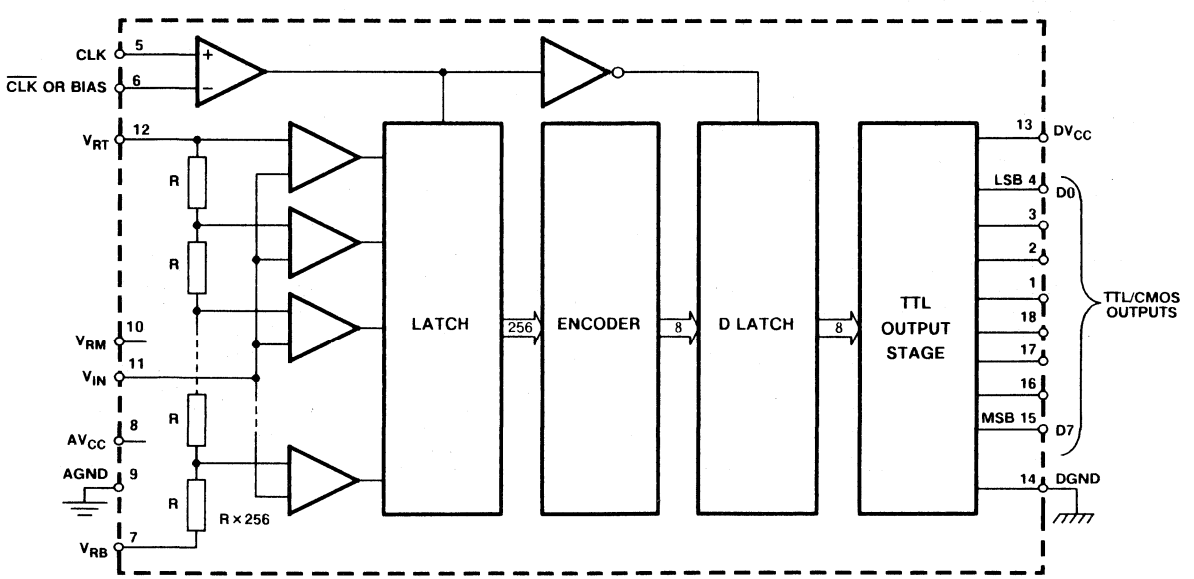


Fig.2 Internal block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25°C, V_{CC} = +5V ± 0.25V

Full temperature range = -40°C to +85°C (SP973T8 B DG), 0°C to +70°C (SP973T8 C DP and SP973T8 C MP)

DC CHARACTERISTICS

Characteristic	Symbol	Temp.	Test level	Value			Units	Conditions
				Min.	Typ.	Max.		
Power Supply								
Supply current	I_{CC}	Full	4	100		140	mA	
		25	1	110	120	130	mA	
Power dissipation	P_D	Full	4	475		735	mW	
		25	1	520	600	680	mW	
Analog Input								
Input range	V_{IN}	Full	4	1.8		V_{CC}-0.7	V	
Input bias current	I_{IN}	25	1	150	390	1100	µA	$V_{IN} = V_{RT}$
3dB bandwidth	f_{3dB}	25	4		70		MHz	
Input capacitance	C_{IN}	25	4		30		pF	
Reference Ladder								
Ladder resistance	R_D	25	1	325	400	475	Ω	
Ladder voltage (top)	V_{RT}	Full	4		4.3	V_{CC}-0.7	V	
Ladder voltage (bottom)	V_{RB}	Full	4	1.8	2.3		V	
Ladder offset (top)	V_{RT0}	25	5		-4		mV	
Ladder offset (bottom)	V_{RB0}	25	5		+3		mV	
Ladder temp. coeff.	R_{TC}	Full	5		1.5		Ω/°C	
Clock Input								
Logic '1' voltage	V_{IH}	Full	4	2.75	4.3	V_{CC}	V	A swing of 1V centred on the voltage applied to the $\overline{CLK}$ pin
Logic '1' current	I_{IH}	25	1			25	µA	
Logic '0' voltage	V_{IL}	Full	4	1.75	3.3	V_{CC}-1.0	V	
Logic '0' current	I_{IL}	25	1			2	µA	
Digital outputs								
Logic '1' voltage	V_{OH}	Full	4	3.3			V	Into Standard LS TTL Load
		25	1	3.5	3.8		V	
Logic '0' voltage	V_{OL}	Full	4			0.4	V	
		25	1		0.1	0.4	V	
Static performance								
Differential non-linearity	DNL	Full	4			±1	LSB	
		25	4			±0.5	LSB	
Integral non-linearity	INL	Full	4			±1	LSB	
		25	4			±1	LSB	

AC CHARACTERISTICS (Refer to Fig 7.)

Characteristic	Symbol	Temp.	Test level	Value			Units	Conditions
				Min.	Typ.	Max.		
Clock min. high	t_{PW1}	25	4	10			ns	
Clock min. low	t_{PW0}	25	4	10			ns	
Max. conversion rate		Full	4	30	50		MHz	A_{IN} = 15MHz at FS
Aperture delay	t_{AD}	25	5		3		ns	
Output data delay	t_D	25	4		7		ns	
Output rise time	t_R	25	4		6		ns	
Output fall time	t_F	25	4		8		ns	
Dynamic Performance								With F_{CLK} = 30 MHz
Differential non-linearity	DNL	25	1	-0.85	±0.5	+1	LSB	$A_{IN\ MAX}$ = 10MHz at FS
Integral non-linearity	INL	25	1		±1	±2	LSB	$A_{IN\ MAX}$ = 10MHz at FS
S/N ratio	SNR	25	1	40.9	44.5		dBc	$A_{IN\ MAX}$ = 1MHz at FS
			4		44.1		dBc	$A_{IN\ MAX}$ = 5MHz at FS
			4		43.3		dBc	$A_{IN\ MAX}$ = 10MHz at FS
Effective No. of bits	ENOB	25	1	6.5	7.1		bits	$A_{IN\ MAX}$ = 1MHz at FS
			4		7.0		bits	$A_{IN\ MAX}$ = 5MHz at FS
			4		6.9		bits	$A_{IN\ MAX}$ = 10MHz at FS
Bit Error Rate	BER	25	4		$1\ in\ 10^9$			

ELECTRICAL CHARACTERISTICS DEFINITIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency, as determined by Fast Fourier Transform analysis is 3dB down on the DC level.

Aperture Delay
The delay between the falling edge of the CLOCK signal and the instant at which the analog input is sampled.

Bit Error Rate (BER)
The number of spurious code errors produced for any given input sinewave frequency. In this case it is the number of codes occuring outside the histogram cusp for a ¾ F.S. sinewave.

Differential Non-Linearity (DNL)
The deviation of any code width from an ideal 1LSB step.

Effective Number of Bits (ENOB)
This is a measure of the dynamic performance and is calculated from the following expression.

$$ENOB = \frac{SNR\text{-}1.76}{6.02}$$

SNR is the signal-to-noise ratio, in decibels, at the test frequency.

Integral Non-Linearity (INL)
The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

Output Data Delay
The delay between the 50% point of the falling edge of the clock signal and the 50% point of any data output change.

Reference Ladder Offset
The voltage error at the ends of the resistor chain caused by the lead frame and bond wire.

Signal-to-Noise Ratio (SNR)
The ratio of the RMS signal amplitude to the RMS value of 'noise' which is defined as the sum of all other spectral components including harmonics but excluding DC with a full scale analog input signal.

Test Levels
Level 1 - 100% production tested
Level 2 - 100% production tested at 25°C and sample tested at specified temperatures
Level 3 - Sample tested only
Level 4 - Parameter is guaranteed by design and characteristics testing
Level 5 - Parameter is a typical value only

PIN DESCRIPTIONS

Pin No.	Function	Description
1, 2, 3, 4	D3, D2, D1, D0	Output data bits 3, 2, 1, 0
5	$\overline{CLK}$	Clock input pin
6	CLK	Clock threshold level pin
7	V_{RB}	Bottom of reference resistor chain
8	AV_{CC}	5 Volt power to all circuitry except the TTL output
9	AGND	5 Volt power to all circuitry except the TTL output
10	V_{RM}	Middle of reference resistor chain
11	V_{IN}	Analog input voltage pin
12	V_{RT}	Top of reference resistor chain
13	DV_{CC}	5 Volt power supply to the TTL output stage
14	DGND	5 Volt power supply to the TTL output stage
15	D7	Most significant bit (output data bit 7)
16, 17, 18	D6, D5, D4	Output data bits 6, 5, 4

RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	+5.0V
Reference V_{RT}	+4.3V
Reference V_{RB}	+2.3V
AV_{CC} to DV_{CC}	0mV
AGND to DGND	0mv
Analog Input V_{IN}	2 Vp-p max

THERMAL CHARACTERISTICS

	DG	DP	MP
Thermal resistance, chip-to-case θ_{jc}	21	20	30 °C/W
Thermal resistance, chip-to-ambient θ_{jA}	92	75	98 °C/W

APPLICATION NOTES

Analog Input Pin (Fig 3.)

The analog input of the SP973T8 is connected to 256 comparators which have a combined capacitance of about 30pF. The sample/latch operation of the comparators causes the input capacitance to vary slightly as the comparator input transistors turn on/off. For this reason the input driver circuit should provide a low impedance signal to keep the harmonic distortion levels of the driver to a minimum.

The maximum amplitude of the analog input is defined by the setting of the two reference voltages V_{RT} and V_{RB}. Optimum performance will be obtained with the input signal biased midway between V_{RT} and V_{RB} with a peak to peak amplitude of V_{RT}-V_{RB}. The SP973T8 has excellent overload tracking of input signals with amplitudes greater than V_{RT}-V_{RB}, and will not be damaged if the absolute maximum ratings are adhered to.

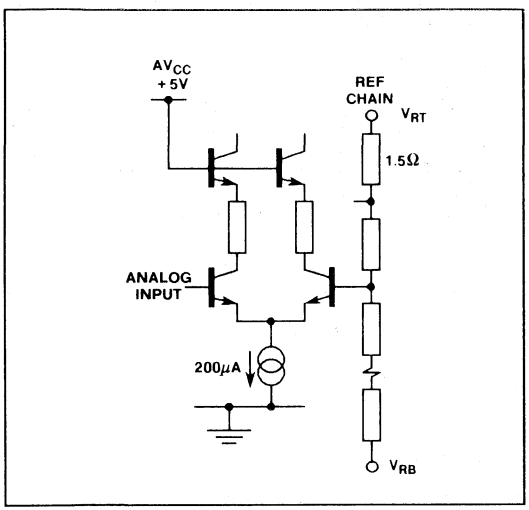


Fig.3 One of 255 analog inputs connected to pin 11

Voltage Reference Pins (Fig 4.)

The SP973T8 converts analog signals in the range $V_{RB} < V_{IN} < V_{RT}$ into digital format, where V_{RB} produces code 0 and V_{RT} produces code 255. Between the pins V_{RT} and V_{RB} are a series of 256 resistors forming a reference chain with a total resistance of 425Ω (typically). The centre point of the reference chain is also connected to an external pin named V_{RM} by which it is possible to provide precision trimming of the integral linearity of the device.

The maximum value of V_{RT} is V_{CC}-0.7 volts since values above this figure will start to saturate the comparator, resulting in noticeable distortion. Optimum performance from a +5 Volt power supply is obtained with $V_{RT} < +4.3V$ and V_{RB} a further 2 volts below V_{RT}. In addition the V_{RT}, V_{RB} and V_{RM} pins should be decoupled to ground close to the device pins using good quality 10nf capacitors. A simple method for providing the reference voltages is shown in Fig. 4, and further information may be found in applications note AN72 (page 4-74). With a reference ladder voltage of less than 2V the reduced LSB size causes a larger differential linearity error. Operation of the device below 1.5V may therefore cause missing codes.

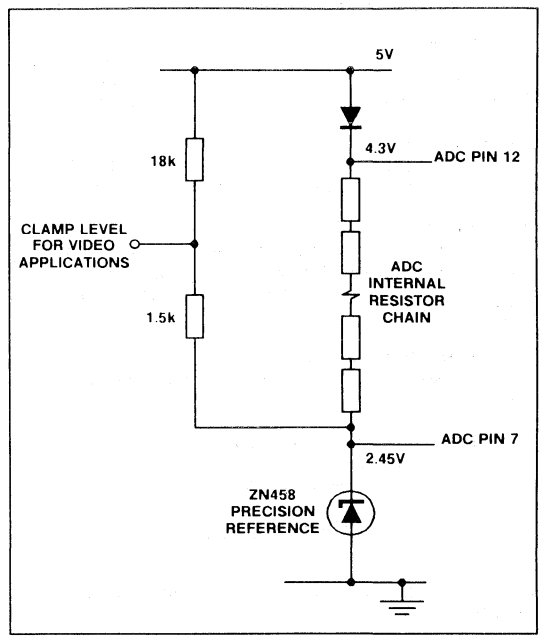


Fig.4 Simple reference voltage generation

TTL/CMOS Outputs (Fig. 5)

The data output levels of the SP973T8 are TTL/CMOS compatible and switch from 0V to +4V. The output circuit is capable of operation at clock frequencies in excess of 60MHz when driving into a standard LSTTL load.

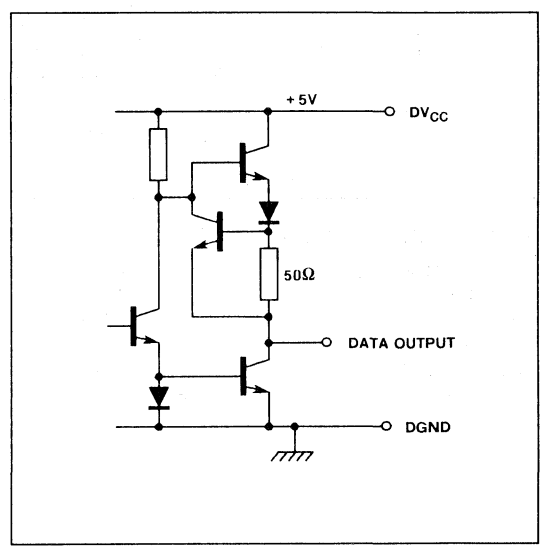


Fig.5 TTL output stage

Clock Input (Fig. 6)

The SP973T8 will operate at clock frequencies up to and above 30MHz. The clock input has been designed to accept a 1Vpp signal, in either differential or single-ended mode, between the $V_{IH(MAX)}$ and $V_{IL(MIN)}$ levels indicated in the electrical specification. At $V_{IH(MAX)}$ or $V_{IL(MIN)}$ the $\overline{CLK}$ input will sink 800µA or source 3.2mA of current, respectively. (See Fig. 6)

When used in single-ended operation, $\overline{CLK}$ may be decoupled to ground so that this input will then self-bias at approximately 1.2V below the supply V_{CC}. It may then be used to bias the $\overline{CLK}$ input, through a termination resistor, for AC-coupled applications as shown in Fig. 8.

Alternatively a TTL level clock may be used by inserting an appropriate value resistor in series with the coupling capacitor.

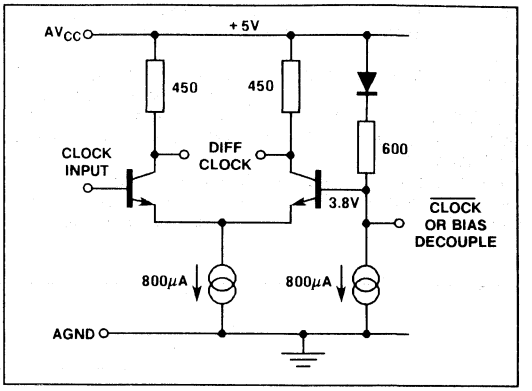


Fig.6 Clock input stage

TIMING (Fig. 7)

The analog input is sampled by the SP973T8 approximately 3ns (t_{AD}) after the falling edge of the clock. Due to the pipelined operation of the device, a further one clock cycle is required to produce the output data. As shown in Fig. 7, the output has a good data valid time, enabling the data to be latched at both the rising and fallingedges of the clock.

However, for clock frequencies above 25MHz the clock-to-output delay time may lead to an inadequate data set up time relative to the rising clock edge and it is therefore recommended that the output data is latched on the falling clock edge.

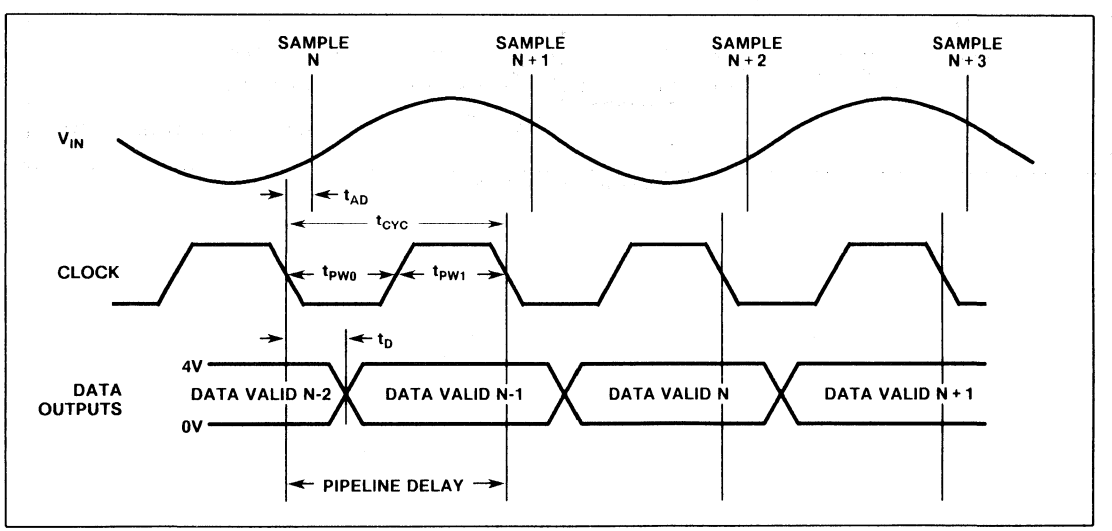


Fig.7 Timing diagram

Circuit Board Construction (Fig. 8)

Excellent performance can be obtained from this ADC using only one solid ground plain for both analog and digital signals.

With all flash ADCs it is important to restrict digital crosstalk into the input, not only within the wanted signal bandwidth but also at frequencies between Nyquist and clock, as such signals will be aliased down into the wanted signal bandwidth.

We can give the designer two useful suggestions to reduce the above. First, due to the on-chip clock regeneration circuit, a low level clock can be fed to the ADC 1V p-p is recommended. The second suggestion is the addition of a small bead inductor in series with and close to the device analog input.

Supply line decoupling is very important when dealing with a mix of analog and digital signals as they can provide a source of digital feedback from the digital output currents. It is wise, therefore, to decouple the SP973T8 close to the device supply pins with good quality, high frequency, low inductance capacitors.

Due to the high clock rates involved, long clock lines to the device should be avoided to reduce the noise pick up.

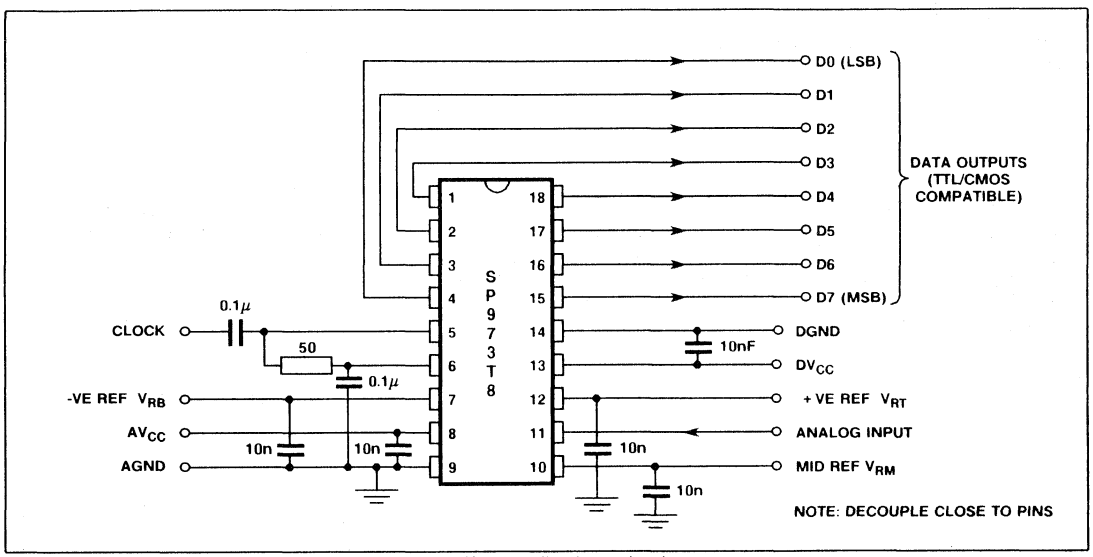


Fig.8 Test/applications circuit

VP101

30/50MHz TRIPLE 8-BIT CMOS VIDEO DAC

The VP101 is a CMOS triple 8-bit video DAC designed for use in high performance, high resolution colour graphics applications.

The device uses video control inputs ($\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$ and REF WHITE) to provide the VP101 with the video pedestal levels required to generate RS-343A compatible video signals into a doubly-terminated 75Ω load, or alternatively to produce RS-170 video signals across a singly-terminated 75Ω load.

Data and control inputs are fully pipelined to maintain synchronisation between the DAC outputs.

The full scale output current is defined by a 1.2V reference and a single resistor. The reference voltage is included on-chip in the VP101, but may be supplied externally if required (see Fig. 2).

Differential and integral linearity errors of the D-A converters are guaranteed to be a maximum of ± 1LSB over the full operating temperature range.

FEATURES

- 30/50MHz Pipeline Operation
- Triple 8-Bit D-A Converters
- ± 1LSB Differential Linearity Error
- ± 1LSB Integral Linearity Error
- Guaranteed Monotonic
- RS-343A/RS-170 Compatible Levels
- Drives Doubly-Terminated 75Ω Load
- Single 5V Power Supply
- Typical Power Dissipation 500mW
- Direct Replacement for Bt101
- On-Chip Reference Available

APPLICATIONS

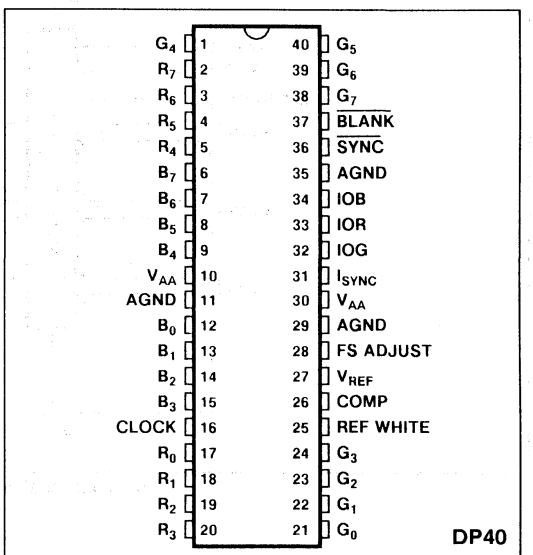
- High Resolution Colour Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction
- Instrumentation

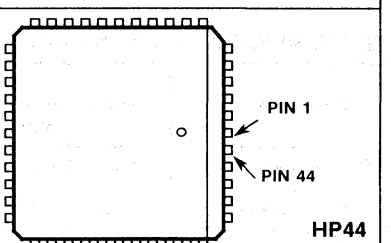
ORDERING INFORMATION

VP101-3 BA DP (Commercial - Plastic DIL package)
VP101-3 BA HP (Commercial - Plastic J-lead package)
VP101-5 BA DP (Commercial - Plastic DIL package)
VP101-5 BA HP (Commercial - Plastic J-lead package)

ABSOLUTE MAXIMUM RATINGS (Referenced to AGND)

DC supply voltage, V_{AA}	-0.3V to +7V
Digital input voltage	-0.3V to V_{AA} +0.3V
Analog output short circuit duration	Indefinite
Ambient operating temperature	0°C to +70°C
Storage temperature range	-55°C to +125°C





Pin	Function	Pin	Function	Pin	Function
1	AGND	16	REF WHITE	31	G_7
2	AGND	17	COMP	32	G_6
3	B_0	18	V_{REF}	33	G_5
4	B_1	19	FS ADJUST	34	G_4
5	B_2	20	AGND	35	R_7
6	B_3	21	AGND	36	R_6
7	CLOCK	22	V_{AA}	37	R_5
8	R_0	23	V_{AA}	38	R_4
9	R_1	24	I_{SYNC}	39	B_7
10	R_2	25	IOG	40	B_6
11	R_3	26	IOR	41	B_5
12	G_0	27	IOB	42	B_4
13	G_1	28	$\underline{\text{AGND}}$	43	V_{AA}
14	G_2	29	$\underline{\text{SYNC}}$	44	V_{AA}
15	G_3	30	$\overline{\text{BLANK}}$		

Fig.1 Pin connections (not to scale) - top view.

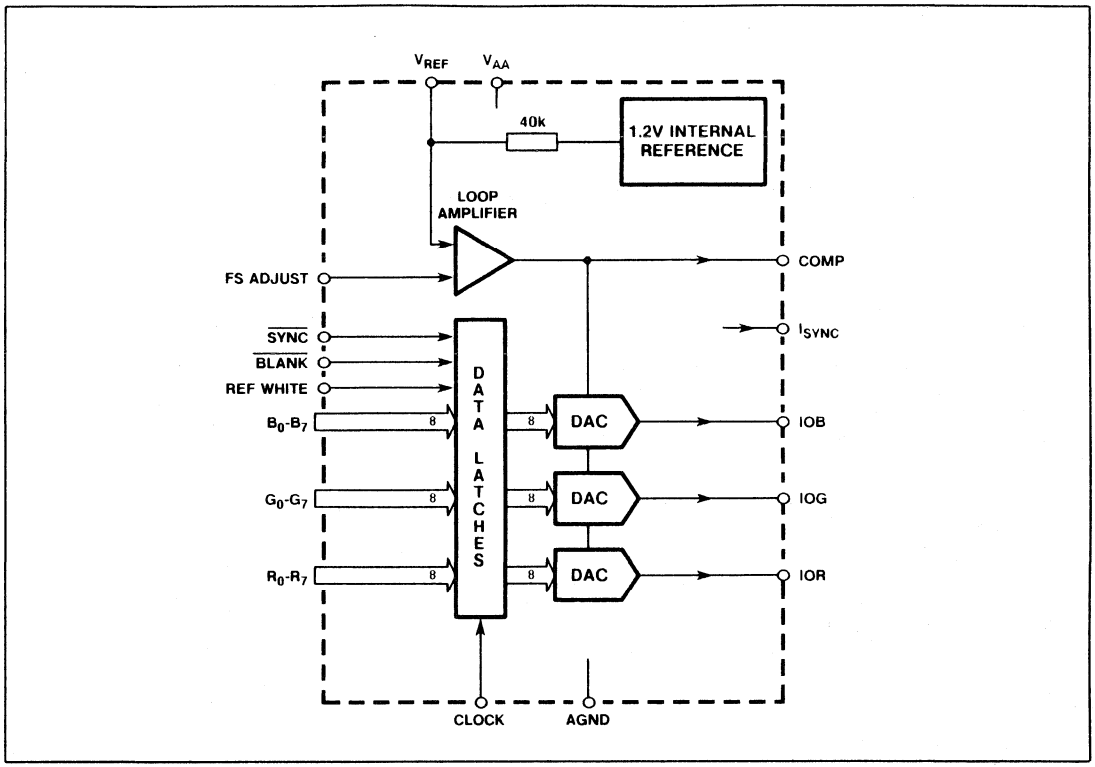


Fig.2 Functional block diagram of VP101

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_{AA}	4.75	5.00	5.25	V	
Ambient operating temperature	T_{amb}	0		+70	°C	
Output load	R_L		37.5		Ω	For RS-343A compatible output levels
Reference voltage (internal or external)	V_{REF}	1.14	1.20	1.26	V	
FS ADJUST resistor	R_{SET}		542		Ω	

THERMAL CHARACTERISTICS

	DP	HP	
Thermal resistance, chip-to-case θ_{jc}	12	17	°C/W
Thermal resistance, chip-to-ambient θ_{jA}	45	50	°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
As specified in Recommended Operating Conditions

DC CHARACTERISTICS

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Resolution (each DAC)		8			Bits	
Accuracy (each DAC)						
Integral linearity error	INL		±0.3	±1	LSB	
Differential linearity error	DNL		±0.3	±1	LSB	
Grey scale error			±1	±5	% grey scale	
Monotonicity			Guaranteed			
Digital Inputs						
Input high voltage	V_{IH}	3.0		V_{AA} + 0.3	V	Binary coding
Input low voltage	V_{IL}	AGND-0.3		1.2	V	
Input high current	I_{IH}			1	μA	
Input low current	I_{IL}			-1	μA	
Analog Outputs						
Grey scale current range		15		20	mA	
			255		LSB	
Output currents						
White level relative to blank level		17.69	19.06	20.40	mA	RS-343A tolerances assumed
			276		LSB	
White level relative to black level		16.74	17.62	18.50	mA	
			255		LSB	
Black level relative to blank level		0.95	1.44	1.90	mA	
			21		LSB	
Blank level on IOR, IOB		0	5	50	μA	
			0		LSB	
Blank level on IOG		6.29	7.62	8.96	mA	
			111		LSB	
Sync level on IOG		0	5	50	μA	
			0		LSB	
LSB size	LSB		69.1		μA	
DAC to DAC matching			2		%	
Output compliance	V_{OC}	-0.5		+1.4	V	
External V_{REF} input current	I_{REF}			10	μA	
Internal reference voltage	V_{REF}	1.14	1.20	1.26	V	
Internal V_{REF} temperature coefficient			40		ppm/°C	

AC CHARACTERISTICS

Characteristic	Symbol	VP101-5			VP101-3			Unit	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Max clock rate	f_{max}	50			30			MHz	
Data and control setup time	t_{SU}	6			8			ns	
Data and control hold time	t_H	2			2			ns	
Clock cycle time	t_{CYC}	20			33.3			ns	
Clock pulse width high time	t_{CLKH}	8			10			ns	
Clock pulse width low time	t_{CLKL}	8			10			ns	
Analog output delay	t_{DLY}		10			10		ns	
Analog output rise/fall time	t_{VRF}			8			9	ns	
Analog output settling time	t_S		12			15		ns	
Glitch impulse			100			100		pV-sec	
Analog output skew			0	3		0	3	ns	
Pipeline delay		1	1	1	1	1	1	Clock	
V_{AA} supply current	I_{AA}		120	175		100	140	mA	At f_{max}, V_{AA} = 5V

CIRCUIT DESCRIPTION

As shown in Fig. 2, the VP101 contains three 8-bit D-A converters, input latches, and a loop amplifier.

On the rising edge of each clock cycle (see Fig. 4), 24 bits of colour information (R_0-R_7, G_0-G_7, and B_0-B_7) are latched into the device and presented to the three 8-bit D-A converters. The REF WHITE input, also latched on the rising edge of each clock cycle, and will force the inputs of each D-A converter to $FF.

$\overline{SYNC}$ and $\overline{BLANK}$ are latched on the rising edge of the clock to maintain synchronisation with the colour data. These inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as shown in Fig. 3. Table 1 details how the $\overline{SYNC}$, $\overline{BLANK}$ and REF WHITE inputs modify the output levels.

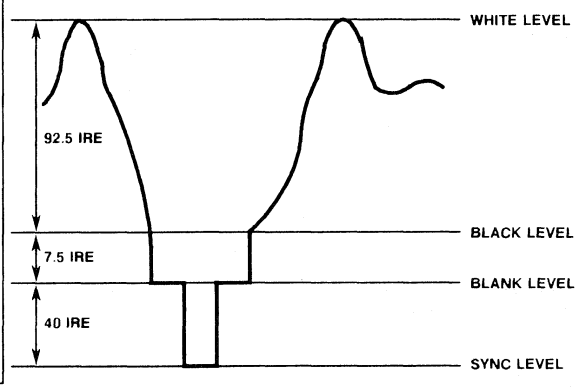
The I_{SYNC} current output is typically connected directly to the IOG output and is used to encode sync information onto the IOG output. If I_{SYNC} is not connected to the IOG output, sync information will not be encoded on the green channel, and the IOR, IOG and IOB outputs will have the same full scale output current.

Full Scale output current is set by an external resistor (R_{SET}) between the FS ADJUST pin and AGND. R_{SET} has a typical value of 542Ω for generation of RS-343A video into a 37.5Ω load. The VP101 may be used in applications where an external 1.2V (typical) reference is provided, in which case the external reference should be temperature compensated and provide a low impedance output.

The D-A converters on the VP101 use a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch energy are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifer stabilizes the full scale output current against temperature and power supply variations.

The analog outputs of the VP101 are capable of directly driving a 37.5Ω load, such as a doubly terminated 75Ω co-axial cable or interpolation filters.

Red/Blue		Green	
mA	V	mA	V
19.06	0.714	26.68	1.000
1.44	0.054	9.06	0.340
0.00	0.000	7.62	0.286
		0.000	0.000



NOTE : 75Ω doubly terminated load, R_{SET} = 542Ω, V_{REF} = 1.2V, I_{SYNC} connected to IOG, RS-343A levels assumed

Fig.3 Composite video output waveform

Description	IOG (mA)	IOR/IOB (mA)	REF WHITE	$\overline{SYNC}$	$\overline{BLANK}$	DAC I/P Data
White Level	26.68	19.06	1	1	1	$XX
White Level	26.68	19.06	0	1	1	$FF
Data	Data + 9.06	Data + 1.44	0	1	1	Data
Data-Sync	Data + 1.44	Data + 1.44	0	0	1	Data
Black Level	9.06	1.44	0	1	1	$00
Black-Sync	1.44	1.44	0	0	1	$00
Blank Level	7.62	0	X	1	0	$XX
Sync Level	0	0	X	0	0	$XX

NOTE : Typical with full scale IOG = 26.68mA, R_{SET} = 542Ω, V_{REF} = 1.2V, I_{SYNC} connected to IOG

Table 1 Video output truth table

PIN DESCRIPTIONS

Pin name	Description
$\overline{\text{BLANK}}$	Composite blank control input. A logic '0' forces the IOR, IOG and IOB outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logic zero, the R_0-R_7, G_0-G_7, B_0-B_7, and REF WHITE inputs are ignored.
$\overline{\text{SYNC}}$	Composite sync control input. A logic '0' on this input switches off a 40 IRE current source on the I_{SYNC} output. $\overline{\text{SYNC}}$ does not override any other control or data input, as shown in Table 1; therefore it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
REF WHITE	Reference white control input. A logic '1' on this input forces the IOR, IOG, and IOB outputs to the white level, regardless of the R_0-R_7, G_0-G_7 and B_0-B_7 inputs. It is latched on the rising edge of CLOCK. See Table 1.
R_0-R_7 G_0-G_7 B_0-B_7	Red, Green, and Blue data inputs. R_0, G_0, and B_0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary. Unused inputs should be connected to either the regular PCB power or ground plane.
CLOCK	Clock input. The rising edge of CLOCK latches the R_0-R_7, G_0-G_7, B_0-B_7 $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, and REF WHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated CMOS buffer.
IOR, IOG, IOB	Red, Green and Blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω co-axial cable. All outputs, whether used or not, should have the same output load. (Note: A DC path to ground must be maintained)
I_{SYNC}	Sync current output. Typically this current output is directly wired to the IOG output, and enables sync information to be encoded onto the green channel. A logic '0' on the $\overline{\text{SYNC}}$ input results in no current being output onto this pin, while a logic '1' results in the following current being output: $I_{SYNC}\ (mA) = 3468 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 111$ LSBs If sync information is not required on the green channel, this output may be connected to V_{AA} and the $\overline{\text{SYNC}}$ input tied high, causing the I_{SYNC} current source to be turned off, reducing the power consumption.
FS ADJUST	Full scale adjust control. A resistor (R_{SET}) connected between this pin and AGND controls the magnitude of the full video signal (Fig. 3). The current flowing in the R_{SET} resistor is equal to 32 LSBs. Note that the IRE relationships in Fig. 3 are maintained, regardless of the full scale output current. The relationship between R_{SET} and the full scale current on IOG (assuming I_{SYNC} is connected to IOG) is: $IOG\ (mA) = 12082 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 387$ LSBs The full scale output current on IOR and IOB for a given R_{SET} is defined as: $IOR, IOB\ (mA) = 8624 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 276$ LSBs
COMP	Compensation pin. This pin provides compensation for the internal loop amplifier. A 0.01μF ceramic capacitor must be connected between this pin and the nearest V_{AA} pin. Connecting the capacitor to V_{AA} rather than to AGND provides the highest possible power supply noise rejection.
V_{REF}	Voltage reference output. The output from an internal reference circuit, providing 1.2V (typical) reference. A 0.1μF ceramic capacitor must be used to decouple this output to V_{AA}.
AGND	Analog ground. All AGND pins must be connected.
V_{AA}	Analog power. All V_{AA} pins must be connected.

APPLICATION NOTES

RS-343A and RS-170 Video Generation

For the generation of RS-343A compatible video levels it is recommended that a doubly terminated 75Ω load be used with an R_{SET} resistor value of approximately 542Ω.

Similarly for the generation of RS-170-compatible video, it is recommended that a singly terminated 75Ω load be used with an R_{SET} value of about 774Ω. If the VP101 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75Ω and singly terminated 75Ω loads.

If driving a large capacitive load (load $RC > 1/20\pi f_C$) it is recommended that an output buffer with an unloaded gain > 2 be used to drive a doubly terminated 75Ω load.

COMP Resistor

To optimise the settling time of the VP101, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

Non-Video Applications

The VP101 may be used in non-video applications by disabling the video specific control inputs. REF WHITE should be a logic '0' while BLANK and SYNC should be a logic '1'. I_{SYNC} should be connected to V_{AA} or AGND. All three outputs will have the same full scale output current.

The relationship between R_{SET} and full scale output current (I_{out}) in this configuration is as follows:

$$I_{out}\,(mA) = 7968 \times \frac{V_{REF}\,(V)}{R_{SET}\,(\Omega)} = 255 \text{ LSBs}$$

$$\text{Note that 1 LSB} \equiv \frac{V_{REF}\,(V)}{32 \times R_{SET}\,(\Omega)}$$

With the data inputs at $00, there is a DC offset current (I_{min}) defined as follows:

$$I_{min}\,(mA) = 656 \times \frac{V_{REF}\,(V)}{R_{SET}\,(\Omega)} \equiv 21 \text{ LSBs}$$

Therefore, the total full scale output current will be $I_{out} + I_{min}$. The REF WHITE input may optionally be used as a 'force to full scale' control.

TIMING WAVEFORMS

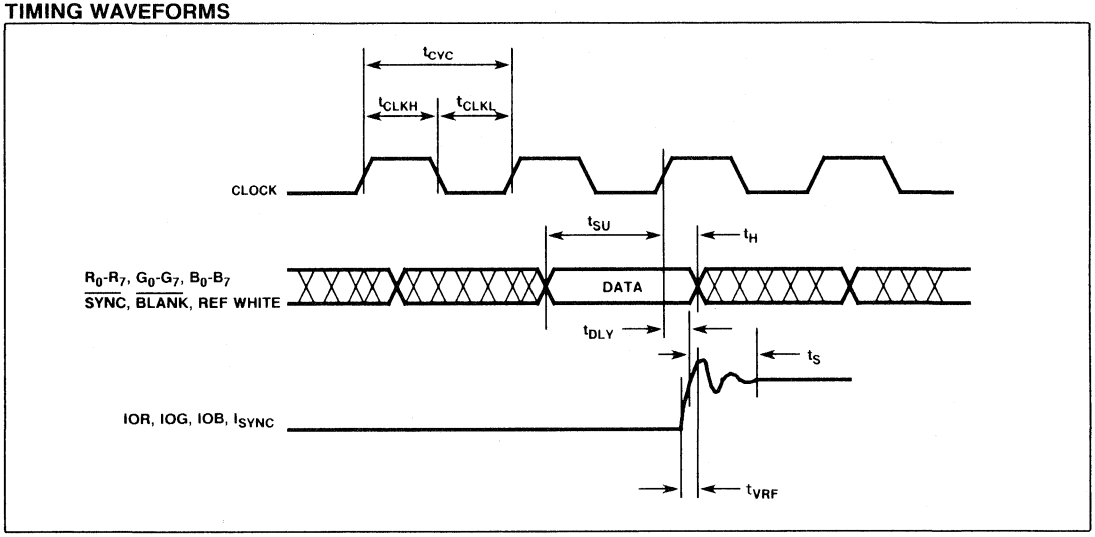


Fig.4 Input/output timing

NOTES

1. Output delay, t_{DLY}, measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.
2. Settling time, t_S, measured from the 50% point of full scale transition to the output remaining within ± 1 LSB.
3. Output rise/fall time , t_{VRF}, measured between the 10% and 90% points of full scale transition.

PCB LAYOUT CONSIDERATIONS

To obtain the optimum performance from the VP101 great care must be taken in the PCB layout to ensure low noise power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling.

Power and Ground Planes

The VP101 and its associated circuitry should have its own separate power/ground planes, which should be connected at a single point through a ferrite bead. It is important that the regular PCB power and ground planes do not overlay portions of the analog power or ground planes to minimise plane-to-plane noise coupling.

Digital Signal Interconnect

The digital signal lines to the VP101 should be isolated as much as possible from the analog circuitry. Due to the high clock rates used, the clock lines to the VP101 should be as short as possible to minimise noise pickup.

Any pull-up resistors used on the digital inputs should be connected to the regular PCB power plane, not to the analog power plane.

Supply Decoupling

Noise on the analog power plane will be further reduced by the use of multiple decoupling capacitors (See Fig. 5.)

Optimum performance is obtained with 0.1μF chip ceramic capacitors placed as close as possible to the V_{AA} pins, with the shortest leads possible to reduce lead inductance.

It should be noted that while the loop amplifier circuitry of the VP101 will reject power supply noise, this rejection decreases with frequency. Any high frequency noise on the regular supply (such as produced by a switch mode power supplies) must be adequately suppressed, else the designer should consider using a three terminal regulator to supply the analog power plane.

Analog Signal Interconnect

For optimum performance the analog output connectors and source termination resistors should be as close as possible to the VP101 to minimise noise pickup and reflections due to impedance mismatch. The video output signals should overlay the ground plane and not the analog power plane, to maximise the high frequency power supply rejection.

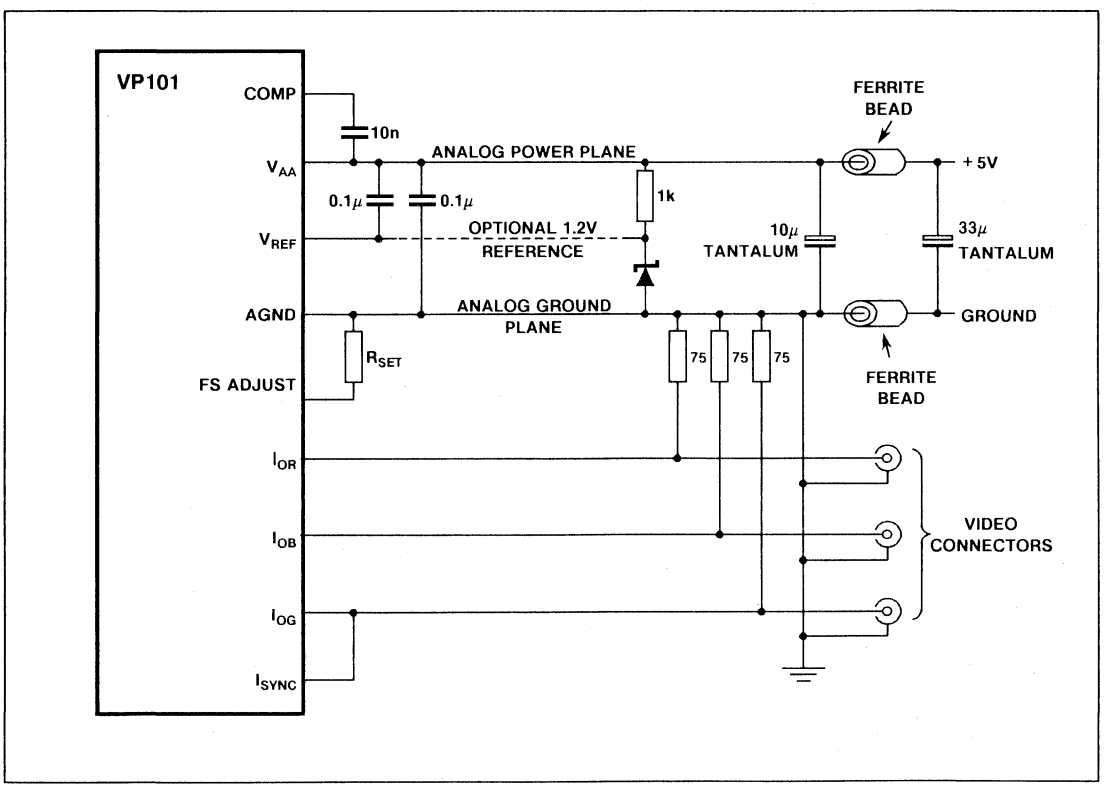


Fig.5 VP101 typical connections

ZN454E

TRIPLE 4-BIT VIDEO D-A CONVERTER

The ZN454 consists of three 4-bit D-A converters, providing a colour palette of 4096 possible display colours. The required logic translators, control logic, a reference voltage source and reference amplifier are also integrated on-chip.

Each D-A converter accepts 4-bit digital video data and SYNC/BLANK signals directly from a TTL source and produces a composite video output to directly drive a 75Ω line terminated by a 75Ω load at both ends.

The ZN454 is ideally suited for pixel colour generation in graphics display systems requiring 4-bit colour resolution. The high linearity of each DAC ensures excellent colour contrast and the fast update rate allows the device to be interfaced to monitors with a resolution of up to 1024 x 1280 pixels assuming a standard refresh rate of 60Hz.

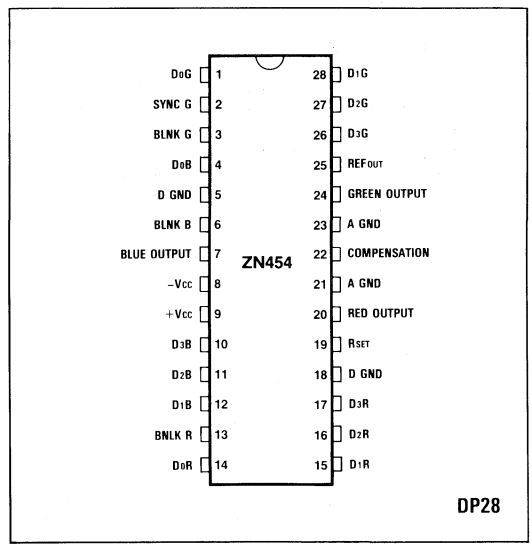


Fig.1 Pin connections - top view

FEATURES

- 3 Video DAC's - Ideal for Colour Graphics
- Fast, 8ns Settling Time
- Update Rates to 100MHz
- Low Glitch Energy
- ¼ LSB Linearity Error
- On-Chip Reference Source
- Composite Sync and Blank Inputs
- TTL Compatible Inputs
- Generates Standard Video Signal Output Across a Doubly Terminated 75 Ohm Load
- 28 Pin DIL Package

GENERAL CIRCUIT DESCRIPTION

Each D-A converter of the ZN454 uses high speed switches to steer current from precision current sources to either analog ground or to the analog output - as governed by the digital inputs (see Fig.4). The analog output voltage is now obtained from these weighted current sources producing the desired voltage drop across the 37.5Ω load impedance. The gain of the D-A converters is adjustable via RSET.

Since the ZN454 utilises current output DAC's the output impedance is inherently high. Thus a 75Ω resistance is required (adjacent to each DAC output) to shunt this high impedance and provide the correct impedance for driving a 75Ω line terminated in 75Ω at the monitor. The desired 1V p-p composite signal will now be developed across this effective 37.5Ω output impedance.

The grey scale output current of each DAC has 16 levels from 0 to -17mA nominally (see Fig.3). This develops 16 levels of output voltage from 0 to -643mV across the specified 37.5Ω load impedance. the 'REFERENCE WHITE' level (0V) corresponds to the digital input code 1111 and the 'REFERENCE BLACK' (-643mV) to 0000.

A logic '1' on the BLANK input overrides the data inputs and drives the output to 71mV more negative than the 'REFERENCE BLACK' level. This corresponds to the 'BLANKING' (or 'blacker-than-black') level.

Activating the SYNC input (logic '1') with the BLANK input 'high' drives the output to 286mV more negative than the 'BLANKING' level. This voltage (nominally -1V) corresponds to the 'SYNC' level.

GAIN ADJUSTMENT (RSET)

RSET provides a means of adjusting the current in the weighted current sources. An amplifier compares the voltage developed across RSET, with the reference voltage. If RSET is increased/decreased the amplifier output causes the current through RSET to decrease/increase (to bring the voltage across RSET back in line with the reference voltage). This also causes the current in each of the current sources to decrease/increase (see Fig.3). In this manner the magnitude of the output waveform can be varied to obtain the desired levels.

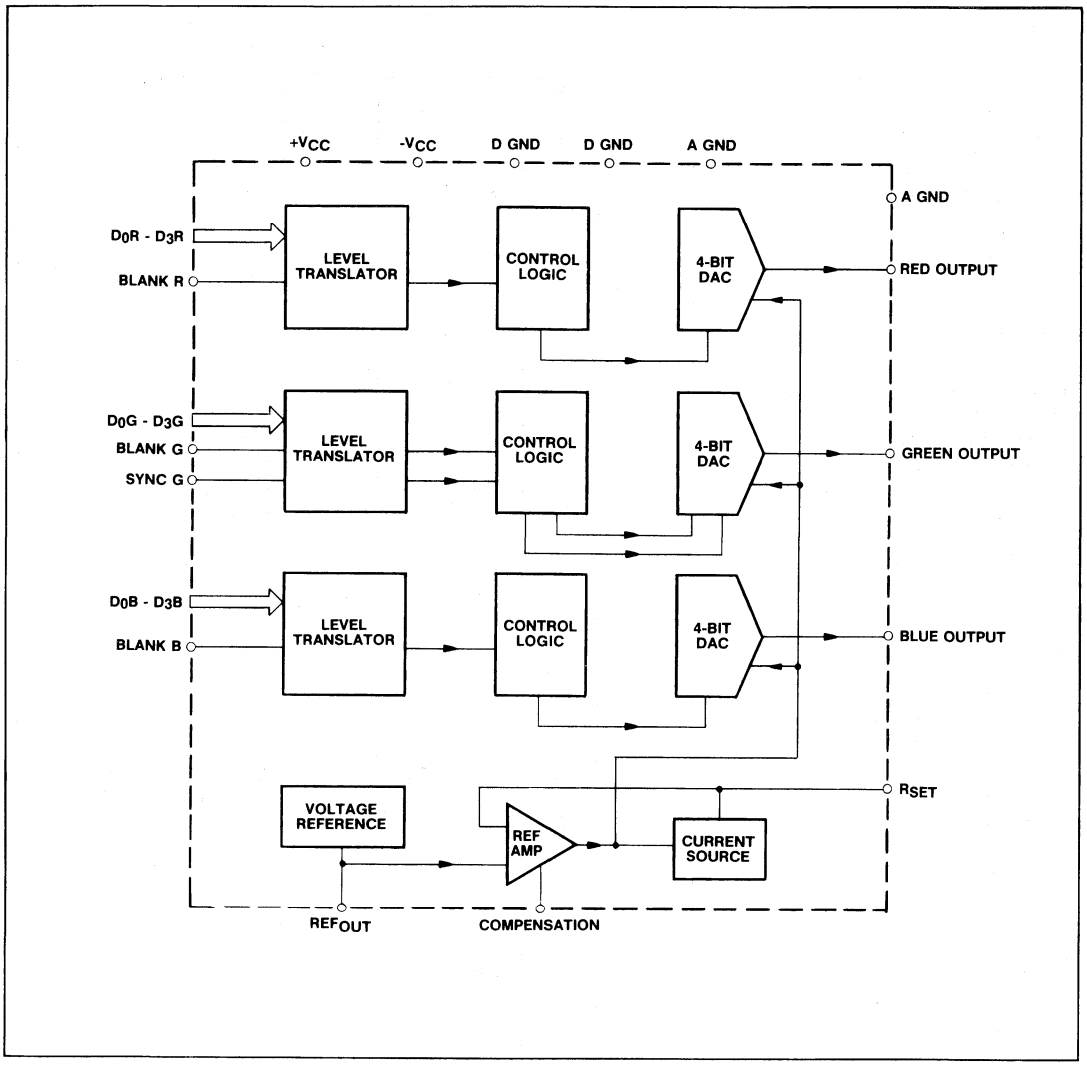


Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage, +Vcc	+6V
Supply voltage, -Vcc	-6V
Logic input voltage	+Vcc
Operating temperature range	0°C to 70°C
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C, V_{CC} = ±5V, R_L = 37.5Ω and R_{SET} = 180Ω

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Resolution		4			Bits	
LSB weight (current)			1.13		mA	Note 1
LSB weight (voltage)			43		mV	
Accuracy						
Linearity error			±0.25	±0.5	LSB	
Differential linearity error				±0.5	LBS	Note 2
Offset error			-5.0	-15.0	mV	
Gain error				±5	% of nom.FSR	
Speed performance - Grey scale output						
Rise/fall times (voltage)			3		ns	10-90% of final value
Settling time (voltage)			8		ns	Note 3
Maximum update rate			100		MHz	Note 4
Slew rate			180		V/μs	10-90% of final value
Glitch energy			60		pV-s	Note 5
Temperature coefficient						
Offset			10		ppm/°C	Measured with
Gain			500		ppm/°C	internal reference
Data, sync and blank inputs						
Logic compatibility			**TTL**			
High level input voltage	V_{IH}	2.0			V	
Low level input voltage	V_{IL}			0.8	V	
High level input current	$I_{IH(1)}$			+20	μA	V_{CC} = max, V_{in} = 5.5V
	$I_{IH(2)}$			±10	μA	V_{CC} = max, V_{in} = 2.4V
Low level input current	I_{IL}			-1.6	mA	V_{CC} = max, V_{in} = 0.4V
Coding (see Fig.2)			**Complementary binary**			
Output - Grey scale						
Voltage range			0.64		V	Note 1
Current range			17		mA	
Output - Composite sync						
Voltage range			286		mV	
Current range			7.6		mA	
Output - Composite blanking						
Voltage range			71		mV	
Current range			1.9		mA	
Output voltage compliance		0		1.5	V	
Internal voltage reference						
Output voltage	V_{REF}		-1.26		V	
Output voltage tolerance				±5.0	%	
Output voltage TC			200		ppm/°C	0°C to 70°C
Power supply requirements						
Supply voltage	+V_{CC}	4.5	5.0	5.5	V	
	-V_{CC}	-4.5	-5.0	-5.5	V	
Supply current	+I_{CC}		22.5		mA	
	-I_{CC}		136.0		mA	

NOTES
1. LSB and full-scale output levels adjustable with R_{SET}.
2. Monotonicity guaranteed over full operating temperature range.
3. The settling time was measured as the time between the start of the output rising/falling edge to where the output entered and remained within ±½ LSB of the final value. The value quoted is for a transition from reference white to reference black and vice versa, and does not include the inherent input propagation delay (2-3ns). See section describing settling time measurement.
4. The maximum update rate is limited by the full-scale settling time to rated accuracy.
5. Measurement of glitch energy is discussed in a later section of this data sheet.

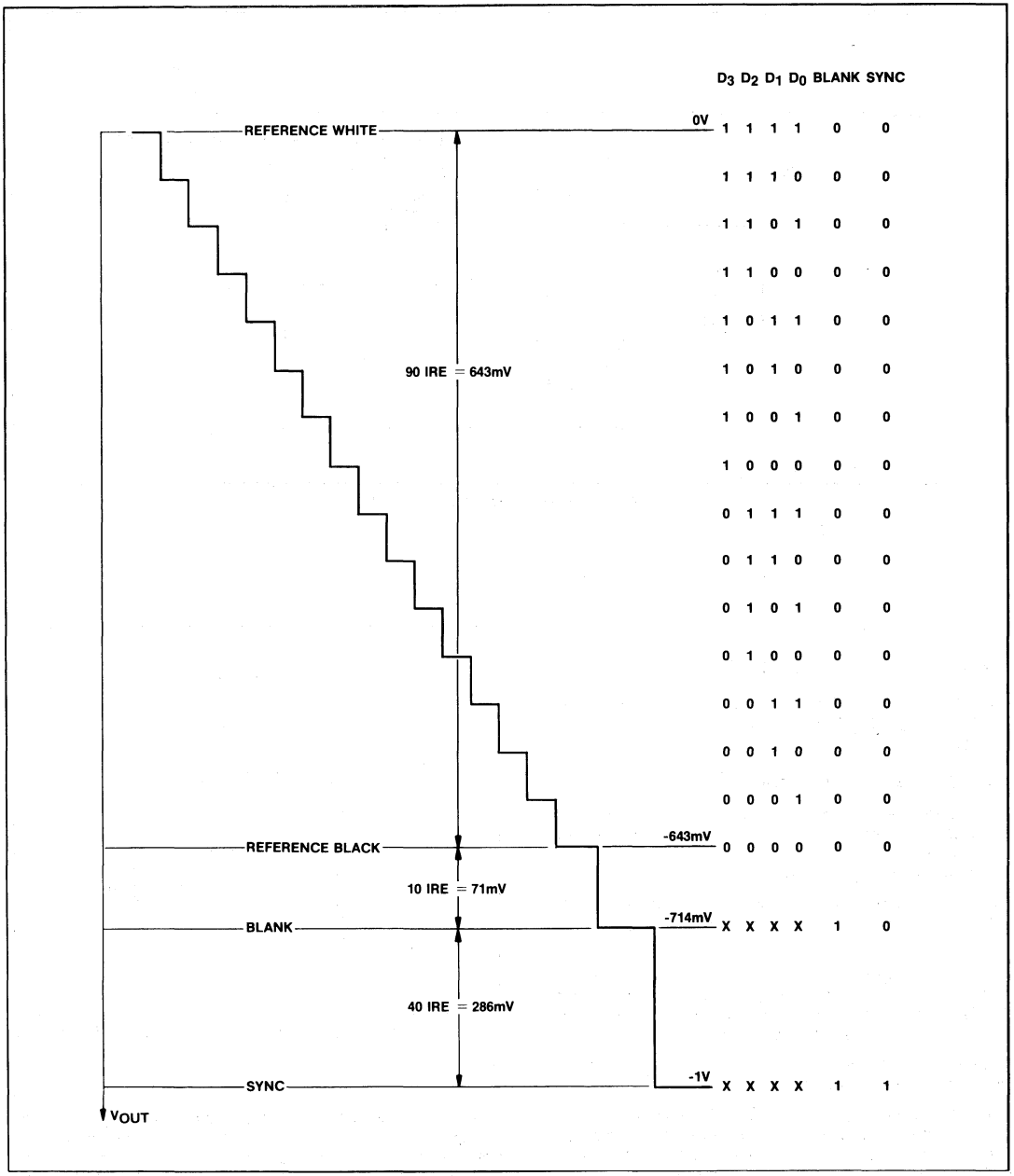


Fig.3 Typical composite video output waveform

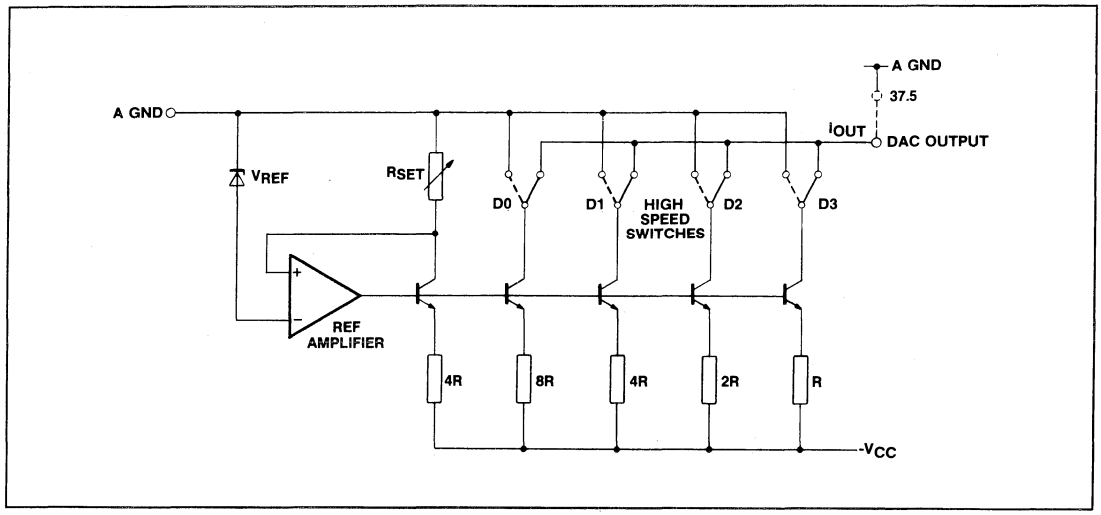


Fig.4 Current source array (schematic)

DIGITAL INPUTS

The digital inputs are high speed level translators (see Fig.5).

The ZN454 requires very few external components for normal operation. Fig.6 illustrates the external component connections.

LAYOUT CONSIDERATIONS

When using the ZN454, as with any other device of this kind, certain precautions must be taken to obtain the best performance.

Some of the requirements are:

1. A ground plane board providing a good earth and with good power supply connections, to keep noise to a minimum.

2. Good decoupling - especially around all the fast switching circuits - including a 0.1μF capacitor from both the +5V and -5V supplies positioned close to the ZN454. The ground connections for these capacitors should be adjacent.

3. Some physical separation between the digital input tracks to minimise crosstalk.

4. Matched digital input signal paths to avoid introducing any unnecessary time skew between the inputs. This would cause glitches on the DAC outputs with changing codes. Also the outputs from the driving device will have to be well matched for the same reason.

5. 75Ω resistors close to the DAC outputs, to provide the correct impedance for driving 75Ω lines.

SETTLING TIME AND GLITCH ENERGY MEASUREMENT

In a finished design the ZN454 would be soldered directly into the board to obtain the best performance possible. However for evaluation purposes a socket really needs to be used. This will give some degradation in performance but useful results can still be obtained.

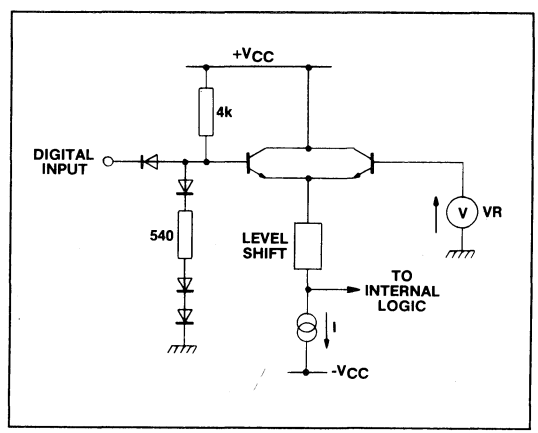


Fig.5 Equivalent circuit of sync, blank and data inputs

Measurement of settling time and glitch energy is not a straightforward task and all of the recommendations previously noted must be adhered to. If these parameters are to be measured using an oscilloscope, great care must be taken to avoid corrupting the analog outputs e.g. conventional probes cannot simply be clipped onto the outputs as this would cause reflections giving rise to errors. Instead the ZN454 needs a 75Ω termination near the chip, a 75Ω cable - also grounded close to the chip - connecting to a 75Ω lead through termination at the oscilloscope. Optimum cable length is about 6 inches but it may need trimming around this. Also the oscilloscope obviously needs to have sufficient bandwidth to cope with the rise and fall times encountered.

The digital circuits driving the DAC's must not introduce too much noise, or time skew between the bit inputs. This

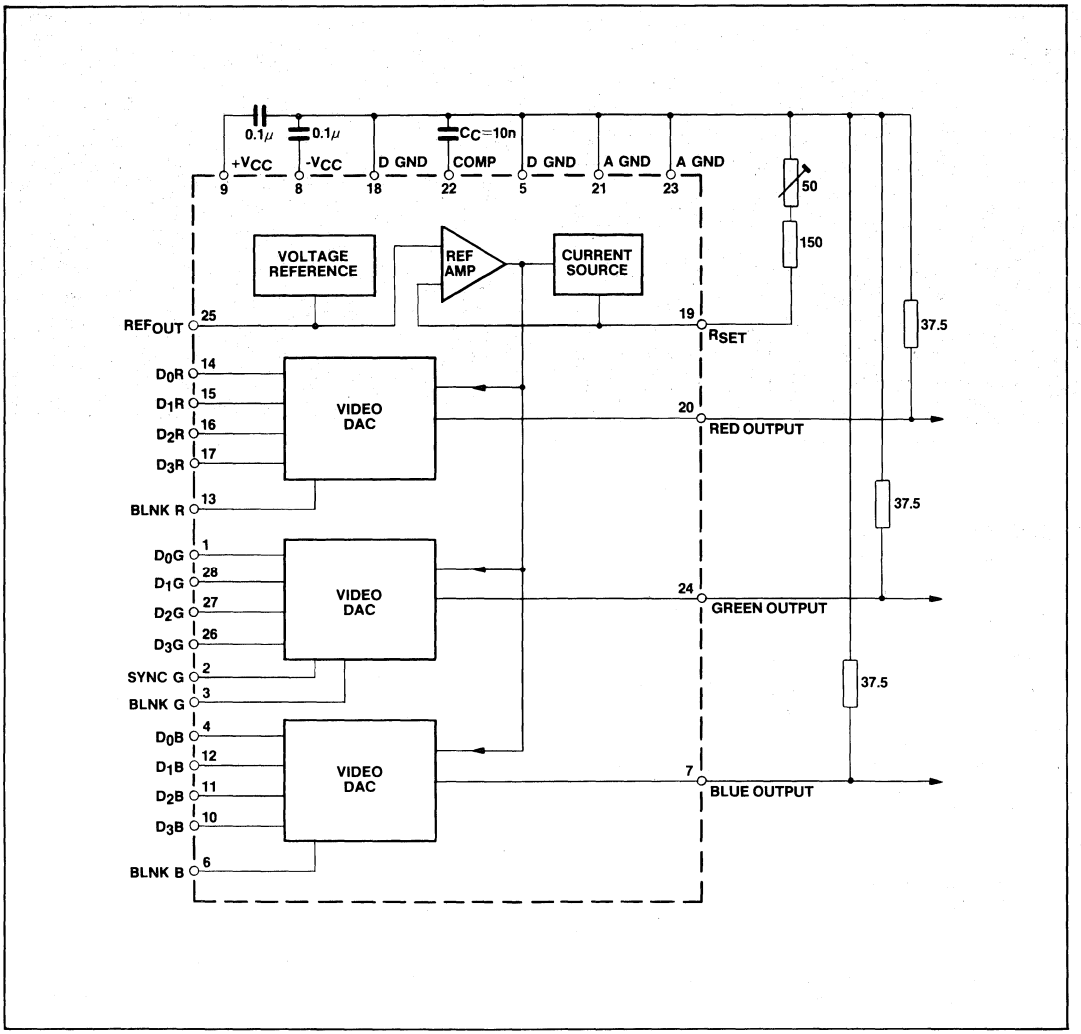


Fig.6 External component connections

can considerably affect the results. However, a convenient way of minimising these problems for evaluation purposes, is to drive the digital inputs directly from a pulse generator. Full-scale transitions of the grey scale can now be monitored by wiring the inputs to a given DAC in parallel (terminating in 50Ω) and clocking with the pulse generator. Each output can now be examined in turn. The circuit diagram is as in Fig.6 except that the sync and blank inputs will be tied low. The 37.5Ω terminations on the DAC output, and the digital input signals are provided as described above. Fig.7 shows an actual full-scale (grey scale) output transition measured using the above procedure, giving a settling time of 5.12ns.

Glitch energy measurements, at the major transition for example, can also be measured by driving the digital inputs directly from a pulse generator but it will need to have well matched complementary outputs. Also the lead lengths from the generator to the digital inputs will have to be well matched (and terminated in 50Ω). This is so because this measurement is especially critical of any time skew between the input signals. Indeed even an ideal DAC would produce glitches if there were timing differences between these changing input signals. These time skew errors which would manifest themselves as exaggerated glitches on the DAC output, are referred to the point at which the input signals cross the digital input thresholds (≏1.5V nom.). Thus the characteristics of the driving signals will have some effect on the amplitude of the glitches, which may be minimised by careful design. The circuit arrangement for measuring the glitch energy is as above but with the digital inputs being switched through different codes. Fig.8 shows an actual mid-scale glitch, measured using the above procedure.

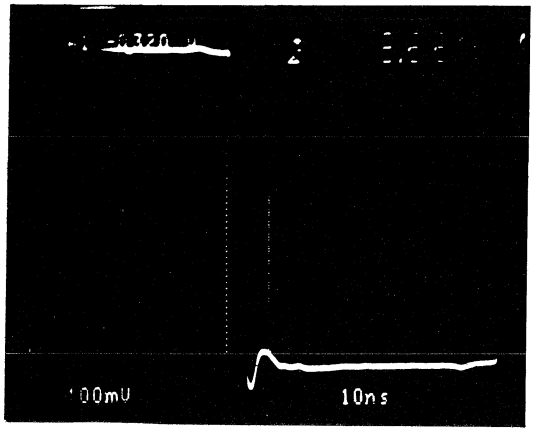


Fig.7 Full-scale output transition - settling time

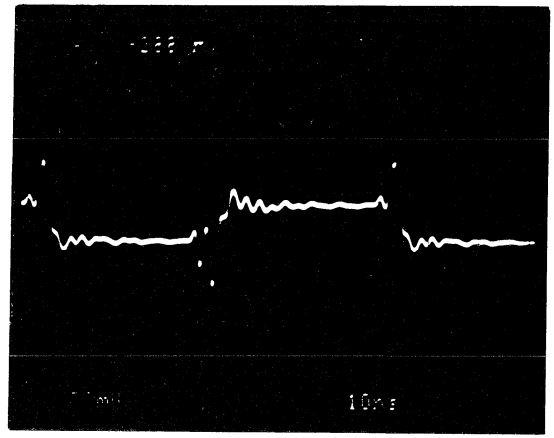


Fig.8 Mid-scale output glitch

GLOSSARY OF VIDEO TERMS

Raster scan

The method of sweeping a CRT one line at a time to generate and display images.

Composite video signal

The VIDEO signal plus the BLANK and SYNC signals.

Video signal

The portion of the composite VIDEO SIGNAL which varies in grey scale levels between 'reference white' and 'reference black' - this is the portion which is visually observed.

Sync signal

The portion of the video waveform that synchronises the raster scanning process.

Grey scale

The discrete levels between and including 'reference white' and 'reference black' - there are 16 levels for a 4-bit DAC.

Blanking level

The level separating the SYNC portion from the VIDEO portion. Usually referred to as the FRONT PORCH or BACK PORCH, this is the level which will shut off the electron guns resulting in the blackest possible display.

Sync level

The negative peak level of the sync signal.

Reference black level

The maximum negative level of the VIDEO signal.

Reference white level

The maximum positive level of the VIDEO signal.

MV1733

MAC SOUND CIRCUIT

The MV1733 is the sound circuit for the Nordic VLSI C/D/D2 MAC Packet receiver chipset.

The MV1733 receives packets of data from the MV1720 control chip. Packets for the desired sound service and Interpretation Block (BI) packets are recognised and processed. The configuration of the sound is automatically controlled by information in the BI packet. Descrambling of sound and scale factor extraction is done before the packet is stored in an external DRAM. The RAM is a buffer which helps to adjust the varying packet arrivals to a regular output sample frequency. The samples are read from the RAM into the MV1733 for further processing. Errors are detected and corrected before they are forwarded to external chips for error concealment, digital filtering and D/A conversion. A microcomputer supplies the MV1733 with the control word for descrambling, packet address etc. via the MV1720 and configuration chain.

FEATURES

- Simultaneous Processing of Two Independent Sound Services
- Digital Mixing of Main Sound and Commentary
- Digital Attenuation/Muting of each Sound Service
- Linear and Companded Sound Decoding
- First or Second Level Error Correction
- Stereo, Mono, High Quality and Medium Quality Sound
- BI Packets Processed in Hardware on Chip
- Indicates News Flash to Controlling Microprocessor
- Conditional or Free Access Sound
- Several MV1733s (and MV1732s) can be used in Parallel
- Software Compatible with the MV1732
- Can use either DRAM or SRAM for External Packet Buffer
- SONY Sound Bus Output

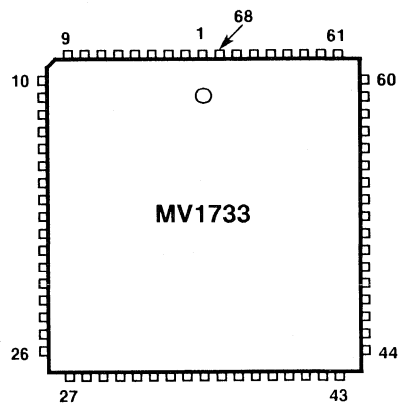
ASSOCIATED DEVICES

SL1700, MV1710, MV1720, MV1732, MV1745

DESCRIPTION OF SIMPLIFIED BLOCK DIAGRAM

Packet Control

The packet control module, provides for packet reception at 20.25Mbit/s and timing for further packet processing. Each incoming packet has a header with a 10 bit address, one bit indicating in which subframe it is located, and two bits used as a continuity index. The packet header of each packet is compared with the contents of the configuration chain, and packets which match address and subframe are extracted. The continuity index is checked and packet loss is flagged.



HP68

Pin	Function	Pin	Function
1	CLAB2	35	ADDR9
2	WSAB2	36	OE
3	40CLK1	37	V_{DD}
4	EFAB1	38	ADDR8
5	WCLK1	39	ADDR7
6	DAAB1	40	ADDR6
7	CLAB1	41	V_{SS}
8	WSAB1	42	ADDR5
9	PURST	43	ADDR4
10	EFCNT	44	ADDR3
11	V_{DD}	45	ADDR2
12	CLK1	46	V_{SS}
13	VSS	47	ADDR1
14	CDATAIN	48	ADDR0
15	CSTRB	49	IRQ
16	DATA7	50	WE
17	SIV	51	V_{DD}
18	SIC	52	MIXI
19	DATA6	53	CDATAOUT
20	D / S	54	V_{SS}
21	DATA5	55	RESIRQ
22	V_{DD}	56	NFI
23	DATA4	57	COMEN
24	DATA3	58	XC2
25	VAL	59	X22
26	PDATA	60	X12
27	DATA2	61	V_{DD}
28	DATA1	62	XC1
29	V_{SS}	63	X21
30	DATA0	64	X11
31	RAS/ADDR12	65	4OCLK2
32	W/ADDR11	66	WCLK2
33	Vss	67	EFAB2
34	CAS/ADDR10	68	DAAB2

Fig.1 Pin connections - top view

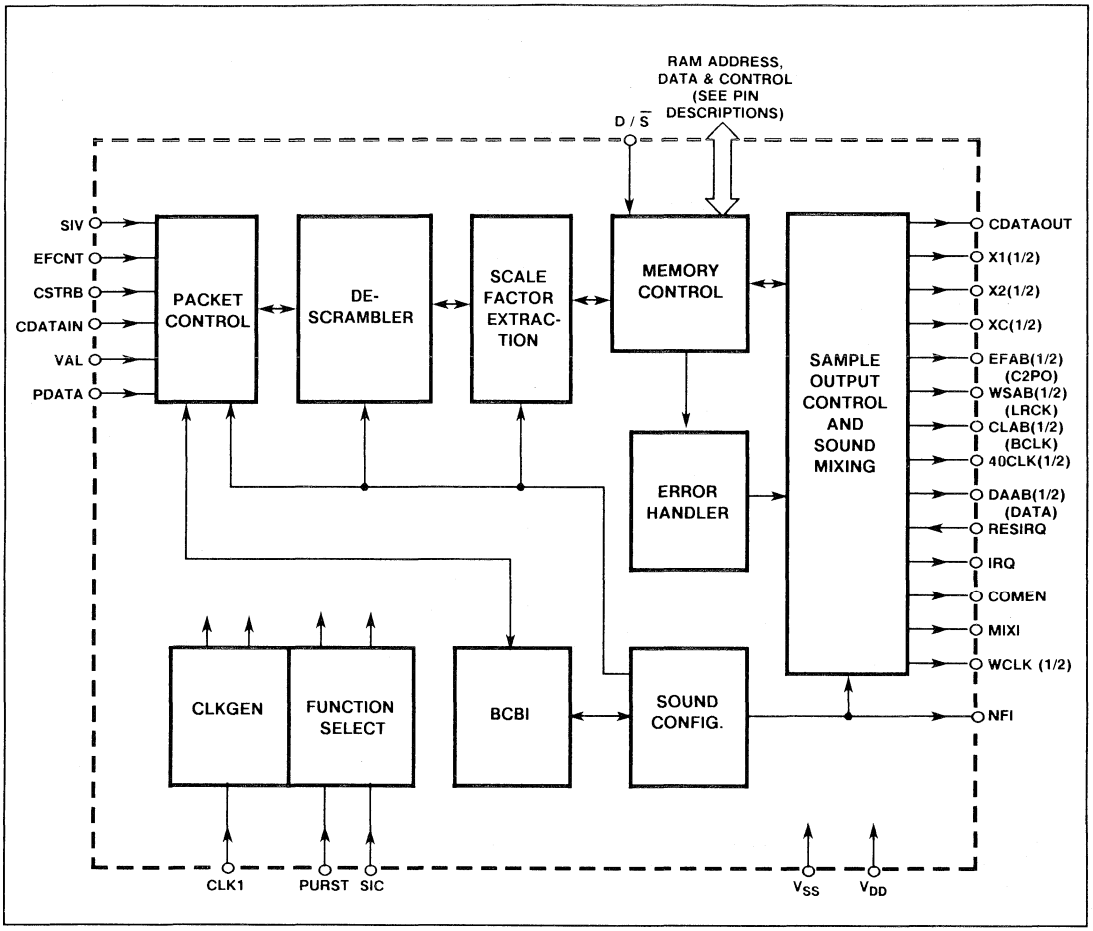


Fig.2 Simplified Block diagram for MV1733 MAC sound chip

PIN DESCRIPTIONS

Symbol	Type	Pin	Description
V_{DD}	Supply	11,22,37, 51,61	Power Supply +5V. All pins must be connected.
V_{SS}	Supply	13,29,33,41, 46,54	Power Supply 0V. All pins must be connected.
CLAB (1/2)	Output	7,1	Output clock 2.048MHz. Sound service 1 and 2. (BCLK*)
WSAB (1/2)	Output	8,2	Word select. 0 = left sample, 1 = right sample. Sound service 1 & 2. (LRCK*)
40CLK (1/2)	Output	3,65	Output clock 8.192MHz. Sound service 1 and 2.
EFAB (1/2)	Output	4,67	Error Flags. Active high indicates bit errors in the sample. Sound service 1 and 2. (C2PO*)
WCLK (1/2)*	Output	5, 66	Specific SONY sound bus signal. Falling edge comes after the LSB of each left and right sample. Sound services 1 and 2.
DAAB (1/2)	Output	6,68	Sound samples. 16-bit serial sound data where the two LSBs are always Zero. Sound service 1 and 2. (DATA*)
PURST	Input	9	Power Up & Reset. Sets all internal registers to Zero.
EFCNT	Input	10	MSB of internal 8-Bit frame count, FCNT. Toggles in bit 3 in line 625 every 128th frame. Generated by MV1720.
CLK1	Input	12	20.25MHz single-phase master clock.

* Symbol names used in SONY data sheets for SONY sound bus.

PIN DESCRIPTIONS (continued)

Symbol	Type	Pin	Description
CDATAIN	Input	14	Configuration chain Input.
CSTRB	Input	15	Strobe signal; when high the configuration data are shifted into the configuration chain.
DATA0-DATA7	I/O	30,28,27, 24,23,21,19,16	Input/Output of sound data to/from buffer RAM. In DRAM mode only D0 to D3 are used.
SIV	Input	17	Sample strobe. Active for UDT, SDF and RDF fields in line 625. Generated by MV1720.
SIC	Input	18	For test purposes only. MUST be connected to PURST.
D / $\overline{S}$	Input	20	Controls whether the MV1733 uses external DRAM or SRAM, (1 = Dram, 0 = SRAM).
VAL	Input	25	Indicates every packet header on PDATA. Duration 13 clocks. Generated by MV1720.
PDATA	Input	26	Packet data (sound/data/line 625 'packet') 20.25Mbits/s spectrum descrambled, de-interleaved and decoded corrected data.
$\overline{RAS}$	Output	31	Row address strobe. Latches the row address on the falling edge. Used in DRAM mode only; in SRAM mode this pin is ADDR 12.
$\overline{W}$	Output	32	Write enable pin. Selects read or write modes ($\overline{W}$ = 0 is write mode). Used in DRAM mode only, in SRAM mode this pin is ADDR11
$\overline{CAS}$	Output	34	Column Address strobe. Latches the column address on the falling edge. Used in DRAM mode only; in SRAM mode this pin is ADDR 10.
ADDR0-ADDR12	Output	48,47,45, 44,43,42, 40,39,38 35,34,32,31	Address pins for external RAM. In DRAM mode, only ADDR 0 to ADDR 7 are used.
$\overline{OE}$	Output	37	Output enable signal for static RAM.
IRQ	Output	49	Sound Chip mix interrupt request.
$\overline{WE}$	Output	50	Write enable signal for static RAM.
MIXI	Output	52	Mixing intended. Bit 4 byte 2 in BI block in sound service 2.
CDATAOUT	Output	53	Configuration chain output.
RESIRQ	Input	55	External reset for the IRQ signal.
NFI	Output	56	News flash indication, logical OR for Sound Services (bit 3, byte 1 BI block).
COMEN	Output	57	Indicates Channel 2 fade in if the signal is high.
XC (1/2)	Output	62,58	Oscillator Frequency Control. Sound service 1 & 2.
X1 (1/2)	Input	64,60	Inputs Crystal Oscillator Sound Service 1 & 2.
X2 (1/2)	Output	63,59	Outputs Crystal Oscillator Sound Service 1 & 2.

BCBI

The BCBI module processes the packet type byte (PT), and determines whether it is a BI, Sound Coding Block (BC1 or BC2) packet. This module also stores changes from BC1 to BC2 and vice versa, and indicates new sound configuration when three packets are received after the change has occurred. The two sound services are handled independently.

Sound Configuration

The sound configuration block handles BI packets. The structuring bytes are error checked (Hamming protection), and if correct, the Bytes 1 and 2 are majority voted over the 5 repetitions. The current sound configuration is updated each time a BI packet is accepted. A new sound configuration is updated when three BC packets are received after a change BC1 to BC2, or BC2 to BC1.

Descrambler

The descrambler handles the two different sound services independently, and synchronisation can be achieved at the start of new frames.

It supports the three different levels of access control described in the MAC standard. (ref .1)

Free access, unscrambled:

The sound data is unchanged.

Free access, scrambled:

The sound data is descrambled with a local control word stored in the receiver.

Conditional access, scrambled:

The sound data is descrambled with a control word from the conditional access system.

The signal EFCNT is the MSB in a frame counter, and it is used to re-synchronise the descrambler. The other bits may be supplied by the configuration chain, to assure fast recovery after change of channel or power up.

The signal SIV starts an update of the descrambling system for each frame.

The control word for descrambling is provided by the configuration chain.

Scale Factor Extraction

The scale factor is extracted by majority decision logic. Nine samples are evaluated for each bit in the scale factor as described in the EBU specification (ref. 1). The control information intended for high speed switching is also extracted.

Memory Block

The external memory can either be DRAM or SRAM controlled by D / $\overline{S}$ (pin 20) .

In DRAM mode the MV1733 can interface to either a 4x16K DRAM or a 4x64K DRAM. The MV1733 generates the address, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ signals. Writing is done in page mode. There are a minimum of 256 refresh cycles per 4ms.

In SRAM mode the MV1733 interfaces to an 8x8K SRAM generating $\overline{OE}$ and $\overline{WE}$ signals.

The number of packets in the RAM varies the sample output frequency slightly to maintain the buffer between 14 and 20 packets. A maximum of 32 packets can be stored per sound service.

Errors such as packet loss, full buffer and empty buffer are handled to minimise sound distortion. The parity bit is restored according to the scale factor and Control Information Bits (CIB) before the sound samples are sent to the error handler.

Error Handler

The Error Handler receives data from Memory Control and checks for errors. Four types of checks are done according to the data format:

Range checking (and if possible correction) according to scale factor and coding method (linear/companded).

Parity check (first level protection) for linear and companded data.

Hamming code check with single bit error correction for linear and companded data (second level protection).

Final range checking according to scale factor and coding method.

If non-correctable errors are detected, the sample is flagged for concealment.

In addition the Error Handler does Range Limiting (for linear coding) and Range Expansion (for companded coding) before data is presented to the Sample Output Control Module.

Sample Output Control

The block contains an oscillator and output buffer for each of the two sound services, and a sound mixing unit. The sound mixing unit makes it possible to mix main sound in channel 1 and commentary sound in channel 2. The resulting sound is output on sound service 1 pins.

When the FMIX bit is turned off, the control information for the sound mixing received in the BI packets is used. If a change in the sound mixing conditions occur an interrupt request (IRQ) is generated.

The polarity and reset of the IRQ is controlled by the configuration chain. IRQ can be reset by the bit IRE in the configuration chain, or by the external signal RESIRQ.

The direction flag COMEN indicates the fade up/down direction. COMEN = 1 is fade up commentary sound.

The channel 1 attenuation is controlled by the configuration chain bits X (9..0). The channel 2 attenuation by bits Y (9..0).

The pin MIXI is controlled by the Commentary channel BI packet and indicates when mixing is intended.

The bit MIX in the configuration chain selects if mixing is required or not.

If the bit FMIX in the configuration chain is turned on, the samples from both services are scaled and mixed independent of the BI packet information and the MIX bit.

The frequency of the oscillator controls the sample output rate. In order to maintain the sample storage in the RAM between 14 and 20 packets, the oscillator frequency is shifted slightly (± 150ppm).

A frequency determining network, consisting of an 8.192MHz crystal and three capacitors connected to X1, X2 and XC, See Fig 3. Frequency control is exercised by pulsing XC.

The error flag indicates unreliable sample data.

Each sample is expanded from 14 to 16 bits by inserting zeros in the two LSB's. The sample output frequency is always 32kHz.

When the B1 packet defines medium quality sound with 16kHz sample frequency, every second sample is supplied from a digital oversampling filter in Sound Channel 2 and output on Sound Service 2 pins. If only one sound service output is used Channel 2 Sound can be output on Sound Service 1 pins by enabling the FMIX bit in the configuration chain.

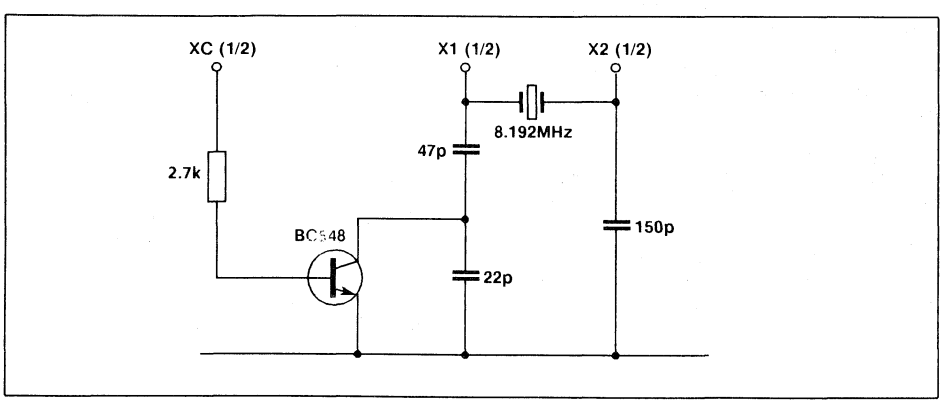


Fig.3 Crystal oscillator circuit.

THE CONFIGURATION CHAIN

The configuration chain is effectively a long shift register running through all circuits which are to be configured from the microcomputer.

Several function blocks of the MV1733 are controlled by the configuration chain. The packet control block needs the packet addresses and indication of which subframe (or both) to select packets from. In addition one bit per sound service is used for muting until a stable state is reached after change of sound service, or after power up.

The configuration chain also provides control words for descrambling. The two services can be descrambled independently.

In addition, the seven least significant bits of the frame count (FCNT), and one bit (NEWFC) indicating update of the frame count after a change of service or power up, are placed in the configuration chain.

The sound mixing can be turned on and off, and the mixing levels for both sound services are controlled independently.

The configuration chain may be updated from the microprocessor at any time except in line 625 and line 1.

The configuration data is clocked into the chain when CSTRB is high, otherwise the contents of each register stage is stored.

Configuration Chain Update

After power up or change of service the corresponding control word, CW, for descrambling should be transmitted to the configuration chain as soon as a valid control word is available, together with the 7 LSBs of the frame count FCNT (the MSB is provided by EFCNT). If the control bit NEWFC = 1, the descrambling control word will be updated in the first line 625 (SIV = 1). If NEWFC = 0, the descrambling control word will be updated when EFCNT changes from '1' to '0' in the next line 625. Thus, in a stable state it is not necessary to provide the CW every frame.

After power up or change of sevice, new address and subframe indication should be provided at the same time as the new CW and FCNT. Packets will be stopped until the new sound configuration is stable. A new address is indicated in the configuration chain by setting NAD low for one or more frames, and then high again indicating a stable address. After acceptance of a BI packet with the new address, the new BI configuration is applied. After the initialization is completed the sound packets are enabled for further processing. When NAD is low the sound is muted.

The contents of the configuration chain for the sound chip is shown in Table 1. Bytes 0 to 2 cover the sound mix. Bytes 3 to 13 cover sound service 2, while bytes 14 to 24 cover sound service 1.

Sound mix :

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Y3	Y2	Y1	Y0	MIX	IRE	IP0	FMIX ← LSB Sent First
1	X1	X0	Y9	Y8	Y7	Y6	Y5	Y4
2	X9	X8	X7	X6	X5	X4	X3	X2

Sound service 2:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3	NEWFC	F6	F5	F4	F3	F2	F1	F0
4	CW7	CW6	CW5	CW4	CW3	CW2	CW1	CW0
5	CW15	CW14	CW13	CW12	CW11	CW10	CW9	CW8
6	CW23	CW22	CW21	CW20	CW19	CW18	CW17	CW16
7	CW31	CW30	CW29	CW28	CW27	CW26	CW25	CW24
8	CW39	CW38	CW37	CW36	CW35	CW34	CW33	CW32
9	CW47	CW46	CW45	CW44	CW43	CW42	CW41	CW40
10	CW55	CW54	CW53	CW52	CW51	CW50	CW49	CW48
11	X	X	X	X	CW59	CW58	CW57	CW56
12	PA6	PA5	PA4	PA3	PA2	PA1	PA0	NAD
13	X	X	X	L12	L11	PA9	PA8	PA7

Sound service 1:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
14	NEWFC	F6	F5	F4	F3	F2	F1	F0
15	CW7	CW6	CW5	CW4	CW3	CW2	CW1	CW0
16	CW15	CW14	CW13	CW12	CW11	VW10	CW9	CW8
17	CW23	CW22	CW21	CW20	CW19	CW18	CW17	CW16
18	CW31	CW30	CW29	CW28	CW27	CW26	CW25	CW24
19	CW39	CW38	CW37	CW36	CW35	CW34	CW33	CW32
20	CW47	CW46	CW45	CW44	CW43	CW42	CW41	CW40
21	CW55	CW54	CW53	CW52	CW51	CW50	CW49	CW48
22	X	X	X	X	CW59	CW58	CW57	CW56
23	PA6	PA5	PA4	PA3	PA2	PA1	PA0	NAD
24	X	X	X	L12	L11	PA9	PA8	PA7

Table1 (part 1) Contents of the configuration chain for the MV1733 sound chip

Where :

MIX	Sound mixing 0 : Mixing not required 1 : Mixing required	FMIX	Force mixing 0 : Normal sound mixing controlled by BI packet and MIX bit. 1 : Sound services 1 & 2 will be mixed independent of the BI packet information.
IRE	Reset interrupt request 1 : reset IRQ		
IPO	Interrupt polarity 0 : IRQ active low 1 : IRQ active high		
X	(9..0) andY (9..0) Main Sound and Commentary Sound mixing levels. All hex values between 200 and 0 may be used to obtain intermediate values of attenuation.		

NOTE: The attenuators only work when the chip is in Mixing mode.

X (9..0) and Y (9..0) value in hex and the resulting attenuation in dB.

Value	dB	Value	dB	Value	dB
200	0	073	13	01A	26
1C8	1	066	14	017	27
197	2	05B	15	014	28
16A	3	051	16	012	29
143	4	048	17	010	30
120	5	040	18	00E	31
101	6	039	19	00C	32
0E5	7	033	20	00B	33
0CC	8	02E	21	00A	34
0B6	9	029	22	009	35
0A2	10	024	23	008	36
090	11	020	24	000	OFF
081	12	01D	25		

CW0	-	CW59	Control word, CW for descrambling
F0	-	F6	The seven least significant bits of the frame counter, FCNT
NEWFC			New frame count for descrambling sent (see text)
L12		L11	Selection of the sound service in the subframes
X		1	Subframe 1 only
1		0	Subframe 2 only
0		0	Both subframes
NAD			New address indication (see text) Sound Muted when NAD is low.
PA0	-	PA9	Packet address
X			Don't care bits

Table 1 (continued) Details of configured chain for the MV1733 sound chip

PA0	-	PA9	Packet address, 10 bits
CI0	-	CI1	Continuity index, 2 bits
SFRI			Subframe 1 or 2, 1 bit 0 : Subframe 1 1 : Subframe 2
PT0	-	PT7	Packet type byte, 1 byte (BI1, BI2, BC1, BC2)
D0	-	D719	Sound/control bits, 720 bits

Table2. Packet format on PDATA pin

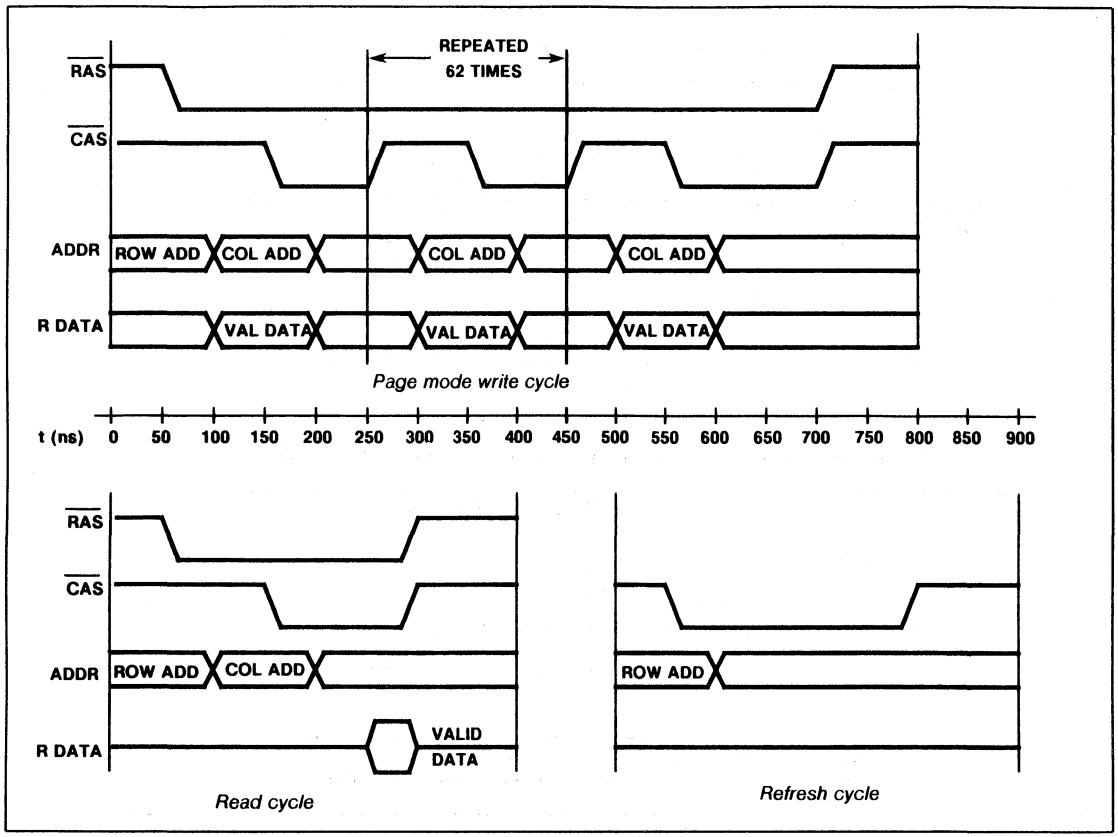


Fig.4 DRAM Signals

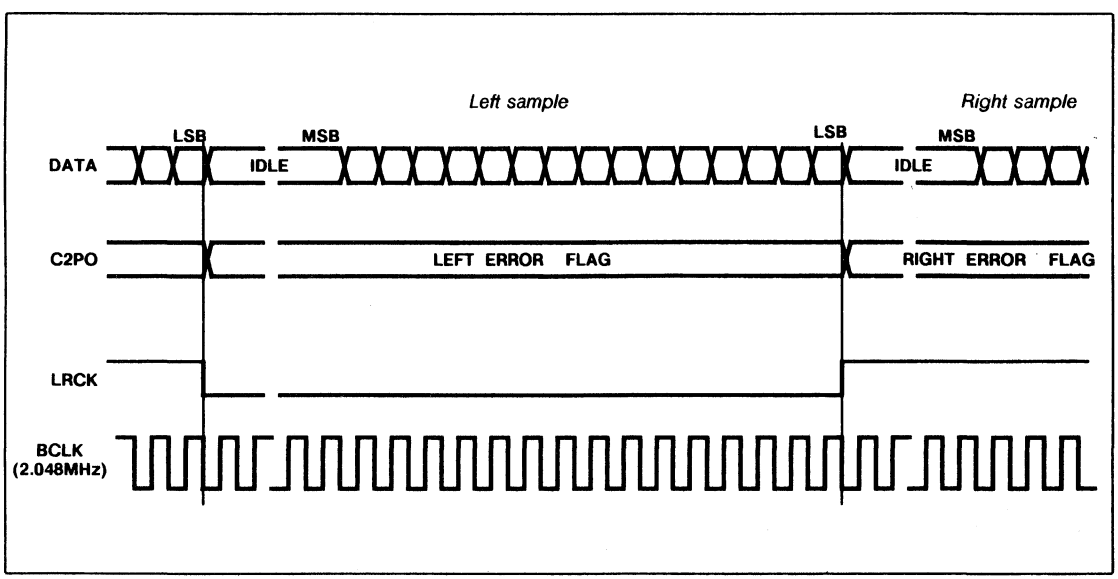


Fig. 5 Sample data output waveforms, SONY format

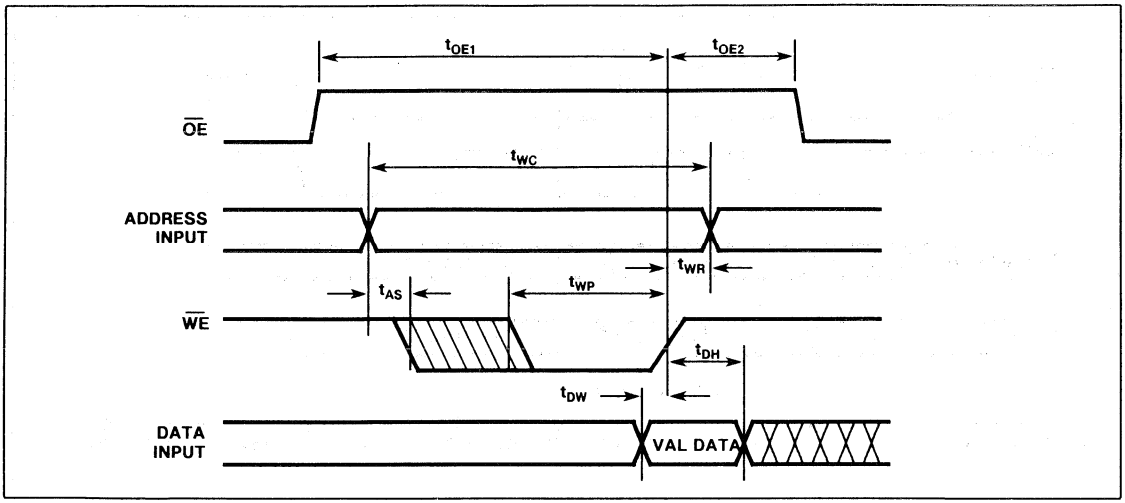


Fig.6 Write cycle $\overline{WE}$ controlled, for SRAM

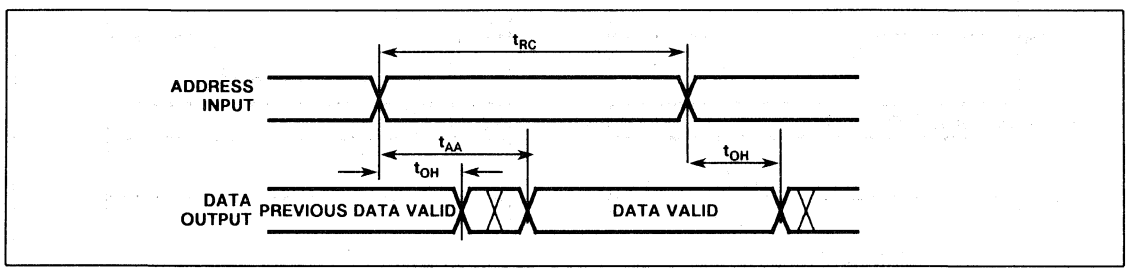


Fig.7 Read cycle (address access), for SRAM

DELAYS ON THE SRAM SIGNALS

Write pulse width	t_{WP}	min 48ns	max 52ns
Address set up time	t_{AS}	min 45ns	
Write recovery time	t_{WR}	min 45ns	
Write cycle time	t_{WC}	min150ns	
Data to write time overlap	t_{DW}	min 45ns	
Data hold from write time	t_{DH}	min 45ns	
Read cycle time	t_{RC}	min 200ns	
Output hold time	t_{OH}	min 0ns	
Address access time	t_{AA}	max 100ns	
$\overline{OE}$ setup time	t_{OE1}	min 295ns	
$\overline{OE}$ hold time	t_{OE2}	min 95ns	

REF. 1.

MAC packet family specifications
EBU No tech 3258-e

ABSOLUTE MAXIMUM RATINGS

(Reference to V_{SS})

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	Tstg	-30	+125	C
Operating Ambient Temp.	Tamb	0	+70	C
Supply Voltage (all supplies)	Vdd	-0.3	+6.5	V
Input Voltage (any input)	Vimax	-0.3	V_{DD} + 0.5	V
Output Voltage (any output)	VOmax	-0.3	V_{DD} + 0.5	V
DC input or output diode current	IIOK		+/-20	mA
Output Current (each output)	Iomax		+/-10	mA
Electrostatic Handling (Mil-STD 883C)	Vstat	-2000	+2000	V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0 °C to + 70°C, V_{DD} = 4.75V to + 5.25V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Low input voltage		V_{SS}		1.2	V	
High input voltage		3.4		V_{DD}	V	
Low output voltage				0.4	V	I_{OL} = 4mA
High output voltage		V_{DD}-0.4			V	I_{OH} = -4mA
Output short circuit current		24		96	mA	V_O = V_{DD}
		-12		-48	mA	V_O = V_{SS}
Clock 1 frequency		1		21	MHz	
Oscillator frequency HIGH		8.192		+ 150ppm	MHz	XC = Low
LOW		8.192		-150ppm	MHz	XC = High
Crystal tolerance		8.192		± 30ppm	MHz	

Section 4

Teletext
TV Signal Generators

MR9735

TELETEXT/VIEWDATA 625-LINE VIDEO GENERATOR

The MR9735 Video Generator chip reads the contents of a Page Store and generates outputs suitable for driving a normal 625-line colour television receiver to display the contents of the page store.

The chip also monitors the composite synchronising signals within the receiver and locks onto the incoming interlaced signals. When no transmission is taking place, the chip generates an interlaced or non-interlaced composite sync. signal which is used to synchronise the receiver.

A full set of colour display facilities as described in the Broadcast Teletext Specification (September 1976) is provided by the device.

The MR9735 is fabricated on the GPS N-channel metal gate process, providing direct TTL interfacing, high speed and good reliability.

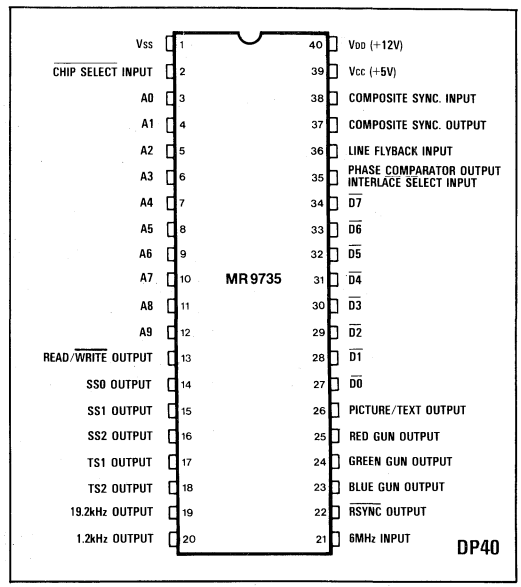


Fig.1 Pin connections - top view

FEATURES

- Interlaced 625 line or non-interlaced 313 line operation
- 24 Row x 40 Character display
- Character Set options available
- On and Off Hours operation
- Half Page Expansion
- Boxed Clock and Header on Teletext
- Can address up to eight Page Stores
- Provides the address information to scan the allocated Page Store
- Provides composite synchronising signals for the receiver for 'Off-Hours' working
- Provides comprehensive set of display facilities

DISPLAY FACILITIES

1. Provides the following display facilities controlled by 'control' characters read from the store i.e. via the TELETEXT/VIEWDATA transmission.

(a) Alpha-numerics/Graphics in seven colour set.

(b) Colour or black backgrounds.

(c) Selected characters can be concealed.

(d) Selected characters can be flashed.

(e) 'Boxed' characters can be inserted into the normal Television Picture. This can be done manually or automatically.

(f) Characters may be either single or double height.

(g) Graphics characters may be contiguous or separated.

(h) Graphics characters may be 'held' during other control characters.

(i) Special graphics for high resolution applications, a dynamically redefinable character set application also available.

2. Provides the following display facilities.

(a) Switch between normal and data video.

(b) Teletext or Viewdata Operation.

(c) Clock time can be boxed into a normal picture (Teletext only).

(d) Display of one half of a page in double height.

(e) Black and white output of data in Mix Mode.

(f) Inhibiting of character rounding and flashing.

(g) Enabling of a cursor.

(h) Inhibit the display until updated.

(i) Reveal 'concealed' characters.

CHARACTER SETS

English	MR9735-002
German	MR9735-003
Swedish/Finnish	MR9735-004
Danish	MR9735-005
Italian	MR9735-006
Others	Contact Factory

PIN FUNCTIONS

Pin Number	Name	Function
1	Vss	This is the negative supply for the chip and is used as a reference for all the electrical parameters.
2	$\overline{\text{Chip Select}}$ Input	The chip can be put in its deselected state by connecting this input to Vcc. The input has an internal pull down to Vss. If connected to Vdd the test mode is selected.
3-12	A0-A9	**These pins are connected to the system Address Bus. They are used for address Input/Output.**
13	Read/$\overline{\text{Write}}$ Output	This output is used to drive the Random Access Memories forming the Page Memory.
14-16	SS0-SS2 Outputs	These binary coded outputs are used to select the required Page Store.
17,18	TS1,TS2 Outputs	These outputs are generated by the Video Generator from the status of the raster scan and are used to indicate this status to other chips within the system.
19,20	19.2kHz and 1.2kHz Outputs	These outputs provide 19.2kHz and 1.2kHz square wave signals which are used by the UAR/T as reception and transmission clocks respectively.
21	6MHz Input	This input is fed from a 6MHz oscillator which is phase locked to the normal transmission for Teletext ON Hours operation. During OFF Hours working a free running crystal oscillator is normally used.
22	$\overline{\text{RSYNC}}$ Output	**This output is an open-drain output and is used to indicate the presence of Teletext lines to the Data Slicer SL9100. The timing of this signal is indicated in Fig. 9.**
23-25	Red, Green and Blue Outputs	These outputs are push-pull outputs which go high to turn on the relevant colour gun for displaying. These outputs are closely matched for propagation delay and rise and fall times.
26	Picture/$\overline{\text{Text}}$ Output	This output may be used by the TV receiver to determine whether to display the normal TV Picture or the generated Text as provided at the Red, Green and Blue outputs. In the mix mode this generates monochrome video. It will then be matched to the gun outputs for propagation delay and rise and fall times.
27-34	$\overline{\text{D0}}$-$\overline{\text{D7}}$ Inputs	The Data Inputs form the communication highway between the Video Generator and the Control Processor and Page Memory.
35	Phase Comparator Output/Interlace Select Input	In on-hours operation the display Line Flyback signal is compared for phase with an internal 64μs period signal derived from the 6MHz display clock. The output is a pulse which produces a voltage for controlling the frequency of a 6MHz display oscillator, thus locking the display to the incoming picture. In off-hours operation this open drain output goes high permanently, and thus can be used as an indication of on-hours/off-hours status. When this output is high the oscillator must run fast and when this output is low the oscillator must run slow. In OFF Hours operation if the Phase Comparator output is held low a 313 line non-interlaced sync. is provided at the Composite Sync. output. If the Phase Comparator output is pulled high connected to Vcc via a 4.7k resistor interlaced sync. will be provided.
36	Line Flyback Input	The Line Flyback input is a signal from the display deflection circuitry which is used for positioning the display on the T.V. screen. Line Flyback pulses are positive. If no Line Flyback is provided in OFF hours mode the display will be positioned so that the start of video is approximately 16μs after the negative edge of line sync.
37	Comp. Sync. Output	This output is an open drain output. In on-hours working or in Picture mode it outputs a regenerated composite sync. signal from the comp. sync. input. In off-hours working it outputs an internally generated composite sync.
38	Comp. Sync. Input	The Composite sync. input monitors the composite sync/video being received and extracts synchronising information and 'on-hours' 'off-hours' information for the Video Generator. This input must be predominantly high for 'off-hours' switching. Sync. pulses are negative.
39	Vcc	This pin is connected to the +5.0V supply.
40	Vdd	This pin is connected to the +10.0V supply.

CHIP DESCRIPTION

The Video Generator Chip contains the logic and control functions to interrogate a selected Page Store and display the contained information at the correct period within the raster scan on a normal TV receiver. The chip also generates the master timing signals TS1 and TS2 which indicate the raster status to the Control processor.
The basic block diagram of the chip is shown in Fig. 4 and major functional blocks are described below.

1. Comp Sync Generator and On Hours Detector

The prime function of this block is to detect negative going sync. signals from the incoming mixed sync. and to synchronise the system with the transmitted signal. When the incoming transmission is turned off, (i.e. goes 'Off-hours'), this is recognised by the detector after at least 300ms of missing sync. pulses. An internally generated Composite Sync signal is then switched to the Composite Sync Out pin. Thus the receiver will continue in lock but synchronised to the Video Generator. Similarly if the normal transmission resumes, the fact that external sync pulses are being received is recognised by the Video Generator and the chip will re-synchronise itself with the incoming transmission. Because the Video Generator is aware of the status of the mixed sync. at all times the chip can detect frame sync., line sync. and even or odd frames. Thus with this information the chip can continuously monitor the current line number. The relevant sections of the line scan are decoded and are indicated externally by the TS1, TS2 time slot outputs. These signals are fully described in Figs.7 and 8, but there are four periods i.e.

(i) Writing to RAM. TS10
This occurs during lines 7 to 22 under external control.

(ii) Reading from RAM. TS00
This occurs under control of the Video Generator chip between lines 48 and 288, and is when the display is active.

(iii) Data Interchange Period. TS11
The interchange of information between Control Processor and Video Generator occurs during this period (lines 23-47).

(iv) Spare TS01
During lines 289–296 the Video Generator does not use the Data Bus.

As the chip is aware of the raster status the chip also starts and stops the address counter/latch combination which is used to scan the relevant Page Memory. The form of the generated sync. pulses are shown in Fig. 5.

2. Character Counter and Address Logic

The address counter is a binary counter which is incremented at the Character Display Rate (1MHz). It can also be loaded from a latch which contains the start address of each character row. Since each character consists of 10 vertical lines of raster scan, the counter is incremented 40 times from a start address and then is reloaded with the same start address ready for the next raster scan of the same forty characters. This occurs nine times. On the last line the counter is incremented an extra once and this new address is stored in the latch. This address being the start address of the next row of forty characters. The above sequence is then repeated.

If displaying only one half of a page with all characters in double height, the Video Generator scans the same forty addresses nineteen times and stores the new address on the twentieth raster scan. If it is in the bottom half of the page, the address counter is initialized to 480.

The display format of 40 characters, each 1μs wide, occurs on a line of 64μs duration thus leaving a border of 12μs at each end of the character row. This address counter is actually started some 4μs before the start of the proper character display thus allowing time for address generation, RAM access time, ROM access time and display processing, these actions being pipelined. Facilities are also provided such that the output address can be reduced by 40 thus allowing accessing of the character in the row above. This is a necessary operation for a 'Double Height' display option which will be described later. This facility is inhibited while displaying one half of a page. The address so produced is presented on the address bus and the required Page Memory is activated by the Store Select Outputs. The address drivers are tristate thus allowing easy bus interface, being active for 40μs starting 3.5–6μs after LFB.

3. Input Latches and Character Read-Only Memory

The data being read from the required Page Memory is placed on the Data Bus and is latched into the Data Bus latches. A total of 450ns is allowed for the RAM read cycle and thus quite slow Random Access memories may be used. Having been latched by the Video Generator chip the seven bit character is used to address the character Read Only Memory. This memory is organised as 96 characters each of 45 dots (5 x 9 array).

4. Data Control Latches (Colour Background Control)

Certain characters indicate to the video generator a change in display status. These characters are contained within columns 0 to 1 of the character set as shown in fig. 7 and may be used to change character colour, background colour, height, etc. These facilities, and the control of them, are fully described in the British Broadcasting Teletext Specification (Sept. 1976) published by the BBC, IBA and BREMA.

5. Output Logic and Drivers

The output logic reads the character ROM into a six bit parallel to serial shift register. This operation occurs at the left-hand side of the character to be displayed, the data in the register is then shifted out at 6MHz (character dot-rate) the data bits selecting between character and background information. This information is used to drive the fast Gun output drivers. These outputs are closely matched for propagation delay and rise and fall time to ensure good legibility.

DATA INTERCHANGE

During the TS11 timeslot the Video Generator can receive information from other devices attached to the system buses. This is normally used by the control chip to update the control and display latches within the Video Generator. The Video Generator is enabled to receive by putting the address 1111XX0XXX on the address highway (active high).

The latches are updated by the following control words, active low signalling, most significant bit is a strobe.

Highway Free	0	0	0	0	0	0	0	0
Control Word 1	1	0	0	0	T	S	s	s
Teletext								
Control Word 2	1	0	0	1	X	C_4	C_6	C_5
Control Word 3	1	0	1	0	C_{10}	C_9	C_8	C_7
Control Word 4	1	0	1	1	C_{14}	C_{13}	C_{12}	C_{11}
Viewdata								
Control Word 2	1	0	0	1	X	F	0	0
Control Word 3	1	0	1	0	b_7	0	b_6	b_5
Control Word 4	1	0	1	1	b_4	b_3	b_2	b_1
Store Select for Display	1	1	0	0	SP	D	d	d
Key Data	1	1	0	1	*	P	*	*
Other Facilities	1	1	1	0	X	BH	M	BC

The Control bits are as follows:-

T	TELETEXT MODE i.e. NOT VIEWDATA
Sss	Identification of Store being written to
Ddd	Identification of Store being displayed from

(a) Teletext

C_4	Erases rows 1-23 of Store defined by Sss and resets Reveal if Sss = Ddd
C_5	Newsflash
C_6	Subtitle
C_7	Suppress Header
C_8	Update Indicator
C_9	No action
C_{10}	Inhibit display
C_{11}	No action
C_{12}-C_{14}	No action (may be programmed to enable and disable the chip)

(b) Viewdata

b_7-b_1	Cursor Control Bits
001 0001	Cursor ON } The two Control Words that make up these codes must be transmitted in numerical order in the same TS11 timeslot
001 0100	Cursor OFF }
F	Form feed or first appearance, Erases store defined by Sss, resets Reveal if Sss = Ddd
SP	Sets Picture/Text to picture (for initialization)
P	P Key presed. Resets Reveal, Half Page Expansion, Newsflash/Subtitle (Auto Box), Suppress header, Inhibit display, Update.
M	Mix Mode
BC	Box Clock (Teletext only)
BH	Box Header (Teletext only)
	For M, BC and BH, the latches are set and reset by the appropriate bit
* * *	These are coded as follows:-
001	Picture/Text Key pressed
010	Reveal/Conceal Key pressed
011	½ Page Key pressed (Cycles Full, Top, Bottom, Full etc).
100	Update/Clear Key pressed
	For 001, 010, 011 and 100, the latches are toggled by the appropriate code
101	Rounding and Flashing OFF (Reset by P Key or new viewdata page)
111	Hold (not used by MR9735)

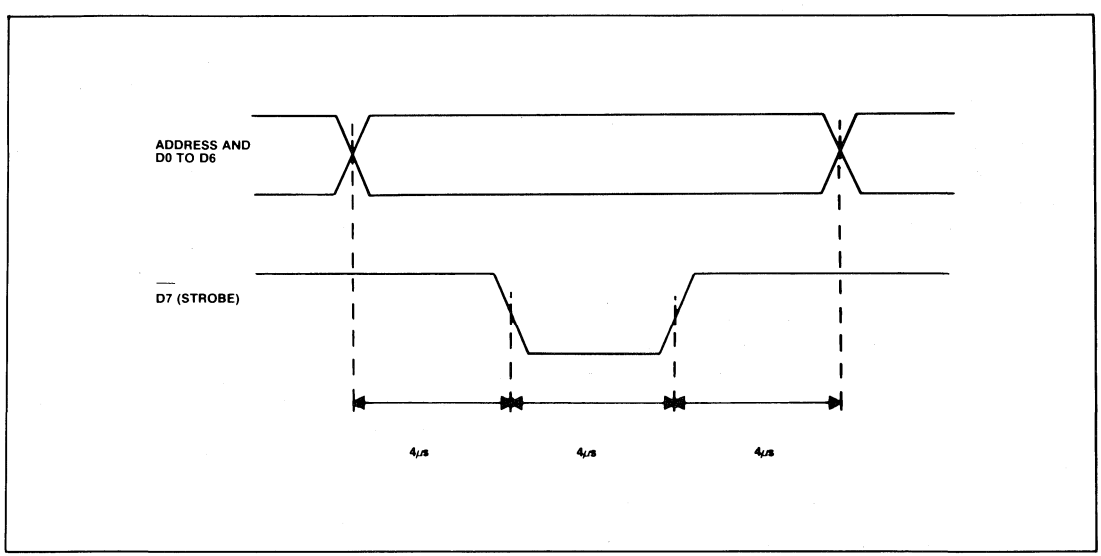


Fig. 2 Typical timing diagram for input data strobing of control data using TS11

DISPLAY OPTIONS

Logic is contained on the Video Generator chip to process the Display Modes as described in the Broadcast Teletext Specification. These facilities are outlined below. Some extra facilities are also included.

1. **Character Set**

   The chip can display 96 Alphanumerics characters and 64 Graphics shapes which may be either contiguous or separated. The alphanumeric format is determined by a 4320 bit Read Only Memory organised as:

   96 (characters) x 5 (dots) x 9 (lines) = 4320

   This can be programmed for different character fonts.

   The graphics shapes are determined directly from the bits of the character code (Fig.10).

2. **Display and Background Colour**

   The characters and the background can be displayed in one of seven colours. In addition the background may be black. This information is stored in two sets of three latches representing character and background colours.

3. **Conceal and Flash**

   Selected characters can be concealed and optionally revealed by the viewer. Selected characters can be flashed on command. The flashing is controlled by an on-chip flash oscillator. During the flash period or when concealed, only background information is displayed. The flash rate is 1.56Hz.

4. **Boxing**

   Text or graphics characters can be boxed into a normal video picture. While in Picture mode boxing is automatic if Newsflash or Sub-title (and Sss = Ddd). Other boxed characters may be manually revealed by Reveal command.

5. **Double Height**

   Double height characters are characters contained between the control characters "Double Height" and "Normal Height" (or end of line). When a "Double Height" control character is read from the RAM only the top half of the subsequent character(s) are displayed during the 10 raster scans. During the next 10 scan lines, 40 is subtracted from the addresses being output on A0–A9 so the same 40 addresses are read from another 10 times. Characters which are not double height are displayed as the background colour and the bottom(s) of the double height character(s) is (are) displayed.

6. **Hold Graphics**

   When this latch is set, any subsequent control characters (except change Double/Normal Height or Change Alpha/Graphics) are displayed as the last graphics character.

7. **Special Graphics**

   While in Graphics Mode the Special Graphics command will give a special high resolution facility. In this mode there is a one to one correspondence between data bits b_1, b_2, b_3, b_4, b_5, b_7 and the six dots in each horizontal line of a character. This gives a possible graphics resolution of 6 x 20 for each character in interlace mode (or 6 x 10 if not interlaced).

8. **Box Clock**

   When box clock is selected in picture mode and teletext the last eight characters of the page header are boxed in double height. To ensure that the "live" clock is displayed the store address is temporarily switched to that defined by Sss. This function is cleared in text mode.

9. **Box Header**

   When box header is selected in picture mode and teletext the page header is boxed in double height (not if bottom half of page selected).

10. **Half-page Operation**

    This allows either the top or bottom half of a normal Teletext/Viewdata page to be displayed over the whole screen, with each character in double height. This makes the display easier to read from a distance. Double height characters are ignored in this mode.

11. **Monochrome Output/Mix Mode**

    In normal operation the Picture/$\overline{\text{Text}}$ Output is used to blank the normal picture information for boxing or displaying a page of text.

    In the mix mode this outputs Monochrome text information which is matched to the Gun Output signals in delay and drive. This can be used to superimpose text onto a picture by "cutting away" the picture below text data or as an output for Monochrome displays or printers. In this mode coloured backgrounds are suppressed for viewing clarity. The output is at a low level to display a character.

12. **Character Rounding**

    Characters are normally rounded by adding half dots to smooth diagonals. For normal height characters the extra TV lines made available by interlace are utilised for this and so if in non-interlace mode single height characters cannot be rounded.

    Character rounding can be inhibited totally by a signal from Control and in this mode, intended specifically for printers, flashing is also suppressed. Reset by P key or new Viewdata page.

13. **Cursor**

    The cursor is stored as the 8th bit of the appropriate character in the Data Store. When switched on it is displayed as a bar on the bottom line of the character rectangle flashing between foreground colour and black in anti-phase to normal flashing characters.

14. Non Interlaced Operation

When interlaced composite sync. is input to the chip it operates in normal Interlaced Mode and regenerates Interlaced composite sync.

If there is no incoming sync. the chip switches to the OFF hours mode.

If the Phase Comparator output is pulled high, e.g. 4k7 to Vcc, Interlaced Sync. is output. If the Phase Comparator output is held low Non Interlaced Sync. is output and character rounding for single height characters is inhibited.

SIGNAL DETECTION CRITERIA (For On Hours Operation)

The Video Generator detection circuitry for incoming sync. signals is designed to prevent mis-operation in the presence of noise. The criteria for detection is defined below.

1. Line Sync

The Comp. Video Input must be negative for greater than 3μs.

2. Frame Sync.

The Comp. Video Input must be negative for greater than 12μs and at least 310 lines (Line Flyback pulses) must have occurred since the previous Frame Sync detection.

3. Odd Frame Detection

Odd Frame Detection occurs when a Line Flyback pulse falls in a window 12–39μs after Frame Sync Detection. This is used to lock the line counter.

4. On-Hours/Off-Hours Detection

The incoming line flyback and line sync pulses are compared to determine whether a valid transmission is being received. Lack of coincidences/frame are accumulated and if more than 16/Frame occur for a period 350–1000ms the logic deems that a valid transmission is not being received and the chip switches 'OFF Hours''. If however, less than eight occur in any two successive ½ frames, the logic deems that a valid Composite Sync is being received and the system goes 'ON Hours'.

For the chip to be able to look for synchronism the following phase relationship between Line Flyback and Comp. Sync must be satisfied.

(a) Earliest back edge of LFB is 2μs after leading edge of line sync.

(b) Latest leading edge of LFB is 2μs after leading edge of line sync.

(c) Latest back edge of LFB is 12μs after leading edge of line sync.

The minimum length of the LFB pulse is 8μs.

5. 6MHz Display Oscillator

The 6MHz display oscillator must run fast in the OFF Hours mode but not so fast that the ON/OFF Hours detection criteria cannot be satisfied. This sets a maximum offset of +1.5kHz, the minimum offset is set by lock time criteria and would typically be +0.5kHz.

The frequency range of the oscillator must extend below the 6.0MHz nominal frequency. The minimum frequency should be at least −0.5kHz but can be as low as convenient.

COMPOSITE SYNC INPUT

On chip D.C. restore is provided which allows simple interfacing to the television, either composite sync. signals or video being acceptable.

As the Composite Sync/Video signal from the television may not be referenced to the system earth it is a.c. coupled to the chip.

A typical Interface Circuit is shown in Fig.3.

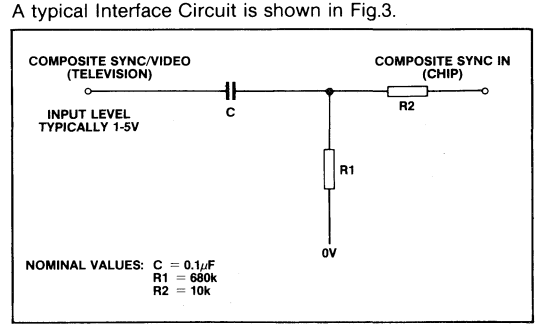


Fig.3 Typical interface circuit

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to Vss . . . . . –0.3 to +15V
Storage temperature range. . . . . –55°C to +150°C

*Exceeding these ratings could cause permanent damage
Functional operation is not guaranteed under these conditions
Operating ranges are specified below

Standard Conditions (unless otherwise indicated)

Vss = 0V (Substrate voltage)
Vcc = +5V ± 5%
Vdd = +10V ± 10%
Operating Temperature (Ta) = 0°C to +70°C
Clock Frequency 6.0MHz

Characteristic	Min	Typ**	Max	Units	Conditions
INPUTS					
Chip Select					
Input Logic High	2.4		Vcc	V	
Input Logic Low	Vss		0.8	V	
Input Current	10	25	100	μA	Vin = 5V
Comp. Sync.					
Input Logic High	1.0		Vcc	V	
Input Logic Low	–0.3		0.05	V	See Note 1
Input Capacitance			15	pF	Vin = 0V
Source Current		50		μA	Vin = 0V
6MHz					
Input Logic High	2.8		Vdd	V	
Input Logic Low	Vss		0.4	V	
Input Capacitance			25	pF	Vin = 0V
Mark to Space Ratio	40:60		60:40		
Frequency	1.0		6.5	MHz	
Input Leakage			10	μA	Vin = 10V
All Other Inputs					
Input Logic High	2.4		Vdd	V	
Input Logic Low	Vss		0.8	V	
Input Capacitance			15	pF	Vin = 0V
Input Leakage			10	μA	Vin = 10V
OUTPUTS					
Addresses, Read/$\overline{\text{Write}}$					
Store Select (Tri-State) (Note 2)					
Logic High Output	2.4		Vcc	V	Ioh = -300μA
Logic Low Output	Vss	0.2	0.5	V	Iol = 3.0mA
Capacitance			15	pF	Vin = 0V
T rise T fall			200	ns	C load = 200pF
Leakage (Disabled)			10	μA	Vo = 0V, 5V
Time Slots (TS1, TS2)					
(Push-Pull)					
Logic High Output	2.4		Vcc	V	Ioh = -300μA
Logic Low Output	Vss	0.2	0.5	V	Iol = 3.0mA
T rise T fall			200	ns	C load = 200pF
Comp. Sync (Open Drain)					
Logic Low Output	Vss		0.5	V	Iol = 1.6mA
Logic High Leakage			10	μA	Vo = 10V
Capacitance			20	pF	V0 = 0V
Delay from Comp. Sync In.			1	μs	ON Hours only

Characteristic	Min	Typ**	Max	Units	Conditions
$\overline{\text{RSYNC}}$ (Open Drain)					
Logic Low Output	Vss		0.5	V	Iol = 4.0mA
Logic High Leakage			10	μA	Vo = 5V
Capacitance			15	pF	Vo = 0V
Phase Comparator (Open Drain)					
Logic Low Output	Vss		0.5	V	Iol = 4.0 mA
Logic High Leakage			10	μA	Vo = 10V
Capacitance			15	pF	Vo = 0V
R.G.B. Outputs Picture/Text Output (Tristate) (Note 2)					
Logic High Output	Vcc−1		Vcc	V	I source = 1mA
Logic Low Output	Vss		1	V	I sink. = 2mA
Capacitance			20	pF	Vin = 0V
T rise T fall (10%–90%)			30	ns	CL = 30pF
Differential T rise T fall			30	ns	CL = 30pF Note 3
19.2kHz, 1.2kHz Outputs					
Logic High Output	2.4		Vcc	V	Ioh = -30μA
Logic Low Output	Vss	0.2	0.5	V	Iol = 300μA
T rise T fall			1	μs	C load = 100pF
POWER					
Vcc Supply		25	40	mA	Vcc = 5V
Vdd Supply		40	66	mA	Vdd = 10V

Note 1: Voltages below −0.3 volts should be current limited to 1mA.

Note 2: All tristated when $\overline{\text{Chip Select}}$ = Vcc. R.G.B. outputs also tristated when displaying picture and not mixed.

Note 3: Picture/$\overline{\text{Text}}$ matched in mix mode only.

** Typical values are at +25°C and nominal voltages.

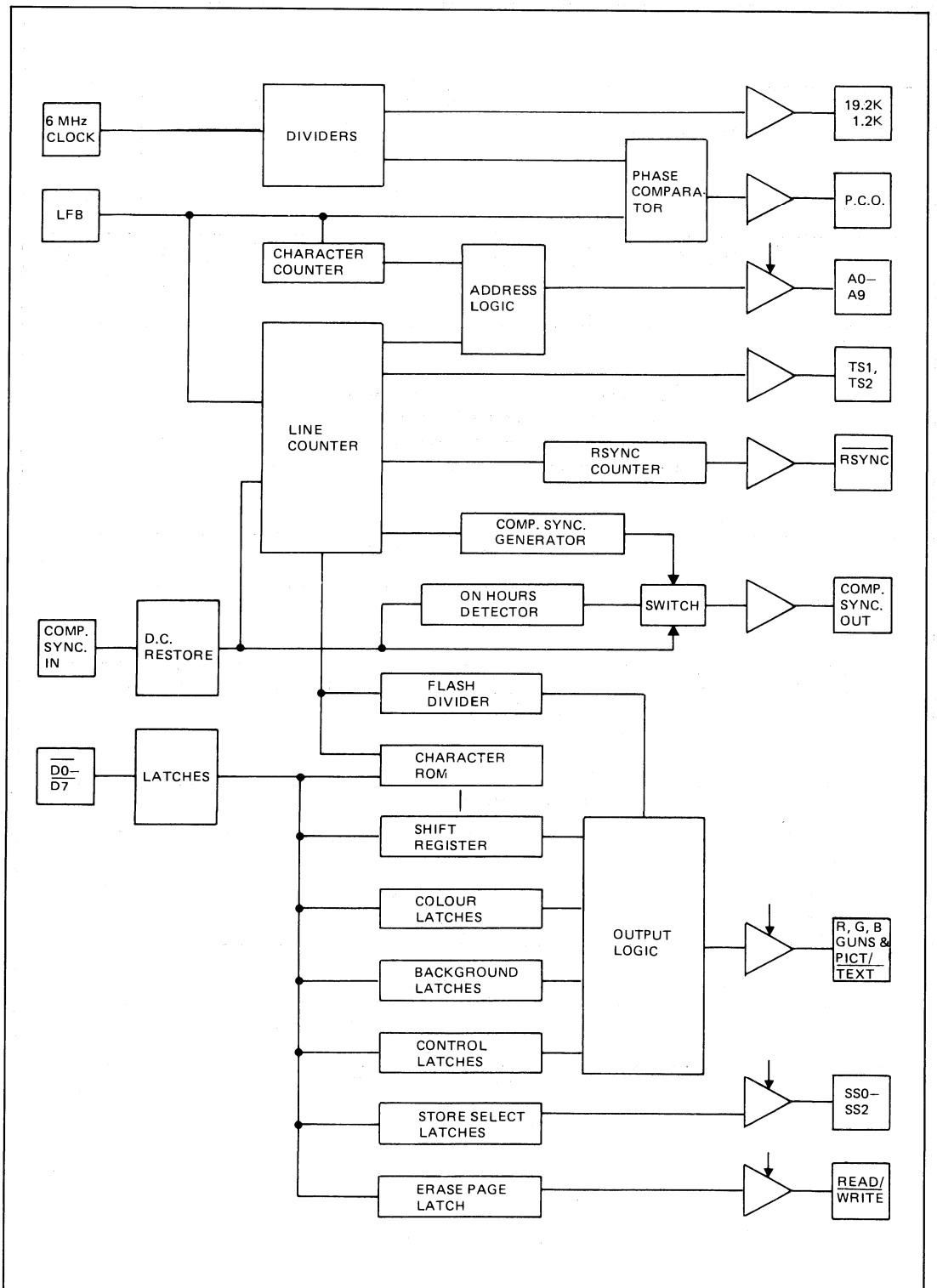


Fig.4 Block diagram

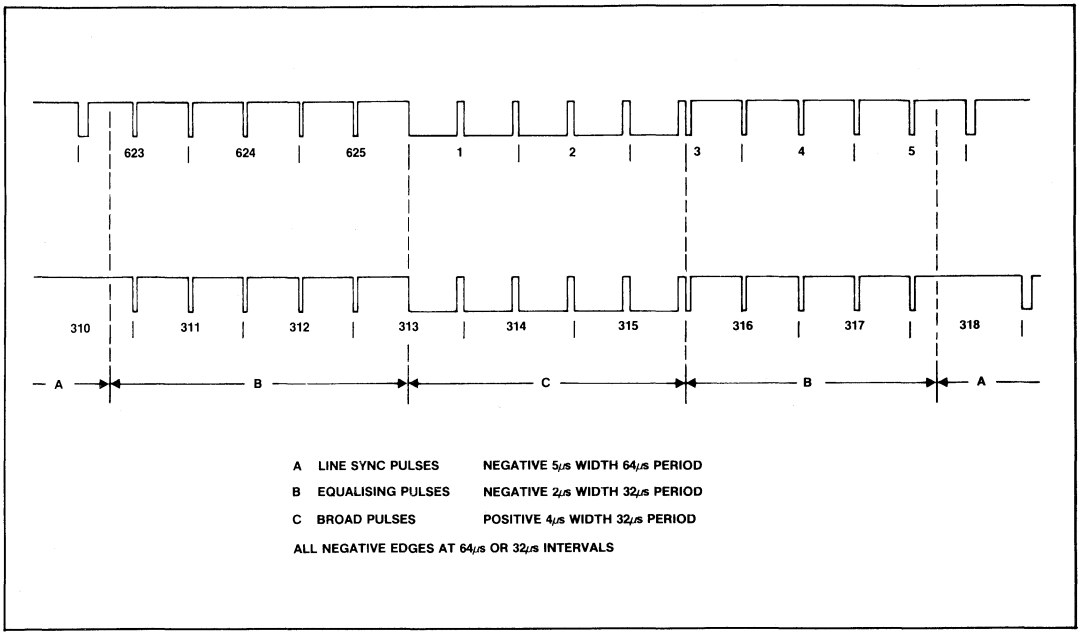


Fig.5 Interlaced composite sync

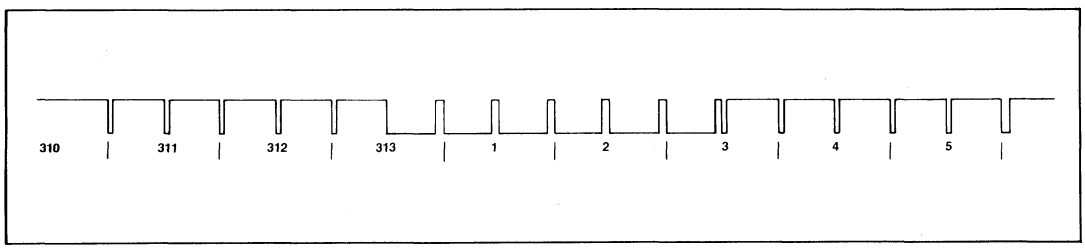


Fig.6 Non interlaced composite sync output

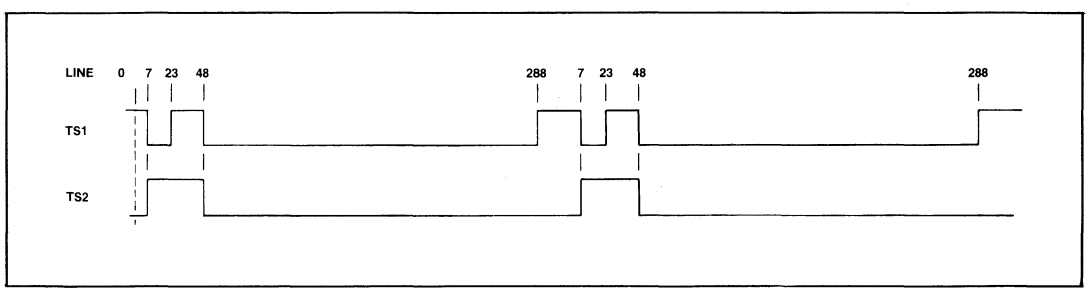


Fig.7 Time slot outputs non interlaced

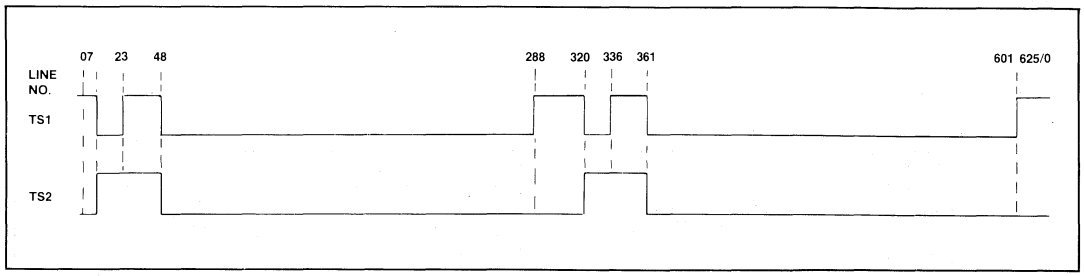


Fig.8 Time slot outputs (interlaced)

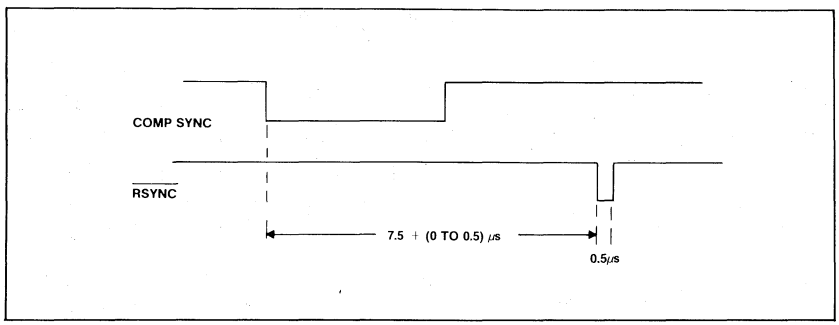


Fig.9 RSYNC timing

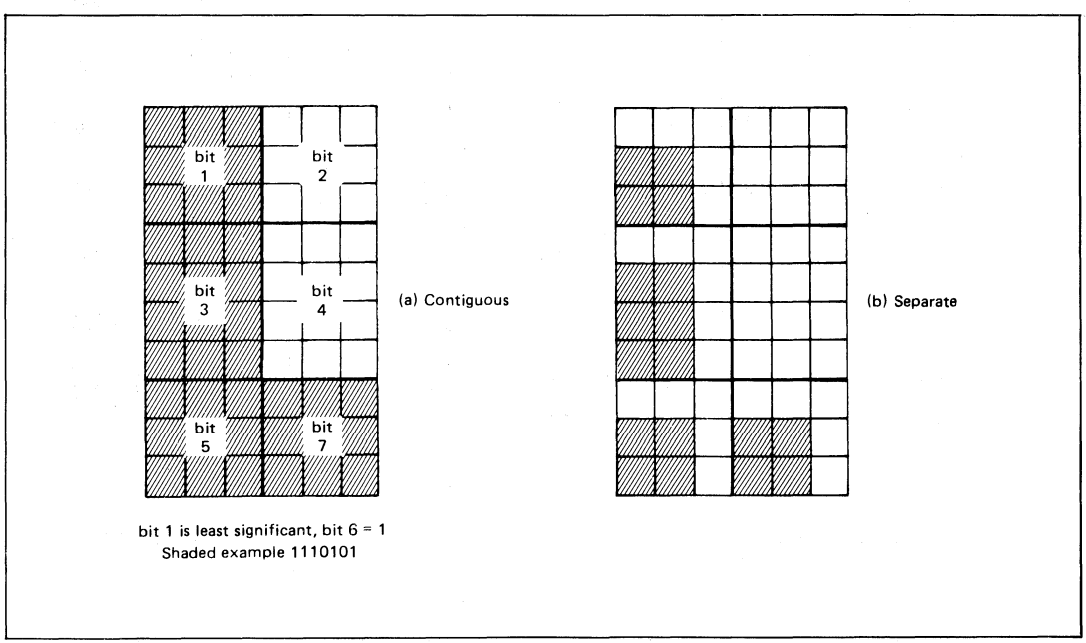


Fig.10 Graphics format

b7 b6 b5 / Bits b4 b3 b2 b1 / Col Row	0_0	0_1	0_2		0_3		1_0	1_1	1_2		1_3	
	0	1	2	2a	3	3a	4	5	6	6a	7	7a
0 0 0 0 0	NUL①	DLE①			O		@	P	—		p	
0 0 0 1 1	Alpha^n Red	Graphics Red	!		1		A	Q	a		q	
0 0 1 0 2	Alpha^n Green	Graphics Green	"		2		B	R	b		r	
0 0 1 1 3	Alpha^n Yellow	Graphics Yellow	£		3		C	S	c		s	
0 1 0 0 4	Alpha^n Blue	Graphics Blue	$		4		D	T	d		t	
0 1 0 1 5	Alpha^n Magenta	Graphics Magenta	%		5		E	U	e		u	
0 1 1 0 6	Alpha^n Cyan	Graphics Cyan	&		6		F	V	f		v	
0 1 1 1 7	Alpha^{n}② White	Graphics White	'		7		G	W	g		w	
1 0 0 0 8	Flash	Conceal Display	(		8		H	X	h		x	
1 0 0 1 9	Steady②	Contiguous② Graphics	)		9		I	Y	i		y	
1 0 1 0 10	End Box②	Separated Graphics	*		:		J	Z	j		z	
1 0 1 1 11	Start Box	ESC①	+		;		K	←	k		¼	
1 1 0 0 12	Normal② Height	Black② Background	,		<		L	½	l		II	
1 1 0 1 13	Double Height	New Background	-		=		M	→	m		¾	
1 1 1 0 14	Special Graphics	Hold Graphics	.		>		N	↑	n		÷	
1 1 1 1 15	Normal② Graphics	Release② Graphics	/		?		O	#	o			

① These control characters are reserved for compatibility with other data codes

② These control characters are presumed before each row begins

Codes may be referred to by their column and row e.g. 2/5 refers to %

Character rectangle

Black represents display colour

White represents background

Fig.11 Teletext character codes (002 character set)

2066-2.1

MV1815

SINGLE CHIP TELETEXT DECODER FOR 625 LINE OPERATION

The MV1815 is an advanced CMOS single chip Teletext decoder for 625 line World System Teletext. The MV1815 has an on-chip data slicer circuit, dual page acquisition circuits, and direct memory addressing, which allow a low cost Teletext decoder to be built with a minimum number of additional components.

FEATURES

- On-Chip Data Slicing.
- Up to 254 Display Pages Stored, using Low Cost 150ns DRAMs.
- Low External Component Count.
- I²C Bus for Low Cost Interfacing.
- Multi-language Capability for Fourteen European Languages.
- Special Parity Inhibit Feature for TOP 8-bit Data.
- Non-display Packets Stored for Linked Page Operation, Video Programming, etc.
- High Resolution Characters Typically 12 Dots Wide on a 15 by 10 Matrix.
- Accepts all Non-display Packets.
- On-chip Video Switch.
- Advanced CMOS Technology gives Low Power Dissipation and High Reliability.

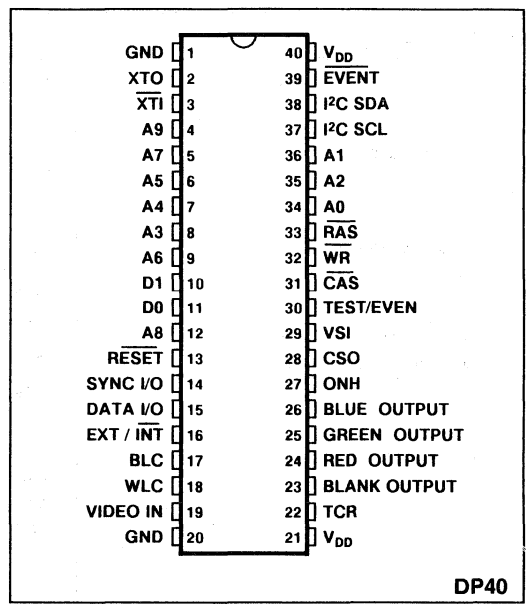


Fig.1 Pin connections - top view

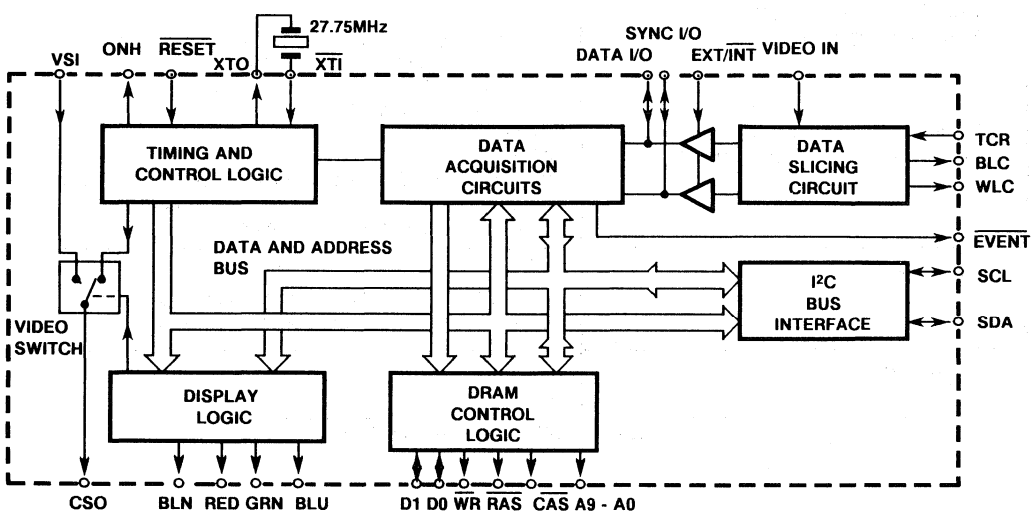


Fig.2. MV1815 block diagram

<table>
<tr><th>Section</th><th>Specification</th></tr>
<tr><td>Data Acquisition Logic
Line standard
Teletext data rate
Data line content
TV lines used VBI
TV lines used full field
Packets accepted
Page numbers
Page subcodes</td><td>
625 Lines 50 Fields / second.
6.9375 Mbits / sec ±25ppm.
360 bits as 45 bytes of 8 bits each.
Lines 6 to 22 and 318 to 335.
All TV Lines
X/0 to X/25, X/26, X/27,X/28, X/29, 8/30 (all formats), X/31
000 to 7FF
0000 to 3F7F</td></tr>
<tr><td>Display Logic
Characters per row
Teletext rows displayed

TV lines used

Character definition
Character sets

Spacing control characters
Data boxing into picture

Displayable page stores

Display options</td><td>
40, occupying 43.24µs of the 52µs display time
0 to 23 with 24 and 25 software programmable

<table><tr><th rowspan="2">Rows displayed</th><th colspan="2">TV lines</th></tr><tr><th>Start</th><th>Finish</th></tr><tr><td>24</td><td>48</td><td>287</td></tr><tr><td>25 or 26</td><td>38</td><td>297</td></tr></table>
15 x 10 dot matrix
English, German, Swedish, Italian, French, Spanish,
Czechoslovakian, Polish, Romanian, Hungarian, Turkish
Danish, Serbo-Croat, ASCII.
Standard Level One Range
Page Number - Row 0 characters 1 to 8
Page Header - Row 0 characters 9 to 32
Clock Time - Row 0 characters 33 to 40
Rows 24 and 25
Up to 254 pages, each of 1Kbytes, depending on the size of the
DRAM being used
Mix of text foreground and picture background
Three part magnify - display rows 0 to 11 double height
rows 6 to 17 double height
rows 12 to 23 double height
Boxing of Newsflash and Subtitles into picture
Boxing of picture into text</td></tr>
<tr><td>Dynamic RAM Control Logic
Memory configuration

Maximum access time (t_{RAC})
Refresh period for complete memory</td><td>
All sizes: Page or nibble mode types
254 pages - 2 off 1M x 1 or 1 off 1M x 4
62 pages - 2 off 256K x 1 or1 off 256K x 4
14 pages - 2 off 64K x 1 or 1 off 64K x 4
150ns
2·048ms.
Refresh occurs during the line flyback period. Contents of
any memory location may be accessed by the
microprocessor via the I²C Bus interface.</td></tr>
<tr><td>I²C Bus Interface</td><td>
Standard implementation of a slave transmitter / receiver
Control of the MV1815 is via 32 on - chip registers.</td></tr>
<tr><td>I²C Bus Address</td><td>
0010 001 R/$\overline{W}$</td></tr>
</table>

Table 1. MV1815 system specification

PIN DESCRIPTION

Symbol	Pin No	Pin Name and Description
GND	1,20	Ground, both pins must be connected
XTO	2	Crystal out 27.75MHz fundamental crystal with an on-chip 1MΩ bias resistor to $\overline{XTI}$
$\overline{XTI}$	3	Crystal input
A9, A7,A5,A4,A3, A6,A8,A0,A2,A1	4-9 12,34,35,36	DRAM address outputs
D1,D0	10,11	DRAM data lines. Internal 100kΩ pull-up resistors are included.
$\overline{RESET}$	13	Active low reset input. Includes 100kΩ pull-up resistor.
SYNC I/O	14	Sliced sync input /output.
DATA I/O	15	Teletext data input /output.
EXT/$\overline{INT}$	16	Control pin for SYNC and DATA I/O. Includes 100kΩ pull-down resistor. When low or not connected internal SYNC and DATA are used, pins 14 &15 are outputs. When high supply SYNC and DATA from an external source, pins 14 & 15 are input.
BLC	17	Black level capacitor.
WLC	18	White level capacitor.
VIDEO IN	19	Input for composite video signal with negative going SYNCs.
VDD	21,40	+5V Supply. Both pins must be connected.
TCR	22	Time constant resistor controlling discharge rate of black and white level capacitor voltages.
BLANK	23	Blanking output, high power push-pull driver.
RED	24	Red output, high power push-pull tri-state driver.
GREEN	25	Green output, high power push-pull tri-state driver.
BLUE	26	Blue output, high power push-pull tri-state driver.
ONH	27	On hours indicator. When high CSO is locked to Video In. When low CSO is not locked.
CSO	28	Generated composite sync output during text, video input is switched through to CSO during modes that contain picture content. See Fig. 6.
VSI	29	Video switch input.
TEST/EVEN	30	Test input is used for factory testing. EVEN output is enabled by bits IOE and EOE in SYNCSW register. If EVEN output is not used, the pin should be left open-circuit. A 100kΩ pull-down resistor is included.
$\overline{CAS}$	31	DRAM column address strobe.
$\overline{WR}$	32	DRAM read / $\overline{write}$ signal.
$\overline{RAS}$	33	DRAM row address strobe.
I²C SCL	37	I²C bus serial clock.
I²C SDA	38	I²C bus bi-directional data port.
$\overline{EVENT}$	39	Active low open drain output interrupt signal to microprocessor.

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency:
27.750000MHz. AT cut.

Tolerance at 20°C ±20ppm.
Tolerance at -10°C to 60°C ± 50ppm.
Tolerance overall ±100ppm.
Nominal load capacitance 20pF
Equivalent series resistance < 20Ω

A variable capacitor is provided internally on pin $\overline{XTI}$ and controlled by a phase locked loop to provide exact trimming of the frequency. This will provide compensation for temperature variation and crystal ageing.

Address		Register	Bit position								R/W	Reset
Dec	Hex	name	7	6	5	4	3	2	1	0		state Hex
		RADD	A17	A16	IAI	RA4	RA3	RA2	RA1	RA0	W	00
0	0	ACONA	ACQ	MGC	PBC	PAC	SDC	SCC	SBC	SAC	W	F0
1	1	STORA	STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0	W	02
2	2	PGS1A	SCS3	SCS2	SCS1	SCS0	SAS3	SAS2	SAS1	SAS0	W	00
3	3	PGS2A	MS2	MS1	MS0	SDS1	SDS0	SBS2	SBS1	SBS0	W	20
4	4	PGS3A	PBS3	PBS2	PBS1	PBS0	PAS3	PAS2	PAS1	PAS0	W	00
5	5	ACONB	HLD (bar)	MGC	PBC	PAC	SDC	SCC	SBC	SAC	W	F0
6	6	STORB	STB7	STB6	STB5	STB4	STB3	STB2	STB1	STB0	W	03
7	7	PGS1B	SCS3	SCS2	SCS1	SCS0	SAS3	SAS2	SAS1	SAS0	W	00
8	8	PGS2B	MS2	MS1	MS0	SDS1	SDS0	SBS2	SBS1	SBS0	W	00
9	9	PGS3B	PBS3	PBS2	PBS1	PBS0	PAS3	PAS2	PAS1	PAS0	W	88
10	A	RECON	WI0	WI24	WI25	PIN B	PIN A	FF	CDB	CDA	W	00
11	B	DISCON1	INV	RLH	DSB	CLS	CUR	BLC	LS3	UDI	W	00
12	C	DISCON2	LS0	LS1	LS2	MGS	IHD	SPH	BX1	BX0	W	00
13	D	DISCON3	TXT	MIX	INT	REV	UDK	SPOS	ST2	ST1	W	00
14	E	DISCON4	BXP	BXH	BXT	BXS	DHT	DHB	SG2	SG1	W	00
15	F	HADD	A15	A14	A13	A12	A11	A10	A9	A8	W	00
16	10	LADD	A7	A6	A5	A4	A3	A2	A1	A0	W	00
17	11	WDATA	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	W	00
19	13	SCROLL	WI29	MV	CRL	SRA4	SRA3	SRA2	SRA1	SRA0	W	00
20	14	SYNCSW	ESS	-	-	-	IOE	EOE	SEN	SVS	W	00
0	0	EVENTA	NPR	VHR	830A	X/29	X/28	X/27	X/26	C8	R	-
1	1	EVENTB	NPR	VHR	830B	X/29	X/28	X/27	X/26	C8	R	-
2	2	CBITSA	C14	C13	C12	C11	C10	C7	C6	C5	R	-
3	3	PGR1A	SCR3	SCR2	SCR1	SCR0	SAR3	SAR2	SAR1	SAR0	R	-
4	4	PGR2A	MR2	MR1	MR0	SDR1	SDR0	SBR2	SBR1	SBR0	R	-
5	5	PGR3A	PBR3	PBR2	PBR1	PBR0	PAR3	PAR2	PAR1	PAR0	R	-
6	6	CBITSB	C14	C13	C12	C11	C10	C7	C6	C5	R	-
7	7	PGR1B	SCR3	SCR2	SCR1	SCR0	SAR3	SAR2	SAR1	SAR0	R	-
8	8	PGR2B	MR2	MR1	MR0	SDR1	SDR0	SBR2	SBR1	SBR0	R	-
9	9	PGR3B	PBR3	PBR2	PBR1	PBR0	PAR3	PAR2	PAR1	PAR0	R	-
10	A	HAMMC	HC7	HC6	HC5	HC4	HC3	HC2	HC1	HC0	R	FF
17	11	RDATA	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	R	-

Table 2 MV1815 register details

NOTE.
Write register addresses 18 and 21-31 (12 and 15-1F HEX) are reserved for future development and should not be used.

WRITE REGISTERS

RADD (W)

A16 / A17	Memory quadrant select.
IAI	Inhibit auto increment..
RA$	Register address ($ = 0 to 4).

ACON A/B (W 0 & 5)

ACQ	Acquisition on.
MGC	Magazine compare.
PAC	Page units compare.
PBC	Page tens compare.
SAC	Page subcode compare digit A.
SBC	Page subcode compare digit B.
SCC	Page subcode compare digit C.
SDC	Page subcode compare digit D.
HLD(bar)	Not hold display acquisition circuit.

STOR A/B (W 1 & 6)

STA$	Store number for acquisition A ($ = 0 to 7).
STB$	Store number for acquisition B ($ = 0 to 7).

PGS /1 /2 /3 A/B (W 2,3,4 & 7,8,9)

SAS$	Sub-Code digit A ($ = 0 to 3) select.
SBS$	Sub-Code digit B ($ = 0 to 2) select.
SCS$	Sub-Code digit C ($ = 0 to 3) select.
SDS$	Sub-Code digit D ($ = 0 or 1) select.
PAS$	Page number (units) ($ = 0 to 3) select.
PBS$	Page number (tens) ($ = 0 to 3) select.
MS$	Magazine number ($ = 0 to 2) select.

RECON (W 10)

WI0	Write inhibit of packet 0.
WI24	Write inhibit of packet 24.
WI25	Write inhibit of packet 25.
PIN B	Parity check inhibit acquisition circuit B.
PIN A	Parity check inhibit acquisition circuit A.
FF	Full field Teletext.
CDA	Clear store disable acquisition circuit A.
CDB	Clear store disable acquisition circuit B.

DISCON1 (W 11)

INV	Invert display.
RLH	Roll headers.
DSB	Display acquisition circuit B (A if zero).
CLS	Clear current display store.
CUR	Cursor enable.
BLC	Block cursor.
LS3	Language group select .
UDI	Display update indicator.

DISCON2 (W 12)

LS$	Language select ($ = 0 to 2).
MGS	Magazine serial.
IHD	Inhibit display, rows 2 to 26 disabled.
SPH	Suppress header.
BX$	Box control bits ($ = 0 or 1).

DISCON3 (W 13)

TXT	Text / not picture.
MIX	Mix text and picture.
INT	Display text in interlace mode (see Figure 6).
REV	Reveal hidden text.
UDK	Update key, rows 1 to 26 disabled.
SPOS	Status line position.

WRITE REGISTERS

DISCON3 (cont)

ST2	Display Status line 2 (row 26).
ST1	Display Status line 1 (row 25).

DISCON4 (W 14)

BXP	Box page number.
BXH	Box header.
BXT	Box time.
BXS	Box status rows.
DHT	Double height top half.
DHB	Double height bottom half.
SG$	Separated graphics control bits ($ = 0 or 1).

HADD and **LADD** (W 15 & 16)

A$	Memory address ($ = 0 to 15).

WDATA (W 17)

WD$	Data to be written to memory($ = 0 to 7).

SCROLL (W 19)

WI29	Write inhibit of packet 29
MV	Majority vote on framing code
CRL	Cursor lock at last HADD. LADD setting
SRA$	Scroll display row up ($ = 0 to 23 only)

SYNCSW (W 20)

ESS	External sync source
IOE	Interlace output enable
EOE	EVEN output enable
SEN	Select enable - SVS bit
SVS	Select VSI as sync source

READ REGISTERS

EVENT A/B (R 0 & 1)

NPR	New page received.
VHR	Valid header received.
830$	Packet 30 received acquisition $ ($ = A or B).
X/29	Packet 29 received.
X/28	Packet 28 received.
X/27	Packet 27 received.
X/26	Packet 26 received.
C8	Update Indicator.

CBITS A/B (R 2 & 6)

C14	Language select bit.
C13	Language select bit.
C12	Language select bit.
C11	Magazine serial.
C10	Inhibit display.
C7	Suppress header.
C6	Sub-title.
C5	Newsflash.

PGR /1 /2 /3 A/B (R 3,4,5 & 7,8,9)

SAR$	Sub-code digit A ($ = 0 to 3) received.
SBR$	Sub-code digit B ($ = 0 to 2) received.
SCR$	Sub-code digit C ($ = 0 to 3) received.
SDR$	Sub-code digit D ($ = 0 or 1) received.
PAR$	Page number (units) ($ = 0 to 3) received.
PBR$	Page number (tens) ($ = 0 to 3) received.
MR$	Magazine number ($ = 0 to 2) received.

HAMMC (R 10)

HC$	Hamming counter ($ = 0 to 7).

RDATA (R 17)

RD$	Data read from memory ($ = 0 to 7).

I²C BUS

Device Address	0010 001 R/$\overline{W}$

The circuit works as a slave transmitter with bit eight set high or as a slave receiver with bit eight low. In receive mode, the first data byte is written to the RADD register, where the least significant five bits form the sub-address for the next register to be written. The most significant three bits of RADD are data bits, see Table 2.

Automatic incrementing of registers allows successive data bytes to be written to or read from the registers. The automatic incrementing can be disabled by setting bit 5 of the sub-address register (RADD) to one.

If the sub-address is set to write or read from DRAM, the auto incrementing allows access to successive bytes of data. All DRAM addresses may be accessed via the I²C bus register. A stop condition resets the sub-address to zero.

Examples of I²C Bus Messages

Write operation - MV1815 as a slave receiver

S	MV1815 ADD	W	A*	RADD (n)	A*	DATA (reg n)	A*	DATA (reg n + 1)	A*	P

Read operation - MV1815 as a slave transmitter

S	MV1815 ADD	R	A*	DATA* (reg 0)	A	DATA* (reg 1)	A	DATA* (reg 2)	NA	P

S	Start Condition
P	Stop Condition
A	Acknowledge
W	Write (= 0)
R	Read (= 1)
*	MV1815 output
NA	No Acknowledge

Write/read operation - MV1815 as a slave transmitter sending data from register n etc.

S	MV1815 ADD	W	A*	RADD (reg n)	A*	S	MV1815 ADD	R	A*	DATA* (reg n)	A	DATA* (reg n + 1)	NA	P

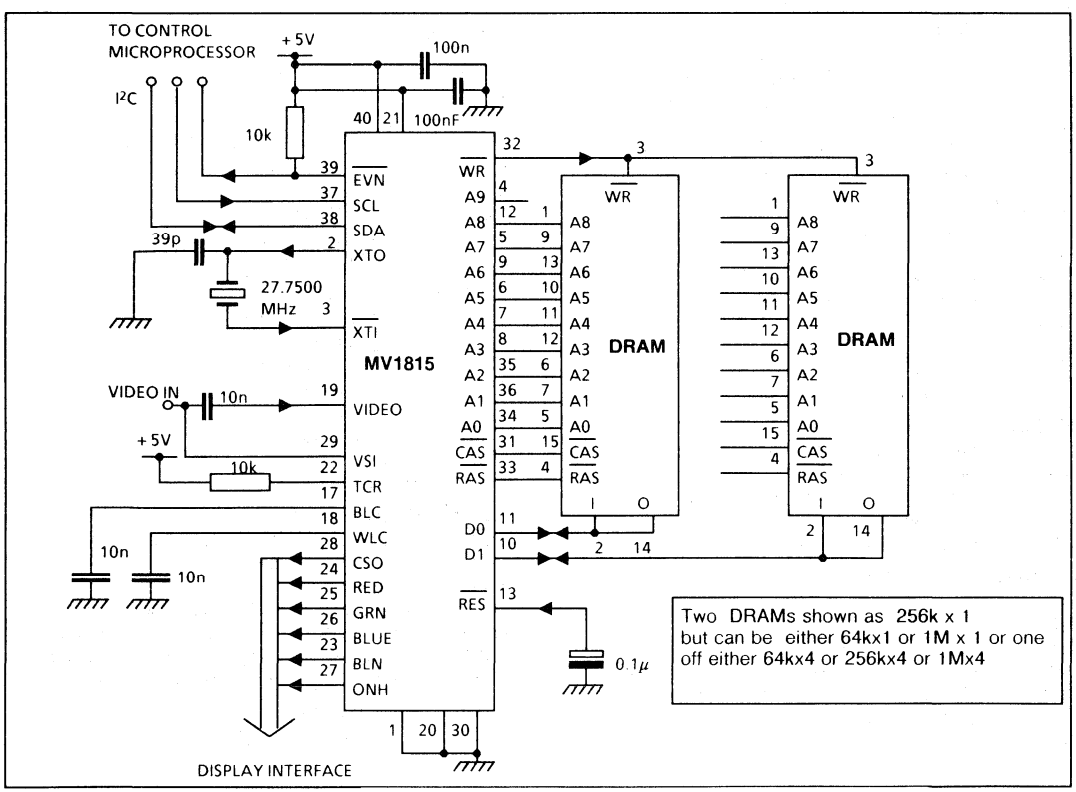


Fig.3 MV1815 Typical Applications circuit

DRAM Memory Organisation

The DRAM Memory as viewed from the I²C Bus is organised in 1024 byte blocks. Each 1024 bytes (400 HEX) block is referred to as a store. Stores 0 and 1 are reserved for the non-display packets from acquisition A and B respectively. Stores 2 and above are used for display pages, one page per store.

The display page number, first 8 bytes on row 0, are held in Store 0 bytes 0 to 7. The Time display, last 8 bytes on row 0 are also held in store 0 bytes 8 to F(HEX). See Figures 4 and 5.

To calculate the values of the start address in RADD, HADD and LADD for any store simply multiply the store number (HEX) by 400(HEX)

e.g. Decimal store 160 = A0

A0x400 = 2 80 00 (HEX)

RADD HADD LADD

To find the address of any particular location in the store add the value of the relative address from Figure 4 or 5.

Table 3 gives examples of the start addresses of stores expressed as values of A17, A16 from RADD, A15-A8 from HADD and A7-A0 from LADD.

STORE NUMBER HEX	START ADDRESS IN HEX		
	RADD	HADD	LADD
00	0	00	00
01	0	04	00
02	0	08	00
03	0	0C	00
04	0	10	00
05	0	14	00
06	0	18	00
07	0	1C	00
08	0	20	00
:		:	
0F	0	3C	00
10	0	40	00
:		:	
40	1	00	00
41	1	04	00
:		:	
7F	1	FC	00
80	2	00	00
:		:	
F0	3	C0	00
:		:	
FF	3	FC	00

Table 3.

Display Row	First byte Relative Address HEX			Last byte Relative Address HEX
0	000	NOTE 1	PACKET 0 24 byte	NOTE 2 017
1	018	PACKET 1 40 bytes		03F
2	040			
3	068			
4	090			
5	0B8			
6	0E0			
7	108			
8	130			
9	158			
10	180			
11	1A8	PACKETS 2 - 23		
12	1D0			
13	1F8			
14	220			
15	248			
16	270			
17	298			
18	2C0			
19	2E8			
20	310			
21	338			
22	360			
23	388			
24	3B0	PACKET 24		
25	3D8	PACKET 25		3FF

Figure 4. Organisation of DISPLAY Memory. Stores 2 to 256.

NOTES

1. Display of page number here, 8 bytes which are located in store 0 with absolute addesses 000 to 007.
2. Display of time here, 8 bytes which are located in store 0 with absolute addresses 008 to 00F.

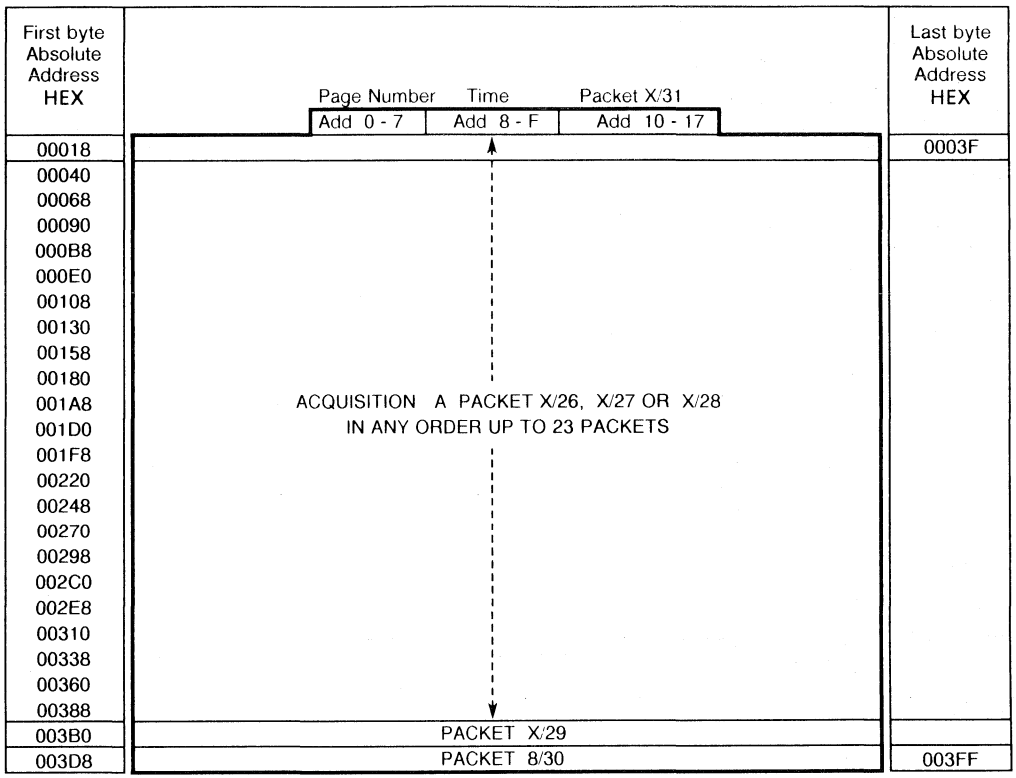


Figure 5. Store 0 Memory Organisation
Packet 8/30 designation codes 0,1,4,5,8,9, C and D are written to store 0.

NOTE
Store 1 is organised similarly except that it accepts acquisition circuit B packets X/26, etc. The starting address is 00400 (HEX) and bytes 00400 to 00417 (HEX) are not used by the MV1815. All addresses shown in Fig.5 add 00400 (HEX). Packet 8/30 designation codes 2,3,6,7,A,B,E and F are written to store 1.

ROW	0	1	COLUMN (bits 5, 6, 7, & 8) 2	3	4	5	6	7
0	Alpha Black	Graphic Black		0	@	P	—	p
1	Alpha Red	Graphics Red	!	1	A	Q	a	q
2	Alpha Green	Graphics Green	"	2	B	R	b	r
3	Alpha Yellow	Graphics Yellow	£	3	C	S	c	s
4	Alpha Blue	Graphics Blue	$	4	D	T	d	t
5	Alpha Magenta	Graphics Magenta	%	5	E	U	e	u
6	Alpha Cyan	Graphics Cyan	&	6	F	V	f	v
7	Alpha White	Graphics White	'	7	G	W	g	w
8	Flash	Conceal Display	(	8	H	X	h	x
9	Steady	Contiguous Graphics	)	9	I	Y	i	y
A	End Box	Separated Graphics	*	:	J	Z	j	z
B	Start Box	No action	+	;	K	←	k	¼
C	Normal Height	Black Background	,	<	L	½	l	‖
D	Double Height	New Background	-	=	M	→	m	¾
E	No action	Hold Graphics	.	>	N	↑	n	÷
F	No action	Release Graphics	/	?	O	#	o	

Table 4. Control Characters, Primary (English) Character Set G0 and Mosaic Graphics Set G1

LS(3210)	0000	0001	0010	0011	0100	0101	0110
TABLE POSITION	ENGLISH	GERMAN	SWEDISH FINNISH	ITALIAN	FRENCH (BELGIAN)	SPANISH	CZECH
2/3	£	#	#	£	é	ç	#
2/4	$	$	¤	$	ï	$	ů
4/0	@	§	É	é	à	¡	č
5/B	←	Ä	Ä	°	ë	á	ť
5/C	½	Ö	Ö	ç	ê	é	ž
5/D	→	Ü	Å	→	ù	í	ý
5/E	↑	^	Ü	↑	î	ó	í
5/F	#	_	_	#	#	ú	ř
6/0	―	°	é	ù	è	¿	é
7/B	¼	ä	ä	à	â	ü	á
7/C	‖	ö	ö	ò	ô	ñ	ě
7/D	¾	ü	å	è	û	è	ú
7/E	÷	ß	ü	ì	ç	à	š

LS(3210)	1000	1001	1010	1011	1100	1101	1110
TABLE POSITION	POLISH	ROMANIAN	HUNGARIAN	TURKISH	DANISH	SERBO CROAT	ASCII
2/3	#	#	#	₺	£	#	#
2/4	ń	¤	ú	ğ	$	½	$
4/0	ą	Ţ	É	i	@	Č	@
5/B	Ź	Â	í	Ş	Æ	Ć	[
5/C	Ś	Ş	Ö	Ö	Ø	Ž	\
5/D	Ł	Ă	Á	Ç	Å	Đ	]
5/E	ć	Î	ű	Ü	↑	Š	^
5/F	ó	ı	ő	Ğ	#	ë	_
6/0	ę	ţ	é	ı	―	č	`
7/B	ż	â	ó	ş	æ	ć	{
7/C	ś	ş	ö	ö	ø	ž	‖
7/D	ł	ă	á	ç	å	đ	}
7/E	ź	î	ü	ü	÷	š	~

Table 5 Latin alphabet optional variations

ROW	COLUMN (bits 5, 6, 7 & 8)													
	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		0	□	P	□	p	Á	æ	ë	Ó	Š	ů	□	
1	!	1	A	Q	a	q	Ă	Ć	ğ	Ò	Ş	ü	[	
2	"	2	B	R	b	r	Â	Č	Í	Õ	ś	ý	\	£
3	□	3	C	S	c	s	À	Ç	Î	Ö	š	Ž	]	$
4	□	4	D	T	d	t	Å	ć	Ï	Ğ	ş	Ź	^	@
5	%	5	E	U	e	u	Ã	č	ı	Ø	ß	ź	'	←
6	&	6	F	V	f	v	Ä	ç	í	ó	Ţ	ž	{	½
7	'	7	G	W	g	w	Æ	Đ	î	ő	ť	ż	□	→
8	(	8	H	X	h	x	á	d	ï	ô	ţ	a	}	↑
9	)	9	I	Y	i	y	ă	É	ì	ö	Ú	o	~	#
A	*	:	J	Z	j	z	â	È	Ł	ò	Ü	§	□	□
B	+	;	K	□	k	□	à	é	ł	õ	ú	·	□	¼
C	,	<	L	□	l	□	ą	ě	Ń	İ	TL	°	□	□
D	-	=	M	□	m	□	å	ê	ń	ø	û	¤	□	¾
E	.	>	N	□	n	□	ã	è	ň	ř	ű	¡	□	÷
F	/	?	O	□	o	■	ä	ę	Ň	Ś	ù	¿	□	■

Table 6 Character ROM contents

NOTES: Character positions F0 and F1 will be displayed as spaces but are actually spacing control characters like columns 0 and 1 of Table 4.
F0 is UNDERLINE start/stop code.
F1 is INVERT display colours start/stop code.
FF is displayed as all foreground.

□ Characters in these positions are displayed according to the setting of LS(0-3) bits. For details see Table 5.
When graphics mode is set, columns 2, 3, 6 & 7 are displayed as the graphic symbols shown in Table 4. All other columns are displayed normally.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 0 to 70°C, V_{DD} = 5V ± 10%

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply Voltage	21 & 40	4.5	5.0	5.5	V	$\overline{XTI}$ = 27.75MHz All outputs open
Supply Current	21 & 40		25		mA	circuit
	21 & 40		15		mA	$\overline{XTI}$ = 0Hz All outputs open circuit
Video Input,VSI	19 & 29					
Voltage amplitude		0.8		3.0	Vp-p	Bottom of Sync to White (p-p)
Source impedance				250	Ω	
TCR input	22					
External resistance		5	10	200	kΩ	Connected to V_{DD}
BLC and WLC	17 & 18					
Capacitor value			10		nF	Connected to GND
Capacitor tolerance		-10		+10	%	
Effective series resistance				5	Ω	1 MHz
Sync I/O	14					100kΩ (nom.) pull-up resistor
Output voltage low			0.2	0.4	V	I_{OL} = 2.4mA
Input voltage low		0		1.0	V	
Input voltage high		V_{DD}-1.0		V_{DD}	V	
Input current low		-22	-50	-220	μA	$V_{IN} = V_{SS}$
Input current high		-30		+30	μA	$V_{IN} = V_{DD}$
Data I/O	15			5	Ω	No pull-up resistor
Output voltage high		2.4	4.5		V	I_{OH} = -1.2mA
Output voltage low			0.2	0.4	V	I_{OL} = 2.4mA
Input voltage low		0		1.0	V	
Input voltage high		V_{DD}-1.0		V_{DD}	V	
Input current		-30		+30	μA	$V_{IN} = V_{DD}$ or V_{SS}
EXT/$\overline{INT}$ (note 1)	16					100kΩ (nom) pull-down resistor
Input current low		-10		+10	μA	$V_{IN} = V_{SS}$
Input current high		22	50	220	μA	$V_{IN} = V_{DD}$
$\overline{XTI}$ (note 1)	3					1M (nom) resistor to XTO
Input current low		-0.5	-5.0	-20	μA	-0.3 < V_{IN} < V_{IL} max
Input current high		0.5	5.0	20	μA	V_{IH} min < V_{IN} < (V_{DD} + 0.3)
XTO output	2					See note 2
Output voltage high		V_{DD}-1.0	4.5		V	I_{OH} = -1.0mA
Output voltage low			0.2	0.4	V	I_{OL} = 2.0mA
Frequency			27.750		MHz	± 100ppm

NOTES
1. Input voltage low and Input voltage high for these inputs are as specified for Data I/O
2. When $\overline{RESET}$ is held low, A9 (pin 4) will output $f_{OSC}/2$. If required, adjust capacitor on XTO for a frequency of 13.875 MHz.

ELECTRICAL CHARACTERISTICS (Continued)

Test conditions (unless otherwise stated)
T_{amb} = 0°C to +70°C, V_{DD} = 5V ± 10%

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
On Hour Indicator ONH	27					
Output voltage V_{OH}		V_{DD}-1.0	4.5		V	I_{OH} = -1.2mA
Output voltage V_{OL}			0.2	0.4	V	I_{OL} = 2.4mA
I²C Bus SCL, SDA I/Ps	37, 38					100kΩ (nom) pull-up resistor
Input voltage low		0		1.5	V	
Input voltage high		3.5		V_{DD}	V	
Output voltage low		0	0.1	0.40	V	I_{OL} = 3mA
SCL clock frequency	37		100	1000	kHz	
Red, Green, Blue	24,25,26					
Output voltage high		V_{DD}-1.0	4.5		V	I_{OH} = -12.0mA
Output voltage low			0.2	0.4	V	I_{OL} = 24.0mA
Tri-state output leakage current		-60		60	μA	V_{OH} = V_{SS} or V_{DD}
$\overline{\text{EVENT}}$	39					100kΩ (nom) pull-up resistor
Output voltage low			0.2	0.4	V	I_{OL} = 2.4mA
Blank	23					
Output voltage high		V_{DD}-1.0	4.5		V	I_{OH} = -12.0mA
Output voltage low			0.2	0.4	V	I_{OL} = 24.0mA
CSO	28					With typical load of 360Ω
Output voltage swing			0.5		Vpp	Text mode only, see note 3.
TEST/EVEN	30					100kΩ (nom) pull-down resistor
Output voltage high		V_{DD}-1.0	4.5		V	I_{OH} = -1.2mA
Output voltage low			0.2	0.4	V	I_{OL} = 2.4mA
Input voltage low		0		1.0	V	
Input voltage high		V_{DD}-1.0		V_{DD}	V	
Input current low		-30		+30	μA	V_{IN} = V_{SS}
Input current high		22	50	220	μA	V_{IN} = V_{DD}

NOTE 3.
CSO output voltage when in Picture or Mix mode will depend on size of Video signal applied to VSI pin 29, together with attenuation due to internal transmission switch (60Ω nom) and external load on pin 28. In these states the video signal at pin 29 is switched straight through to pin 28.

ELECTRICAL CHARACTERISTICS (Continued)

Test conditions (unless otherwise stated)
T_{amb} = 0°C to +70°C, V_{DD} = 5V ± 10%

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Memory Interface						100kΩ (nom.) pull-up resistor
Data D0,D1	11,10					
Output voltage high		V_{DD}-1.0	4.5		V	I_{OH} = -1.2mA
Output voltage low			0.2	0.4	V	I_{OL} = 2.4mA
Input voltage low		0		1.0	V	
Input voltage high		V_{DD}-1.0		V_{DD}	V	
Input current low		-22	-50	-220	μA	$V_{IN} = V_{SS}$
Input current high		-30		+30	μA	$V_{IN} = V_{DD}$
Address A0-A9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WR}$	see Fig. 1					
Output voltage high		V_{DD}-1.0	4.5		V	I_{OH} = -1.2mA
Output voltage low			0.2	0.4	V	I_{OL} = 2.4mA
$\overline{RESET}$ (Schmitt input)	13					100kΩ (nom.) pull-up resistor
Input voltage low		0		1.0	V	
Input voltage high		V_{DD}-1.0		V_{DD}	V	
Input current Low		-22	-50	-220	μA	$V_{IN} = V_{SS}$
Input current high		-10		+10	μA	$V_{IN} = V_{DD}$
Hysteresis voltage			0.8		V	(Rising threshold) - (falling threshold) voltages

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	-0.3V to +7.0V
All inputs	-0.3V to V_{DD} + 0.3V
Operating temperature	-40°C to +85°C
Storage temperature	-65°C to +150°C

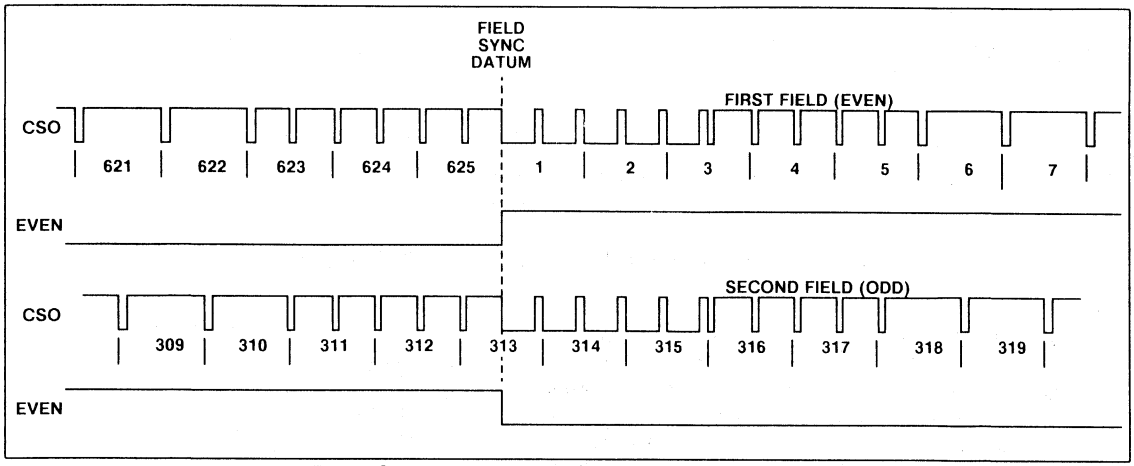


Fig.6a. Composite sync (output interlaced) and EVEN output

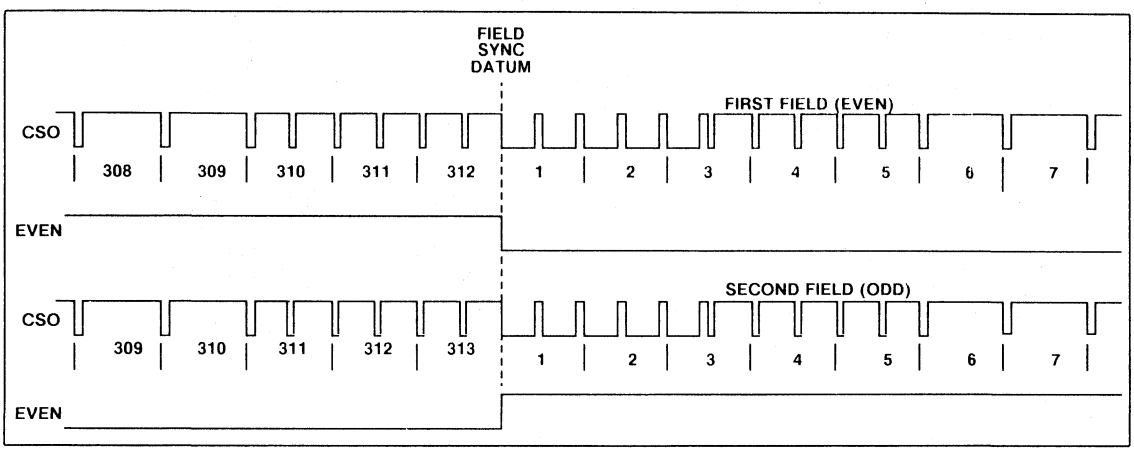


Fig.6b. Composite sync output (non-interlaced) and EVEN output

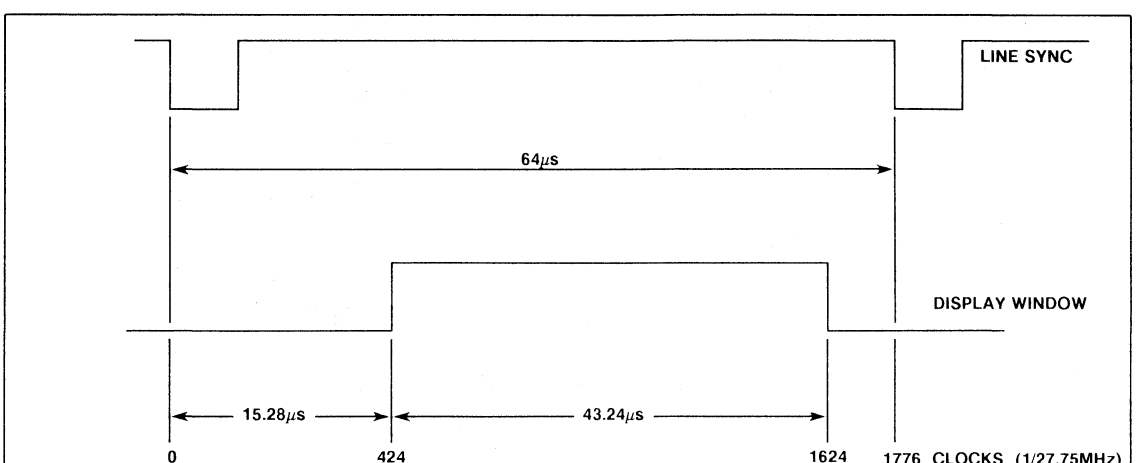


Fig.7. Timing of display window for RGB outputs related to composite sync output

MV1820

VIDEO PROGRAMME DELIVERY CONTROL INTERFACE CIRCUIT

The MV1820 is a high speed CMOS receiver for Programme Delivery Control (PDC) messages broadcast in World System Teletext (WST) Format Two Broadcast Service Data Packets (BSDP). The PDC message can be read on an I²C bus with a data format similar to standard Video Programming Service (VPS) decoders. Additional data is appended to include new PDC features.

It is intended for use in Video Cassette Recorders to provide automatic recording of suitably labelled Television programmes requested by the user.

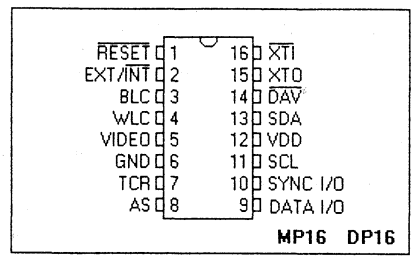


Fig.1 Pin connections - top view

FEATURES

- On-chip data slicing.
- Low external component count.
- I²C bus for low cost interfacing.
- Advanced CMOS technology gives low power disipation and high reliability.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0·3 to 7·0V
All inputs	-0·3 to V_{DD} + 0·3V
Operating Temperature	-40 to 85°C
Storage Temperature	-65 to 150°C

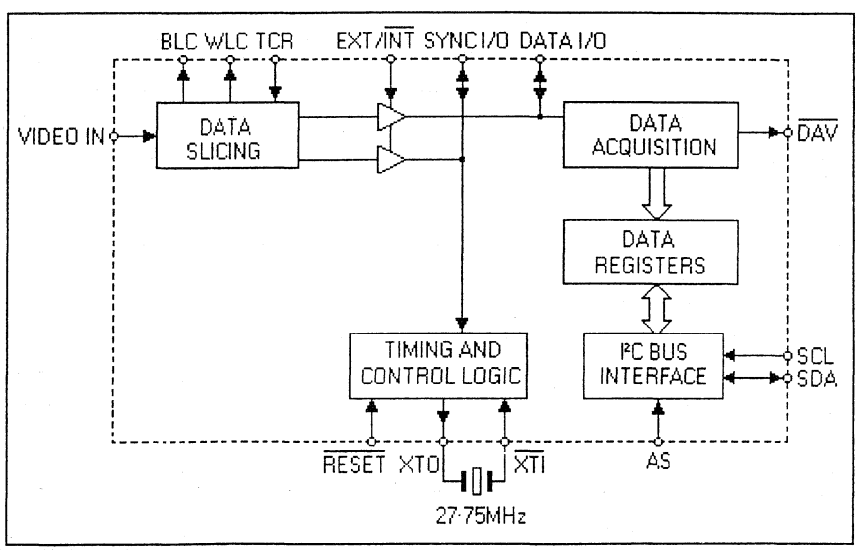


Fig.2 MV1820 block diagram

PIN DESCRIPTION

Symbol	Pin No	Pin Name and Description
$\overline{\text{RESET}}$	1	Active low reset. Includes a 100kΩ pull-up resistor.
EXT/ $\overline{\text{INT}}$	2	Control pin for SYNC and DATA I/O. Includes a100kΩ pull-down resistor. When low or not connected, internal SYNC and DATA are used, pins 9 and 10 are outputs. When,high supply SYNC and DATA from an external source, pins 9 and 10 are inputs.
BLC	3	Black level capacitor.
WLC	4	White level capacitor.
VIDEO	5	Input for composite video signal with negative going syncs.
GND	6	Ground 0 volts.
TCR	7	Time constant resistor controlling discharge rate of black and white level capacitor voltages.
AS	8	Address select for I²C bus. 0010 0001 with AS set high, or 0010 0011 with AS set low.
DATA I/O	9	Data input / output.
SYNC I/O	10	Sync input / output.
SCL	11	I²C bus serial clock.
VDD	12	Positive supply voltage +5V.
SDA	13	I²C bus bidirectional data port.
$\overline{\text{DAV}}$	14	Active low open drain output data available signal to microprocessor.
XTO	15	Crystal out, 27·75MHz fundamental crystal with on-chip 1MΩ resistor to $\overline{\text{XTI}}$
$\overline{\text{XTI}}$	16	Crystal input.

CRYSTAL SPECIFICATION.

Parallel resonant fundamental frequency 27·750000MHz. AT cut.

Tolerance at 20°C	± 20ppm.
Tolerance at -10°C to 60°C	± 50ppm.
Tolerance overall	± 100ppm.
Nominal load capacitance	20pF.
Equivalent series resistance	<20Ω

FUNCTIONAL DESCRIPTION

The video signal is sliced to produce data and synchronising signals. Timing circuits monitor the sync signal to enable the MV1820 to lock onto the broadcast signal. A timing window, for the Vertical Blanking Interval (VBI) lines 6 - 22 and 318 - 335, is established to enable the acquisition circuit to monitor the sliced data signal for valid teletext data.

The framing code is checked for valid World System Teletext (WST) data. Magazine, packet and designation code bytes are checked and valid Broadcast Service Data Packets (BSDP) format two type only are accepted. These are also known as packet 8/30. Format two is signalled by byte six, data bit two being set high and bits 3 and 4 set low. Bytes 13 to 25 inclusive are Hamming decoded (8, 4) and stored in seven registers each of eight bits. If the complete message is correctly received with no uncorrectable Hamming errors, an interrupt to the microprocessor is signalled by the $\overline{\text{DAV}}$ pin going low. At the same time the data is transferred to a second bank of registers, reorganized with original numbered bytes 14, 15, 24, 25 and 13 placed after byte 23, to be read out on the I²C bus when so requested. Subsequent valid messages will continue to be transferred to the output registers over-writing any existing data. In this way the output registers always contain the latest PDC message.

The MV1820 is configured as an I²C bus slave transmitter with a selectable address. The I²C bus address is 0010 0001 (20+1hex) with the address select (AS) pin set high, or 0010 0011 (22+1hex) with the AS pin set low. The read bit (LSB) must always be set, it is not possible to write to the MV1820.

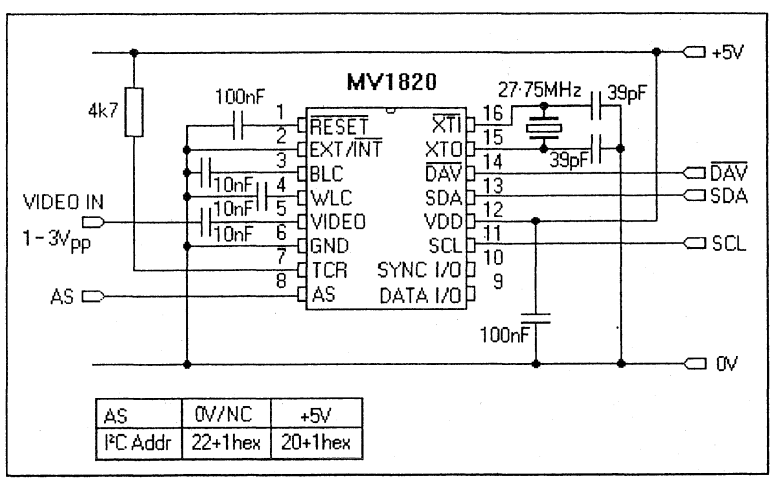
On recognising its address, the MV1820 will send an acknowledge and then transmit on the SDA line the first byte from the output registers (decoded bytes 16 and 17) most significant bit (MSB) first. It will then monitor the SDA line for an acknowledge from the microprocessor. If the microprocessor does NOT send an acknowledge, the MV1820 will release the data line to allow the microprocessor to send a stop condition. If the microprocessor does send an acknowledge, the following bytes of the message will be output provided each byte is acknowledged. The final data will be byte 13 followed by four '1's.

When readout is complete, the $\overline{\text{DAV}}$ pin is reset high and the output registers are all set high. If the microprocessor continues to send clocks on the SCL line, the MV1820 will output FF bytes on the SDA line. Also, if the MV1820 is re-addressed before another PDC message is received, the MV1820 will output FF bytes on the SDA line. The microprocessor can prematurely stop the message by NOT sending an Acknowledge followed by a STOP condition after any byte has been sent by the MV1820. The registers will then be reset to FF bytes and the $\overline{\text{DAV}}$ pin will be reset high.

To prevent any corruption of the data in the output registers during I²C bus activity, valid PDC messages are held in the incoming registers until I²C bus activity ceases. Here they may be over-written by new PDC messages until the I²C bus activity ceases and they can be transferred to the output registers.

System clock is provided by an on chip 27·75MHz oscillator together with an external parallel resonant fundamental frequency AT cut crystal.

Following a reset, $\overline{\text{RESET}}$ pulled low, the output I²C bus registers will contain FF bytes and the $\overline{\text{DAV}}$ pin will be set high.



AS	0V/NC	+5V
I²C Addr	22+1hex	20+1hex

Fig.3 Typical application diagram

Order of data output on the I²C bus.

BIT ORDER		EBU NUMBERING		BIT VALUE		VPS EQUIVALENCE
byte 1	bit 7	byte 16	bit 0 - CNI b9		reserved	byte 11
	bit 6		bit 1 - CNI b10	64	network (or programme provider)	
	bit 5		bit 2 - PIL b1	16		
	bit 4		bit 3 - PIL b2	8		
	bit 3	byte 17	bit 0 - PIL b3	4	day	
	bit 2		bit 1 - PIL b4	2		
	bit 1		bit 2 - PIL b5	1		
	bit 0		bit 3 - PIL b6	8		
byte 2	bit 7	byte 18	bit 0 - PIL b7	4		byte 12
	bit 6		bit 1 - PIL b8	2	month	
	bit 5		bit 2 - PIL b9	1		
	bit 4		bit 3 - PIL b10	16		
	bit 3	byte 19	bit 0 - PIL b11	8		
	bit 2		bit 1 - PIL b12	4	hour	
	bit 1		bit 2 - PIL b13	2		
	bit 0		bit 3 - PIL b14	1		
byte 3	bit 7	byte 20	bit 0 - PIL b15	32		byte 13
	bit 6		bit 1 - PIL b16	16		
	bit 5		bit 2 - PIL b17	8		
	bit 4		bit 3 - PIL b18	4	minute	
	bit 3	byte 21	bit 0 - PIL b19	2		
	bit 2		bit 1 - PIL b20	1		
	bit 1		bit 2 - CNI b5	8		
	bit 0		bit 3 - CNI b6	4		
byte 4	bit 7	byte 22	bit 0 - CNI b7	2	country	byte 14
	bit 6		bit 1 - CNI b8	1		
	bit 5		bit 2 - CNI b11	32		
	bit 4		bit 3 - CNI b12	16		
	bit 3	byte 23	bit 0 - CNI b13	8	network (or programme provider)	
	bit 2		bit 1 - CNI b14	4		
	bit 1		bit 2 - CNI b15	2		
	bit 0		bit 3 - CNI b16	1		
byte 5	bit 7	byte 14	bit 0 - PCS b1	2	status (define the analogue sound	byte 5
	bit 6		bit 1 - PCS b2	1	transmission system)	
	bit 5		bit 2 - unallocated			
	bit 4		bit 3 - unallocated			
	bit 3	byte 15	bit 0 - CNI b1	128		
	bit 2		bit 1 - CNI b2	64		
	bit 1		bit 2 - CNI b3	32	country	
	bit 0		bit 3 - CNI b4	16		
byte 6	bit 7	byte 24	bit 0 - PTY b1	128		byte 15
	bit 6		bit 1 - PTY b2	64		
	bit 5		bit 2 - PTY b3	32		
	bit 4		bit 3 - PTY b4	16	programme type	
	bit 3	byte 25	bit 0 - PTY b5	8		
	bit 2		bit 1 - PTY b6	4		
	bit 1		bit 2 - PTY b7	2		
	bit 0		bit 3 - PTY b8	1		
byte 7	bit 7	byte 13	bit 0 - INT b1	2	Interleave up to	
	bit 6		bit 1 - INT b2	1	four PIL messages.	
	bit 5		bit 2 - LUF	1	Label Update Flag (LUF)	
	bit 4		bit 3 - unallocated			
	bit 3		- set to 1			
	bit 2		- set to 1			
	bit 1		- set to 1			
	bit 0		- set to 1			

NOTE: Data is output on the I²C bus MSB first.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0 to 70°C, V_{DD} = 5V ±10%

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply Voltage	12	4·5	5·0	5·5	V	
Supply Current	12		20		mA	
Video Input	5					
Voltage amplitude		1·0		3·0	Vpp	Bottom of sync to white (pk to pk)
Source impedance				250	Ω	
TCR input	7					
External resistance		4·7	4·7	200	kΩ	Connected to V_{DD}
BLC and WLC	3 & 4					
Capacitor value			10		nF	Connected to GND
Capacitor tolerance		-10%		+10%		
Effective series resistance				5	Ω	1MHz
DATA I/O & SYNC I/O	9 &10					
Output voltage High		V_{DD} - 1·0	4·5		V	I_{OH} = -1·2mA
Output voltage Low			0·2	0·4	V	I_{OL} = 2·4mA
Input voltage Low		0		1·0	V	
Input voltage High		V_{DD} - 1·0		V_{DD}	V	
Input current		-30		+30	µA	$V_{IN} = V_{SS}$ or V_{DD}
EXT/$\overline{INT}$ & AS	2 & 8					100k (nom) pull-down resistor
Input current Low		-30		+30	µA	$V_{IN} = V_{SS}$
Input current High		22	50	220	µA	$V_{IN} = V_{DD}$
$\overline{XTI}$ input	16					
Input current Low		-0·5	-5·0	-20	µA	-0·3 <V_{IN} <V_{IL} max
Input current High		0·5	5·0	20	µA	V_{IH}min <V_{IN} <(V_{DD} +0·3)
XTO output	15					
Output voltage High		V_{DD} - 1·0	4·5		V	I_{OH} = -1·0mA
Output voltage Low			0·2	0·4	V	I_{OL} = 2·0mA
Frequency			27·750		MHz	±100ppm
I²C bus						
SCL, SDA Schmitt inputs	11, 13					100k (nom) pull-up resistor
Input voltage Low		0		1·5	V	
Input voltage High		3.0		V_{DD}	V	
Output voltage Low			0.1	0·4	V	I_{OL} = 3·0mA
SCL Clock Frequency	11		100	1000	kHz	
$\overline{DAV}$ Data available	14					100k (nom) pull-up resistor
Output voltage Low			0·2	0·4	V	I_{OL} = 2·4mA
$\overline{RESET}$ Schmitt input	1					100k (nom) pull-up resistor
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD} - 1·0		V_{DD}	V	
Input current Low		-22	-50	-220	µA	$V_{IN} = V_{SS}$
Input current High		-10		+10	µA	$V_{IN} + V_{DD}$
Hysteresis Voltage			0·8		V	(Rising threshold) – (falling threshold) voltages

NOTE

Input voltage low and Input voltage high for EXT/$\overline{INT}$, AS and $\overline{XTI}$ are as specified for DATAI/O

3104-1.0

ZNA134

CCIR/EIA TV SYNCHRONISING PULSE GENERATOR

FEATURES

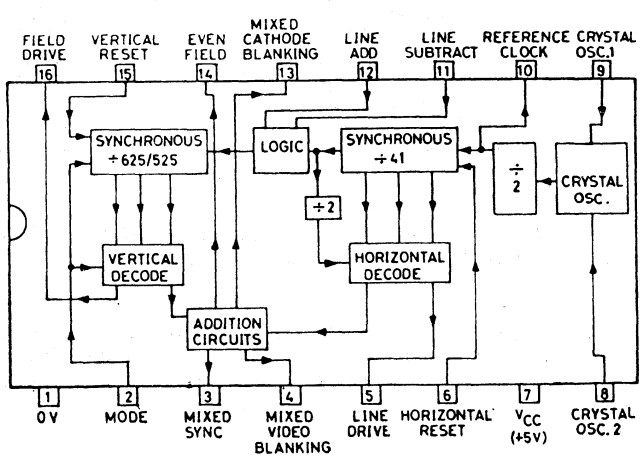
- 625 and 525 line standards.
- CCIR and EIA standard outputs.
- Single 5 volt supply, fully TTL compatible.
- Easy synchronising between generators.
- Direct reset to vertical and horizontal counters.
- Facility for adding and subtracting lines.
- Automatic interlacing.
- On chip oscillator (requiring external crystal).
- Can be driven with an external oscillator.
- Field reference output.

GENERAL DESCRIPTION

The ZNA134 integrated circuit utilises a 2.5 MHz* crystal to generate all the horizontal, vertical, mixed blanking and synchronising pulses necessary for raster generation in 625 or 525 line commercial, industrial or military television systems. The synchronous dividers and decoding logic employed within the unit ensure perfect interlace, together with spike-free output waveforms having precisely defined relative positions and pulse widths. The device is contained in a 16 pin D.I.L. and can be selected to operate over the military temperature range.

*Dependent on line system used, series resonant.

SYSTEM DIAGRAM



DG16

CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Maximum value
Supply Voltage	7 volts
Input Voltage	5 volts
Operating Temperature Range	0°C to +70°C*
Storage Temperature Range	−65°C to +150°C

*Also available over wider range on request.

OPERATING CHARACTERISTICS

(over recommended temperature range)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		4.75	5.0	5.25	Volts
Supply Current	I_S		–	100	–	mA
High-level Input Voltage	V_{IH}		2.4	–	–	Volts
Low-level Input Voltage	V_{IL}		–	–	0.8	Volts
High-level Input Current	I_{IH}	$V_{CC} = 5V$, $V_I = 2.4V$ (See Note 1)	–	–	40	μA
Low-level Input Current	I_{IL}	$V_{CC} = 5V$, $V_I = 0$ V. (See Note 1)	–40	–	–	μA
High-level Output Voltage	V_{OH}	$V_{CC} = 5V$, $I_{source} \leqslant 80\mu A$ (See Note 2)	2.4	–	–	Volts
Low-level Output Voltage	V_{OL}	$V_{CC} = 5V$, $I_{sink} \leqslant 3.2$ mA (See Note 2)	–	–	0.5	Volts
Clock frequency	f_{clock}	625 lines, Mode = '1' 525 lines, Mode = '0'	– –	2.56250 2.5830	– –	MHz MHz
External Oscillator Pulse Width	t_w	-ve going pulse, 625/525 lines	150	200	250	ns

Note 1

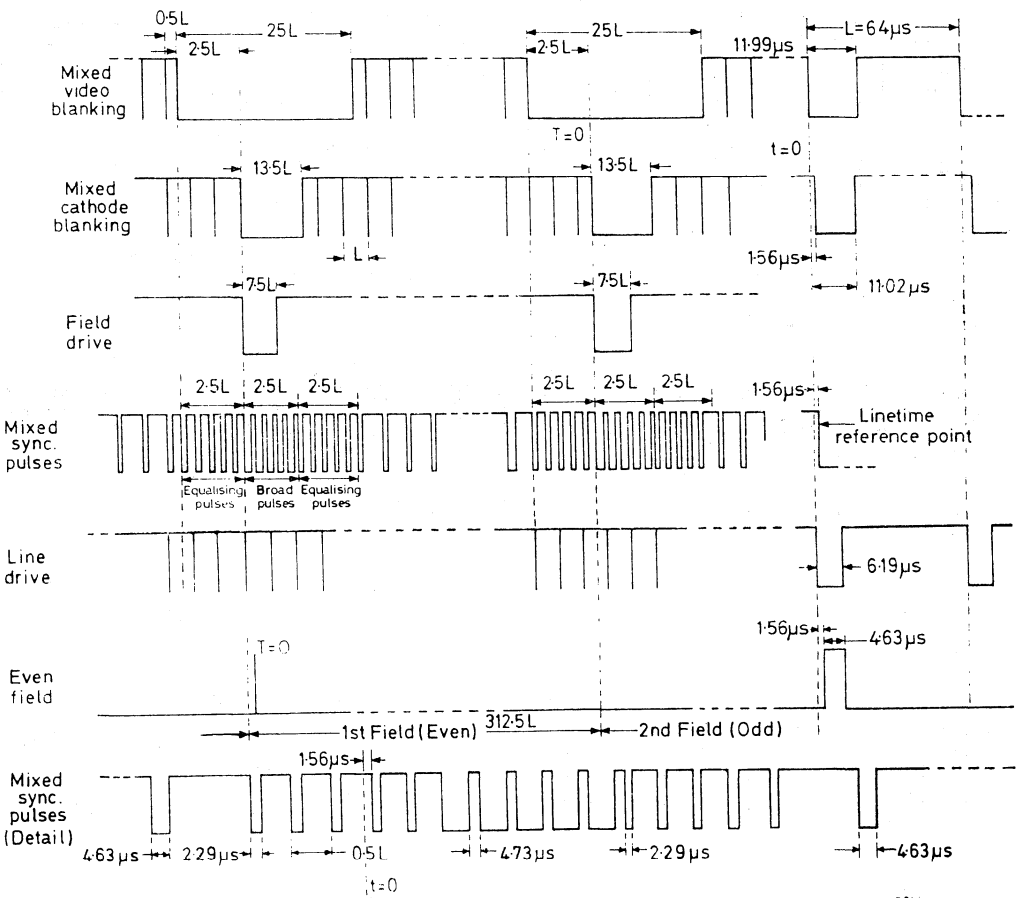
Input conditions only apply to mode, horizontal reset, vertical reset, line subtract and line add. For input conditions of oscillator inputs C.0.1, C.0.2, see applications section.

Note 2

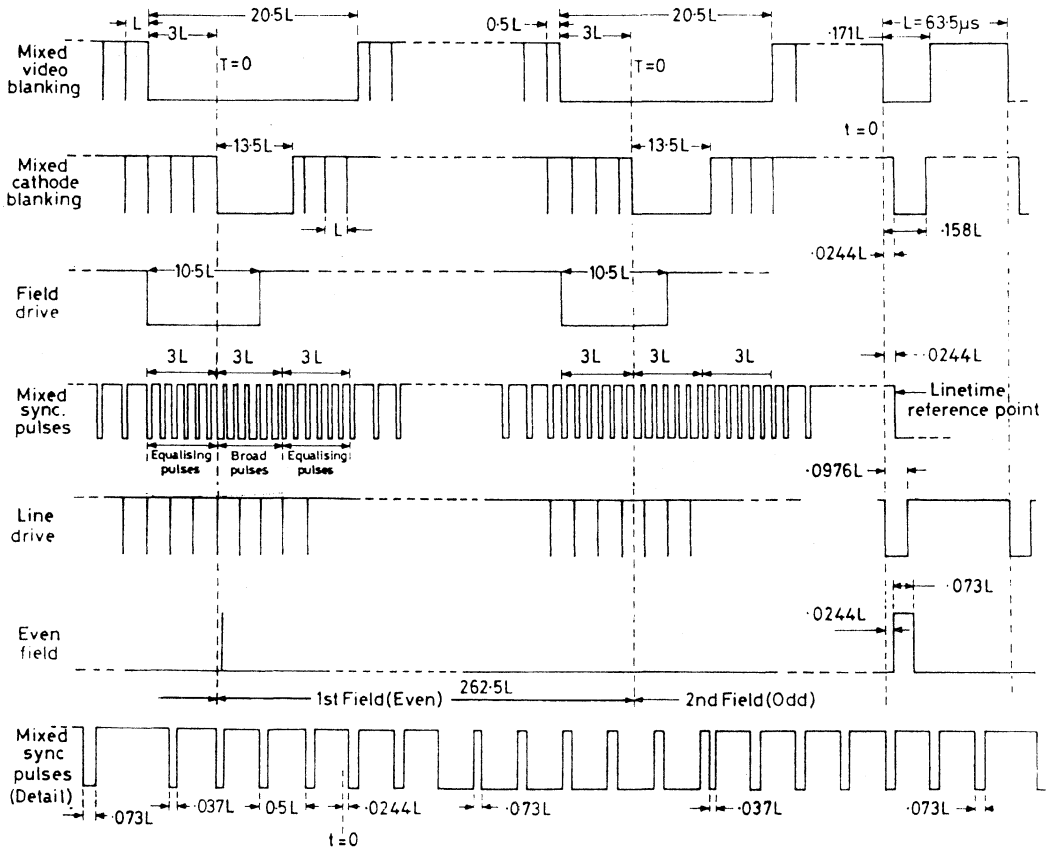
All outputs – mixed sync, mixed video blanking, line drive, reference clock, mixed cathode blanking, even field and field drive have internal 10kΩ pull-up resistors. Edge speeds and sourcing capability can be increased, if required, by the addition of external pull-up resistors. These should have a minimum value of 2kΩ.

OUTPUT WAVEFORMS

(a) 625 line CCIR standard output (Mode = 1).
Crystal frequency = 2.5625 MHz.
Line frequency = 15.625 kHz, Field frequency = 50 Hz.
Line period = 64 μs, Field period = 20 ms.



(b) 525 line EIA standard output (Mode = 0).
Crystal frequency = 2.5830 MHz
Line frequency = 15.750 kHz, Field frequency = 60 Hz
Line period = 63.5 μs, Field period = 16.66 ms.



APPLICATIONS INFORMATION

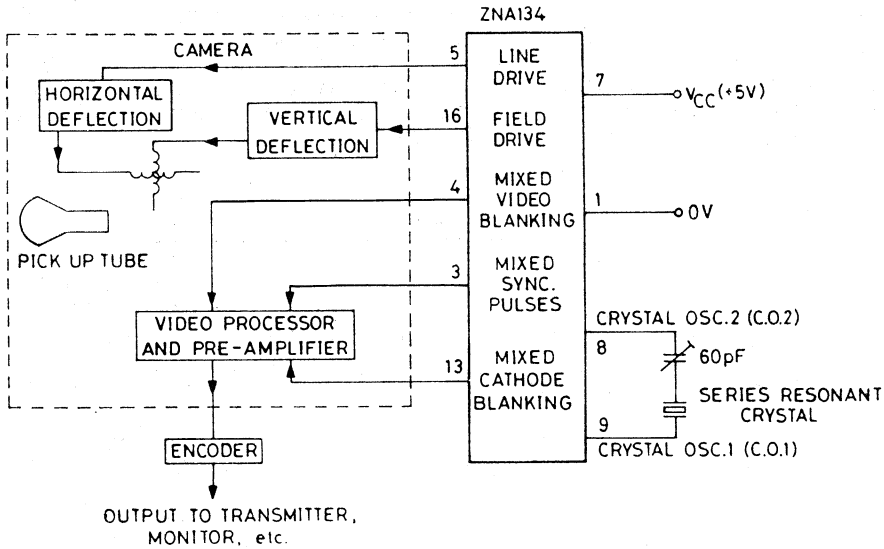


Fig. 1. Application in a TV system

The sync. pulse generator can be driven from an external oscillator if required. C.O.1 must then be connected via a 10kΩ resistor to V_{CC}. The external oscillator can then drive directly into C.O.2 input as shown in Fig. 2.

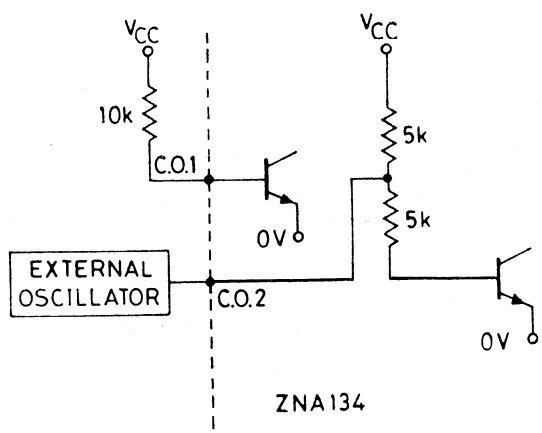


Fig. 2

Mode input (pin 2) can be connected directly to V_{CC} or 0V for 625 or 525 line operation respectively Any of the inputs: vertical reset, horizontal reset, line add, line subtract, not being used should be connected to 0V.

SIMPLE METHOD OF SYNCHRONISATION USING VERTICAL AND HORIZONTAL RESET

Line synchronisation (Fig. 3) is achieved by using a narrow positive going pulse derived from the negative going edge of the Line Drive output of the first generator to drive the Horizontal Reset inputs of the other generators. This monostable pulse, which should have a width of 200 ns ± 40 ns, resets the generators to the start of a line (t = 0). This results in the Line Drive waveforms of the driven generators being one reference clock period (≃800 ns) delayed from the first generator. The C.O.2 pins of the generators must be connected together.

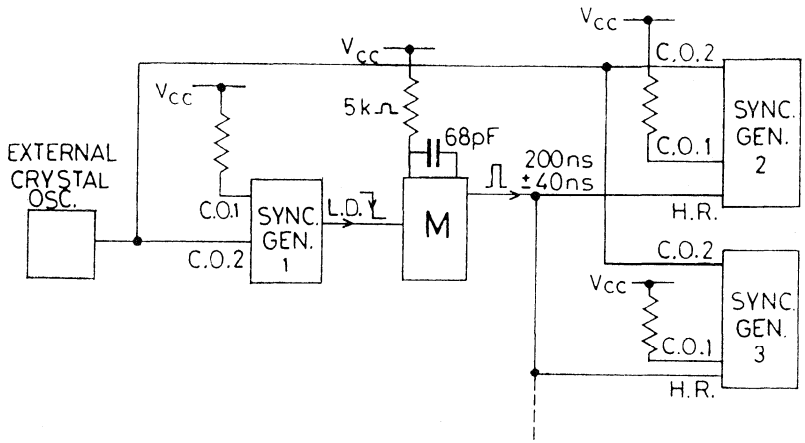


Fig. 3 Line Synchronisation using Horizontal Reset

Field Synchronisation (Fig. 4) is achieved by driving the Vertical Reset inputs of the driven generators directly from the Even Field output of the first generator (the Line drive outputs should already be in phase). This resets the generators to the start of the first field (T = 0, start of broad pulses.)

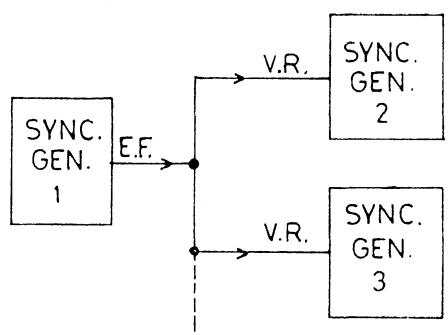


Fig. 4 Field Synchronisation using Vertical Reset

With this method of synchronisation, line sync and field sync are lost at the monitor for a brief period due to a sudden change in the Mixed Sync waveform. Hence it is only suitable for CCTV systems where momentary loss of picture is not critical or where the generators are to be synchronised automatically at power switch on.

SYNCHRONISATION USING THE LINE ADD/SUBTRACT FACILITY

This is suitable where generator lock must be achieved gradually, i.e. without loss of picture at the receiver, as in studio camera systems.

Line Synchronisation can be achieved smoothly by the use of a phase locked loop technique rather than the direct Horizontal Reset technique (Fig. 5).

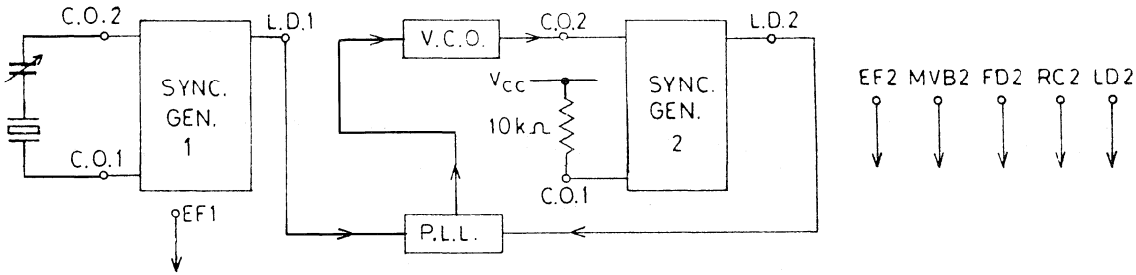


Fig. 5 Line Lock Circuitry

Field Synchronisation (Fig. 6). The generator waveforms are brought into synchronisation by adding or subtracting one line per frame to the second generator until the waveforms are exactly in phase. This is achieved by adding or inhibiting pulses at the start of the first full line after field blanking, thus preventing any changes to the mixed sync. waveform during the broad and equalising pulse periods. Lines are 'added' by clocking the vertical counter faster than the normal half line rate. Setting Line Add high for a period equal to 4 Reference Clock pulses, increments the vertical counter by one line thus effectively reducing the field period by one line.

Lines are 'subtracted' by inhibiting the clock pulses to the vertical counter. Setting Line Subtract high for a period of one line leaves the state of the vertical counter unchanged for one line thus effectively increasing the field period by one line.

Hence the add or subtract periods are generated by counting Reference Clock or Line Drive pulses respectively with a 3 bit counter.

Lines are added or subtracted until the generators are in phase. The two Even Field outputs together generate a pulse which inhibits the add/subtract circuitry when an in-phase condition occurs.

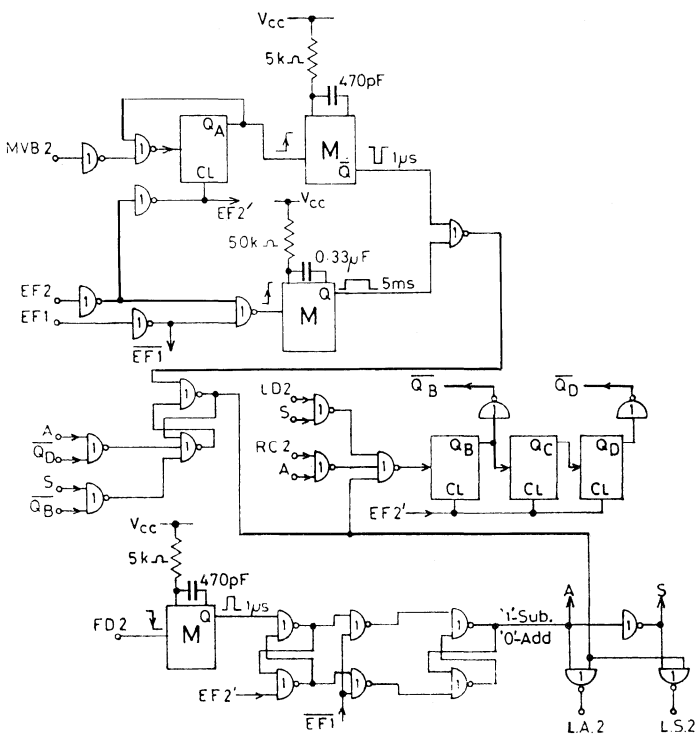


Fig. 6 Field Lock Circuitry

Lines are added to the second generator if EF2 is less than one field period delayed from EF1, and subtracted if EF2 is greater than one field period delayed from EF1 to reduce synchronisation time The add/subtract circuitry can be built using nine TTL packages :-

4 off	7402
1 off	7427
1 off	7404
1 off	74123
1 off	74121
1 off	7493

The circuit in Fig. 6 adds or subtracts one line per frame but this could be extended to two or more lines per frame by adding further bits to the 3 bit counter and decoding the relevant states. Similarly half a line per frame can be added by decoding 'QC' instead of 'QB'.

The circuit operates in 625 or 525 line mode without any changes to the component values.

ZNA234E

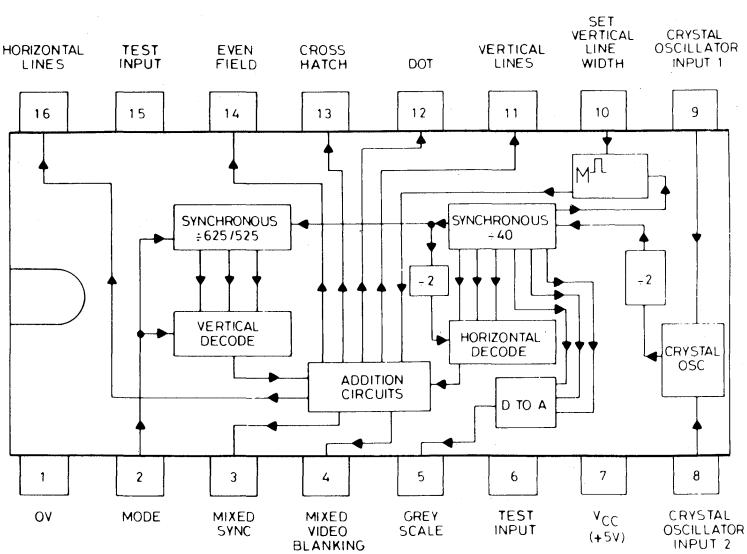
TV PATTERN GENERATOR

FEATURES

- Single 5V supply.
- 625 or 525 line operation.
- Sync and Blanking outputs to CCIR or EIA Standard.
- Field Reference output.
- Separate outputs for:
  - Crosshatch
  - Dot
  - Vertical Lines
  - Horizontal Lines
  - Greyscale
  - Mixed Sync
  - Mixed Video Blanking
- Adjustable vertical line width.

DESCRIPTION

The ZNA234E integrated circuit makes available all the waveforms necessary to produce cross-hatch, dot and greyscale test patterns on a television screen. All that is required is a 2.50MHz crystal (or external oscillator) and a minimum number of external components for mixing video, sync and blanking pulses to give a composite video signal. This can be either injected directly into the video stages of a receiver, or used to drive a UHF modulator/oscillator for connection to the aerial socket. The device is contained in a 16 pin DIL package.



System Diagram

DP16

ABSOLUTE MAXIUMUM RATINGS

Supply Voltage	7 volts
Input Voltage	5 volts
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

OPERATING CHARACTERISTICS (over recommended temperature range).

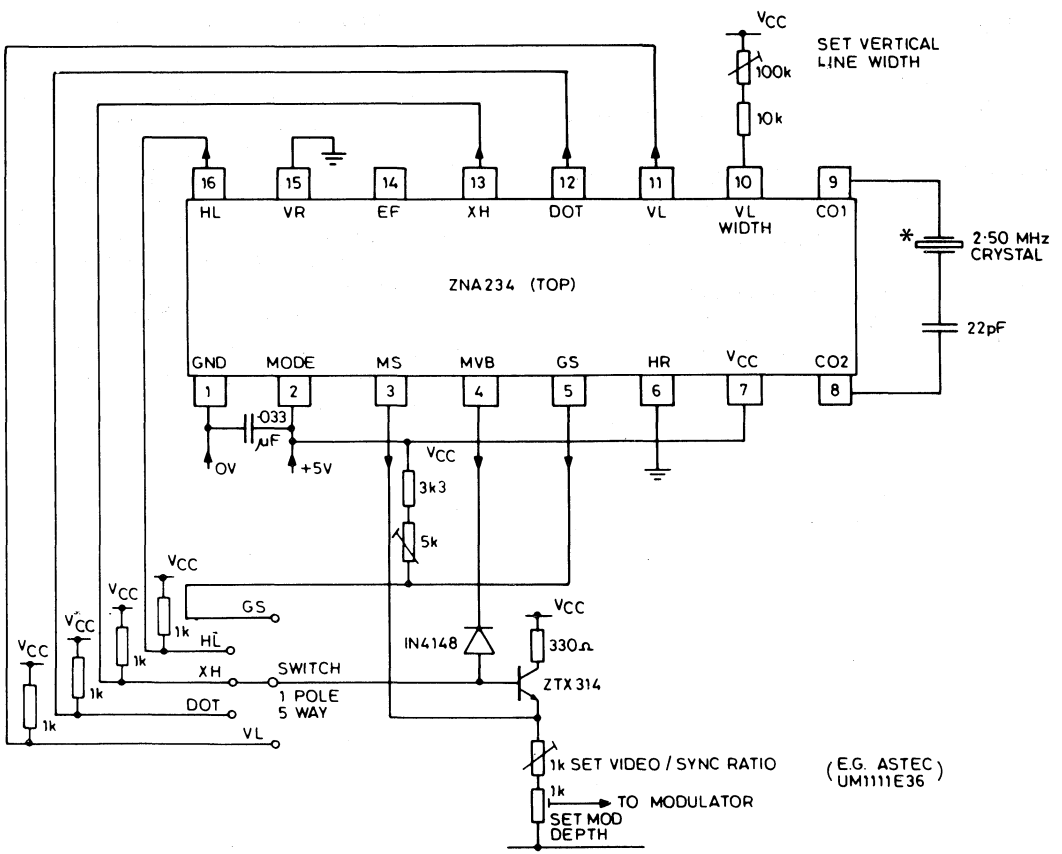
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Voltage	V_{CC}	4.75	5.0	5.25	Volts	
Supply Current	I_S	—	135	—	mA	
High-level Input Voltage	V_{IH}	2.4	—	—	Volts	
Low-level Input Voltage	V_{IL}	—	—	0.8	Volts	
High-level Input Current	I_{IH}	—	—	40	μA	$V_{CC}=5V$, $V_I=2.4V$ (See Note 1)
Low-level Input Current	I_{IL}	−40	—	—	μA	$V_{CC}=5V$, $V_I=0V$ (See Note 1)
High-level Output Voltage	V_{OH}	2.4	—	—	Volts	$V_{CC}=5V$, $I_{Source}\leqslant 250\mu A$ (See Note 2)
Low-level Output Voltage	V_{OL}	—	—	0.5	Volts	$V_{CC}=5V$, $I_{Sink}\leqslant 5.0mA$ (See Note 2)
Clock Frequency	f_{clock}	— —	2.500 2.520	— —	MHz MHz	625 lines, Mode = '1' 525 lines, Mode = '0'
External Oscillator Pulse Width	t_w	150	200	250	ns	−ve going pulse, 625/525 lines

Note 1:
Input conditions only apply to mode input. For input conditions of oscillator inputs C01, C02, see applications section.

Note 2:
All outputs except greyscale, i.e. mixed sync, mixed video blanking, vertical lines, dots, crosshatch, even field and horizontal lines have internal 3k3 pull-up resistors. Edge speeds and sourcing capability can be increased, if required, by the addition of external pull-up resistors, These should have a minimum value of 1 kΩ.

COMPLETE PATTERN GENERATOR USING THE ZNA234

(for detailed information see applications section)



*The following Companies can supply suitable crystals for use with the ZNA234

IQD
(Interface Quartz Devices Limited),
Crewkerne,
Somerset.
Tel: 0460 74433 Telex: 46283
Contact: Mr. Jarvis

McKnight Crystal Company,
Hardley Industrial Estate,
Hythe, Southampton.
Tel: 0703 848961 Telex: 47506
Contact: Mr. Carpenter

SEI
(Salford Electrical Instruments Limited),
Times Mill,
Heywood, Lancashire OL10 4NE
Tel: 0706 67501 Telex: 635106
Contact: Mr. P. Kenyon or Mr. D. Standring

OUTPUT INFORMATION AND WAVEFORMS

(a) **625 Lines** CCIR Timing (Mode=1)
Crystal Frequency = 2.50MHz
Line Frequency = 15.625kHz,
Line Period = 64μs
Field Frequency = 50Hz,
Field Period = 20ms.

Outputs
20 Horizontal Lines; 18 visible, 2 during Field blanking.
20 Vertical Lines; 16 visible, 4 during Line blanking.

Crosshatch squares have approx. 1.4:1 aspect ratio (0.98" × 0.67" on 20" screen).

For timing diagrams see page 5.

(b) **525 Lines** EIA Timing (Mode=0)
Crystal Frequency = 2.520MHz
Line Frequency = 15.750kHz,
Line Period = 63.5μs
Field Frequency = 60Hz,
Field Period = 16.66ms.

Outputs
17 Horizontal Lines; 15 visible, 2 during Field blanking.
20 Vertical Lines; 16 visible, 4 during Line blanking.

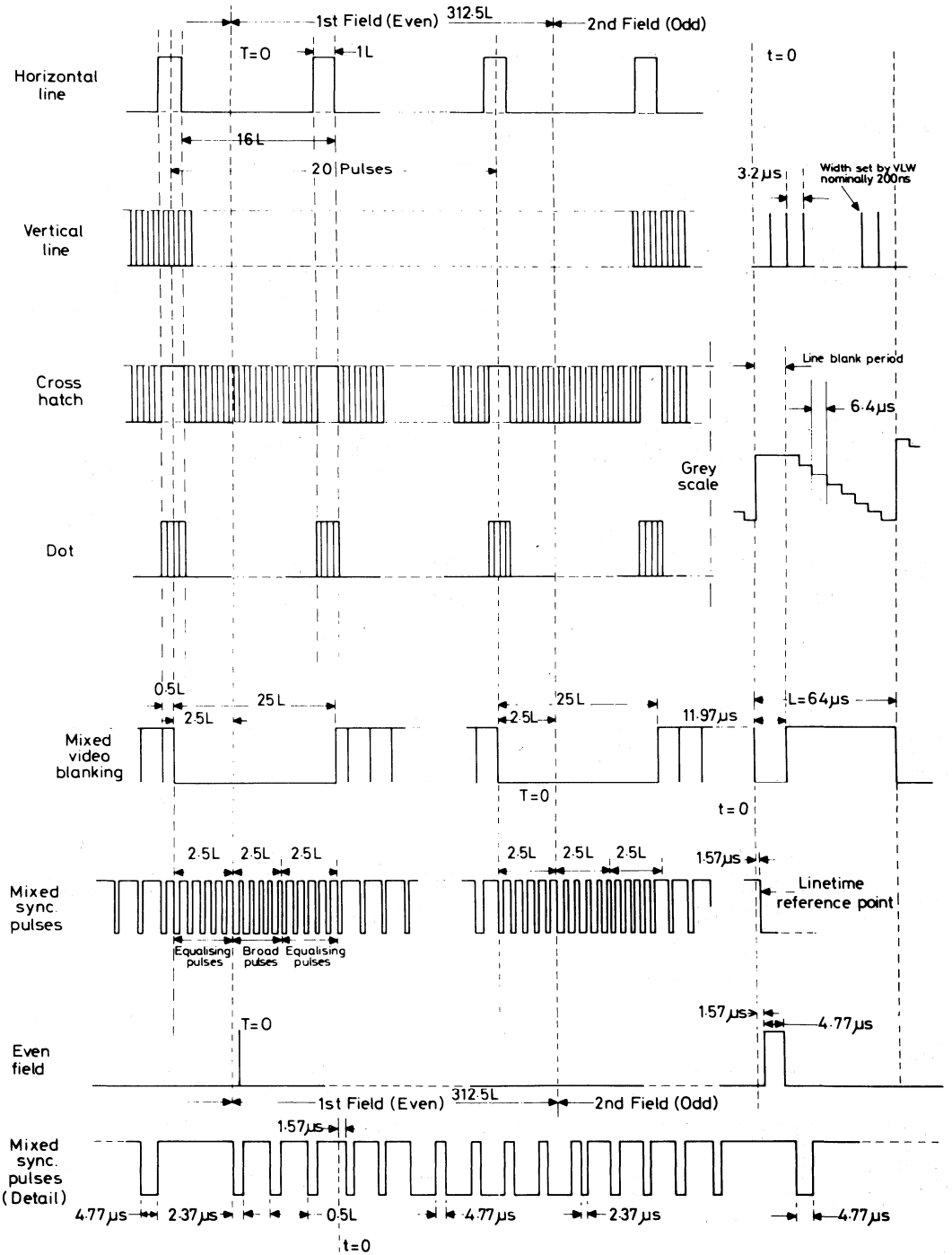
Crosshatch squares have approx 1. 2:1 aspect ratio (0.97" × 0.79" on 20" screen.)

For timing diagrams see page 6.

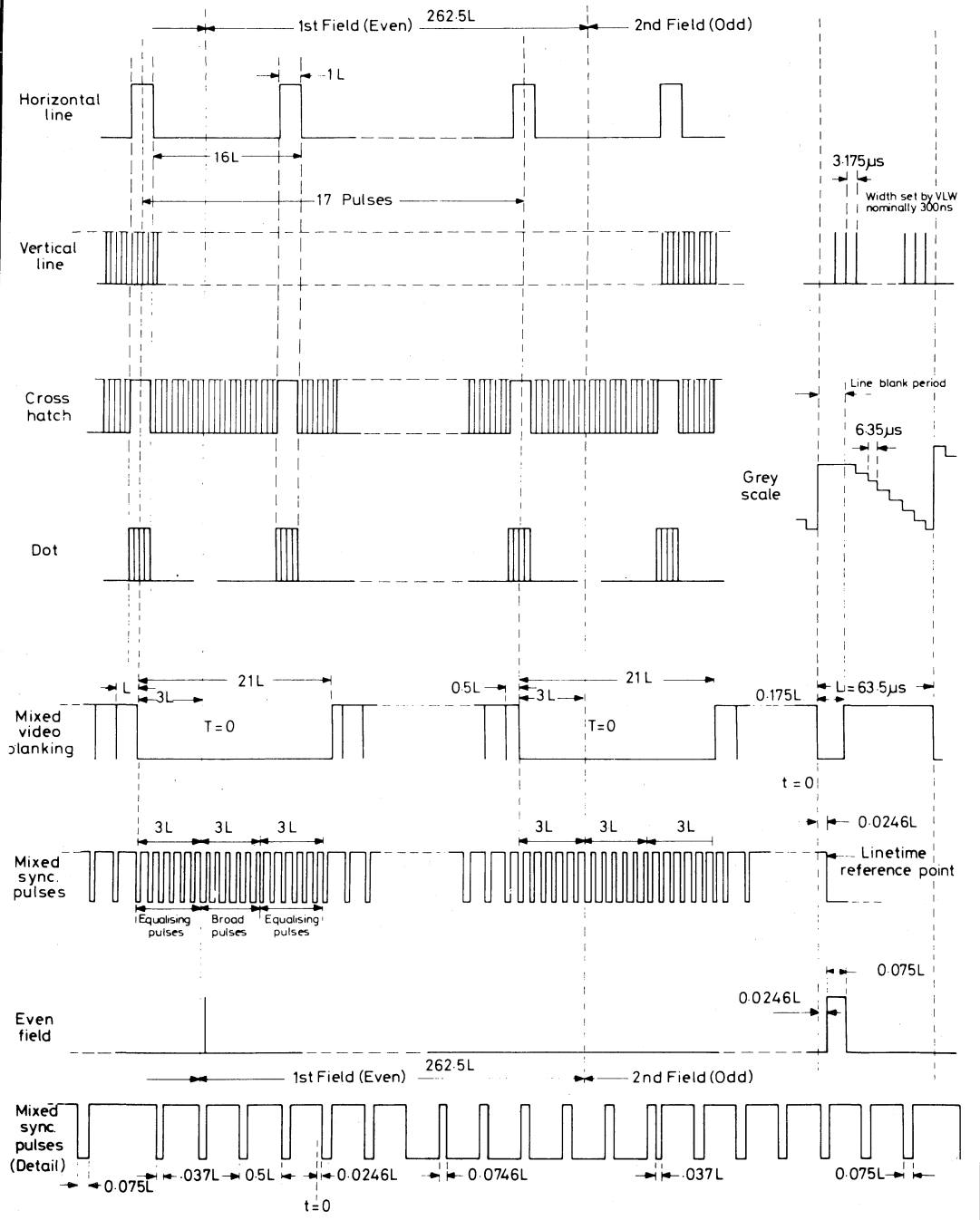
The horizontal line waveform consists of pulses 1 line wide occuring every 16 lines, producing horizontal lines 2 lines wide (owing to interlacing) on the screen. The vertical line waveform is a continuous series of pulses nominally 300ns wide occuring every 3μs (approximately). As these pulses occur in the same position in every line period the result is a series of vertical lines on the screen.

The two waveforms are fed to internal AND and OR gates to produce dot and crosshatch outputs respectively.

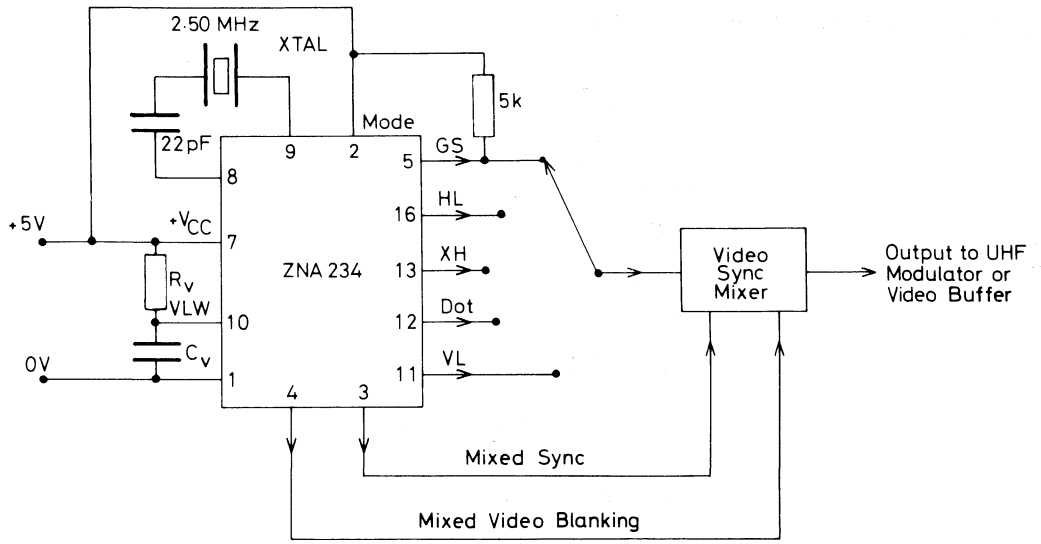
OUTPUT WAVEFORMS — 625 LINES



OUTPUT WAVEFORMS — 525 LINES



APPLICATION INFORMATION



T.V. Pattern Generator Using the ZNA234 (625 lines)

NOTES:

Mode, Pin 2

The mode input should be connected to V_{CC} for 625 lines or to 0V for 525 line operation.

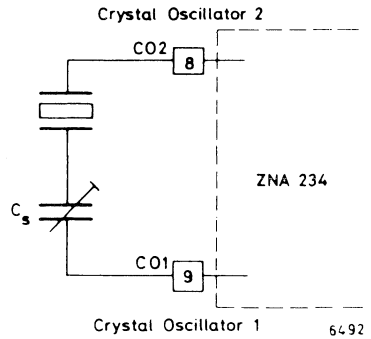
Greyscale, Pin 5

The greyscale output is produced by a D to A converter from the horizontal counter. The D to A converter is effectively a switched current sink providing 8 equal current steps of approx 60μA/step. When used with an external pull-up resistor, 8 voltage steps are produced (approx 0.3V/step with $R_L = 5K$). The output has a saturation level of approximately +2V and requires a buffer stage (emitter follower) to match into the video/sync mixer.

Oscillator. Pins 8 and 9.
The ZNA234 oscillator can be driven in several ways, depending on the application.

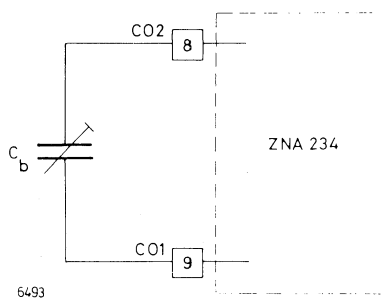
(a) Using external 2.50MHz crystal (625 lines mode)

Series
Resonant
Crystal



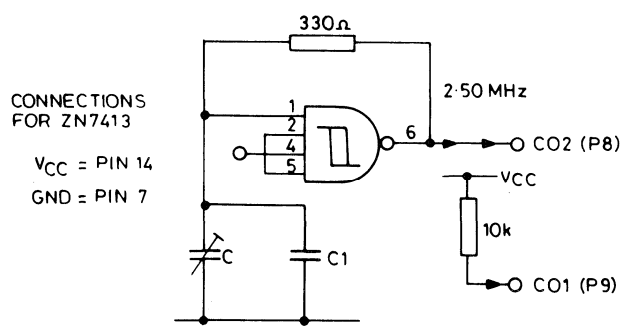
C_s is normally about 22pF

(b) If stability is not important, a capacitor may be used instead of the crystal.



$C_b \approx 15pF$

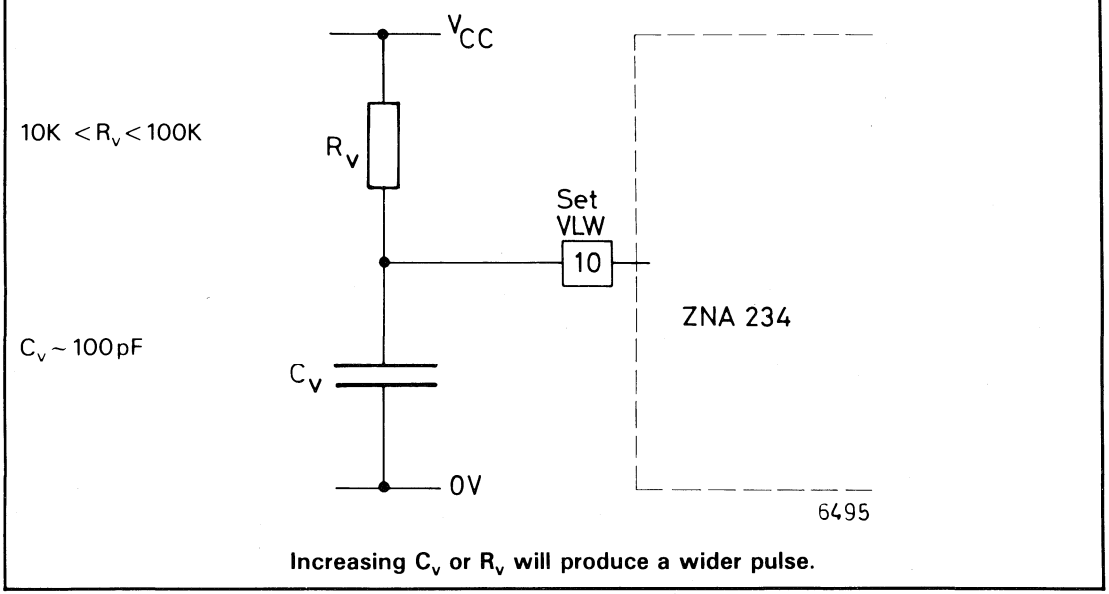
(c) Alternative oscillator circuits.



The external oscillator pulse width t_w, must be within the range shown in the table on page 2.

Vertical Line Width, Pin 10

Provision has been made for the width of the vertical lines to be varied if required. With pin 10 open circuit, the width of the vertical line pulses generated by the device is approximately 300ns. The pulse width may be varied from 100ns to 1μs by connecting a capacitor and resistor to pin 10 as shown below.



Increasing C_V or R_V will produce a wider pulse.

N.B. If pin 10 is left open circuit to give a 300ns pulse width, any external capacitance on the pin (e.g. from long lead or p.c.b track) will affect the timing. It is, therefore, recommended that if pin 10 is to be left open circuit then no connection at all is made to it.

Test Inputs, Pins 6 and 15

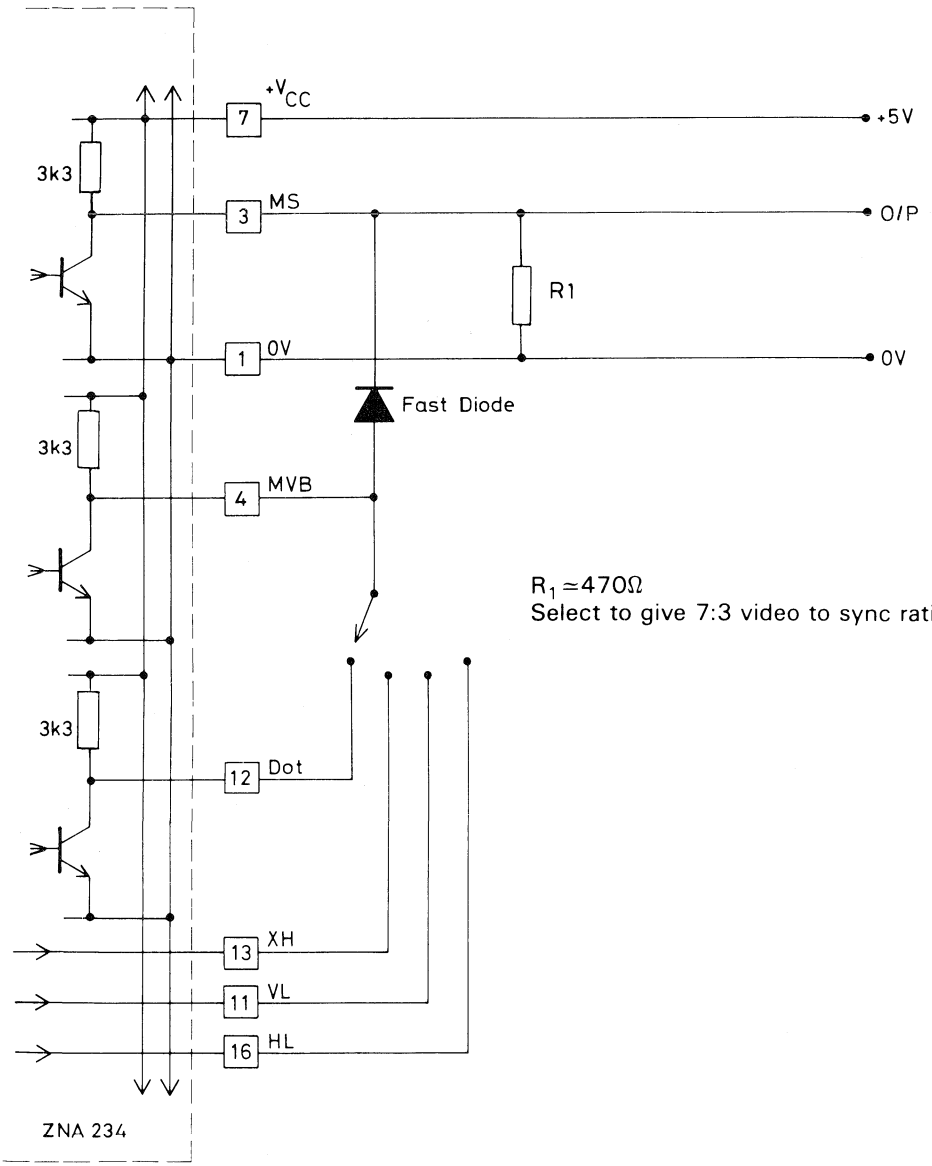
These should be connected to 0V.

Circuits for Video/Sync Mixer

The following two circuits on pages 10 and 11 for the video/sync mixer are suggested as starting points only. They have been found to work on the bench, but no detailed applications work has been carried out to date.

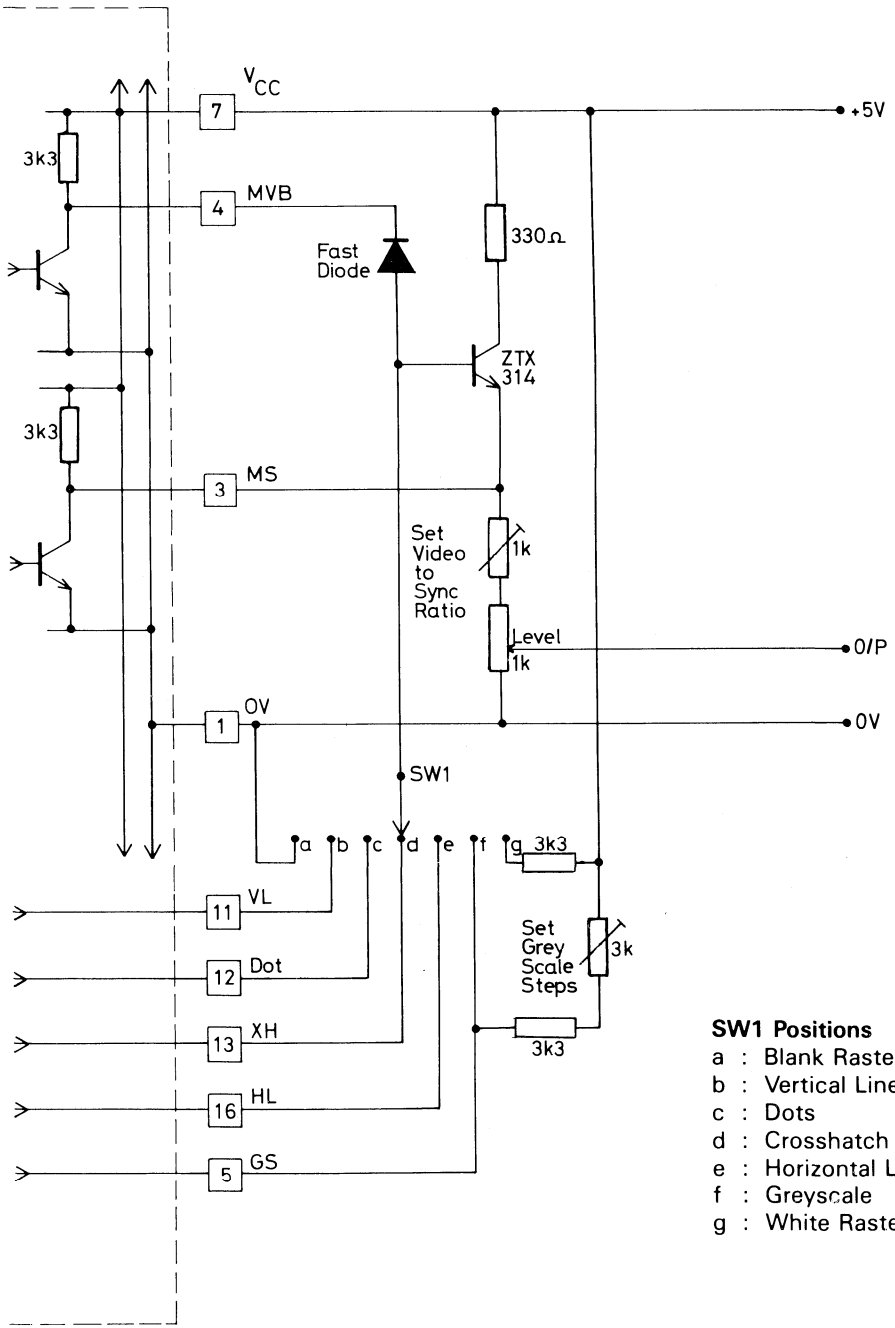
The circuit on page 10 is probably the simplest possible method, but it does have the disadvantage that the Greyscale output cannot be used owing to its different d.c. levels compared with the other video outputs. The second circuit, page 11, is hardly any more complex, and does allow the use of the Greyscale output.

SIMPLE CIRCUIT FOR VIDEO/SYNC MIXER (NO GREYSCALE)



$R_1 \simeq 470\Omega$
Select to give 7:3 video to sync ratio.

CIRCUIT FOR VIDEO/SYNC MIXER ALLOWING USE OF GREYSCALE



SW1 Positions

a : Blank Raster
b : Vertical Lines
c : Dots
d : Crosshatch
e : Horizontal Lines
f : Greyscale
g : White Raster

Section 5
Remote Control

2084-1.0

MV500

REMOTE CONTROL TRANSMITTER

Together with a simple low cost keypad, an infra-red diode and a transistor, the MV500 forms a complete transmitter for remote control data. The device uses pulse position modulation (PPM) without a carrier and is therefore best suited to infra-red or direct wire link applications. CMOS technology is used which allows low power battery operation down to 3V. One of three output data rates may be selected, all timing being derived from a low cost ceramic resonator. The MV500 may be used with the MV601 remote control receiver or decoded directly by a microprocessor.

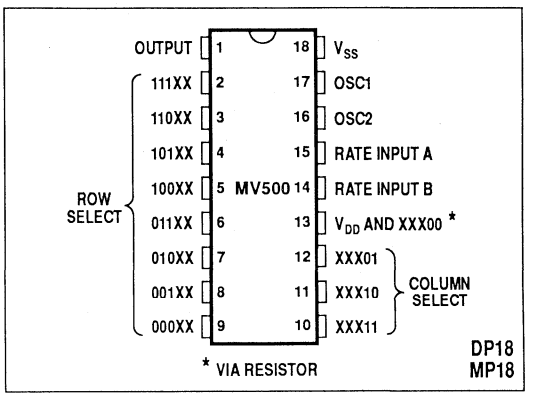


Fig.1 Pin connections - top view

FEATURES

- Very Low Power Requirements
- 3V to 9V Operation
- Low Cost Ceramic Resonator
- Selectable Data Rates
- Single Pole Key Matrix
- Few External Components
- Code Synchronising Pulses

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-0.5V to 11V
Input voltage (all pins)	-0.5V to V_{DD} +0.5V
Operating temperature range	0°C to +70°C
Storage temperature range	-55°C to +125°C

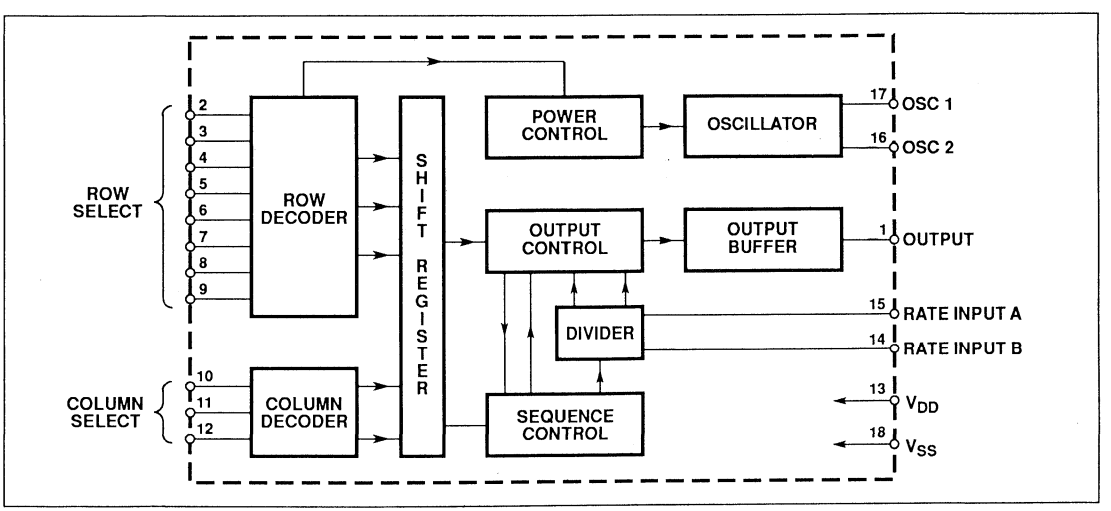


Fig.2 MV500 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{AMB} = 0°C to +70°C, V_{DD} = +3V to +10.5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply current	13		0.5	2	mA	See circuit, Fig. 4
Standby supply current	13		0.3	2	µA	All inputs open circuit, V_{DD} = 9V, T_{AMB} = +25°C
Output source current	1	50	100	200	mA	V_{DD} = 6V, V_{OH} = 1V
		10	25		mA	V_{DD} = 3V, V_{OH} = 1V
Keyboard contact resistance	2-12					
Closed		0		20	kΩ	
Open		100		∞	kΩ	
Oscillator frequency	16, 17	400		1000	kHz	

TIMING

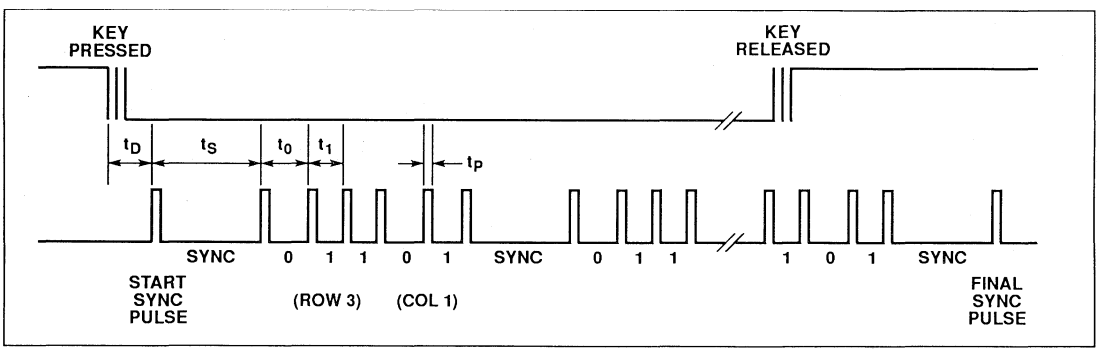


Fig.3 PPM data timing

Rate inputs		Rate value 'T' (clock cycles)
B	A	
0	0	Output inhibited
0	1	2048
1	0	1024
1	1	512

Table 1 Rate control

Delay time, t_D = 1024 clock cycles (min.)
Sync time, t_S = 6T (see Table 1)
Logic '0' time, t_0 = 3T
Logic '1' time, t_1 = 2T
Pulse width, t_P = 8 clock cycles

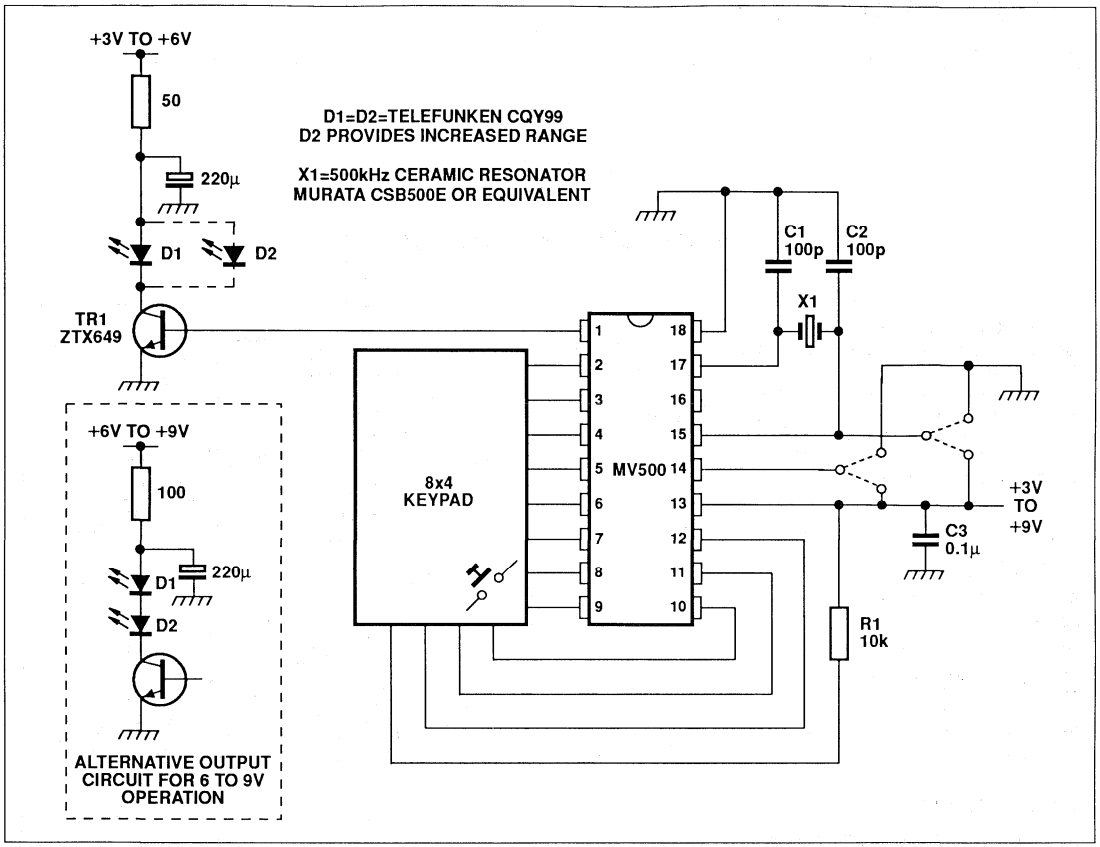


Fig.4 Infra-red application circuit

OPERATION

The circuit diagram of Fig. 4 shows a typical infra-red transmitter application. With no key pressed, the MV500 remains in its power-down mode, isolating the oscillator and most of the logic from the supply, thus minimising the drain on the battery. The output is held low.

The device may be activated in one of two ways:-

(a) one or both of the RATE inputs is held high, then a key switch is closed connecting any COLUMN to any ROW, or

(b) any COLUMN and ROW are connected, then one or both of the RATE inputs is taken high.

Once activated, power is applied to the rest of the device, the oscillator started and a delay imposed before any change at the output occurs. After this time, an initial sync pulse is transmitted, followed by the code word, which is repeated for as long as the key remains pressed. When the key is released, the word being transmitted is completed before the device enters its standby mode again.

Taking both RATE inputs low will also force the device into its power down state at the end of the current word. A final sync pulse is always added at the end of the last word to be transmitted (Fig. 3).

When the transmitter is operated from a supply between 6V and 9V, two infra-red LEDs may be used in series as shown inset in Fig. 4. At other voltages, consideration must be given to the arrangement of diodes used and a series resistance should be used to limit the diode current. It should be noted that using two diodes in parallel increases the current drawn from the battery at each pulse. A significant increase in range may be obtained by using a plated plastic parabolic reflector in conjunction with one or two diodes, rather than simply increasing the number or power of the diodes used.

Transistor TR1 should be chosen to have high current gain and fast switching speeds at the current levels relevant to the diode arrangement used.

MV601

REMOTE CONTROL RECEIVER

The MV601 is a remote control receiver designed to operate in conjunction with the MV500 transmitter. A five bit tristate binary output corresponding to the 32 codes available from the MV500 is provided together with data ready and output enable signals, allowing a simple interface to a microprocessor. A ceramic resonator and two rate inputs set the data rate to correspond to that produced by the MV500.

FEATURES

- High Noise Immunity
- 5V Operation
- Very Low Supply Current
- Momentary or Latched Operation
- Tri-State Outputs
- Ceramic Resonator and Data Rate Inputs to match MV500

APPLICATIONS

- Remote Control Interface to Microprocessor
- Industrial and Consumer Remote Control

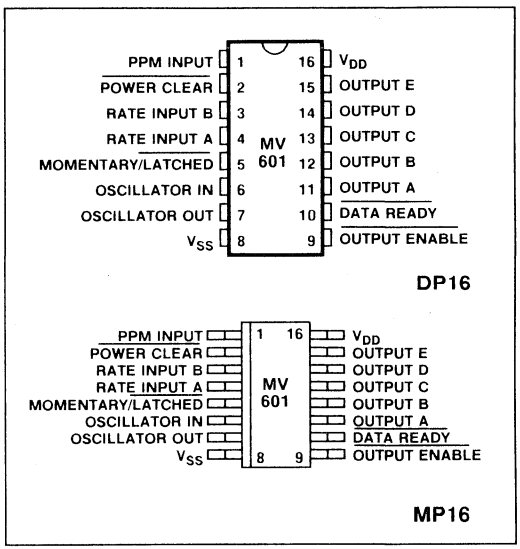


Fig 1 Pin connections - top view

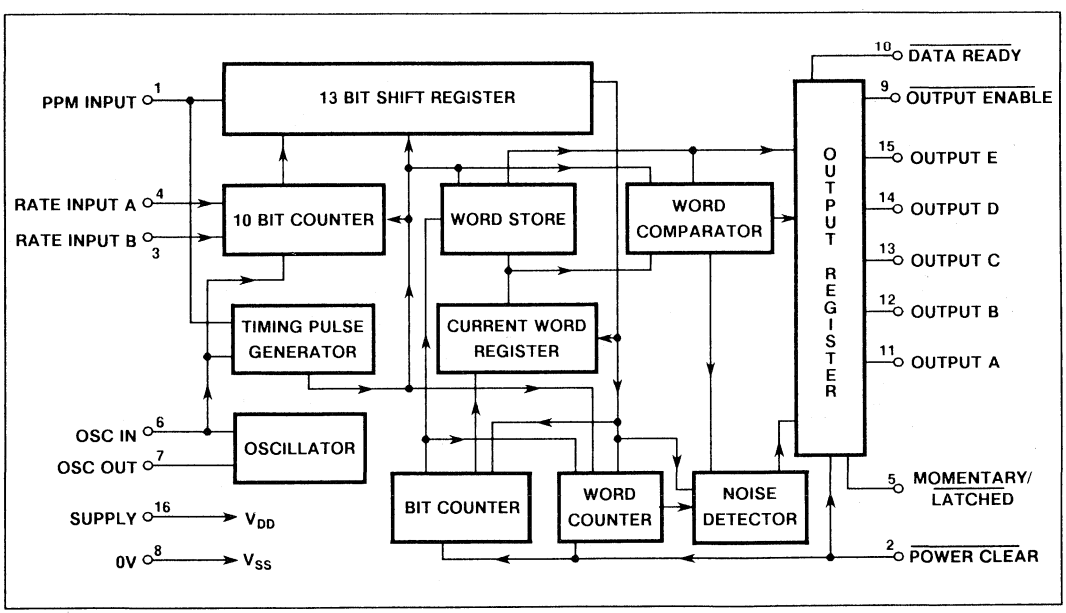


Fig.2 MV601 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0°C to 70°C, V_{DD} = +4.5V to +5.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Power supply current, I_{DD}	16		0.2	2.0	mA	
Oscillator frequency	6, 7			10	MHz	
INPUTS						
OSCIN, RATE A, RATE B,	6, 4, 3,					
MOM / $\overline{LAT}$, $\overline{OEN}$	5, 9					
Input low voltage (V_{IL})				V_{DD} / 3		
Input high voltage (V_{IH})		V_{DD} ×2/3				
PPM, $\overline{POWER\ CLEAR}$	1, 2					
Input low voltage (V_{IL})				1.0	V	V_{DD} = 5.0V
Input high voltage (V_{IH})		2.0			V	
Threshold voltage rising			1.85		V	
Threshold voltage falling			1.05		V	
$\overline{POWER\ CLEAR}$, RATE A, RATE B	2, 4, 3					
Input low current			-33	-100	μA	Nom. 150k pullup resistor
All other inputs except OSCIN Input current	1, 5, 9			±2.5	μA	V_{IN} = V_{SS} -0.3V to V_{DD} +0.3V
OSCIN	6					
Input current				±10	μA	V_{IN} = V_{SS} -0.3V to V_{DD} +0.3V
OUTPUTS						
A - E, $\overline{DATA\ READY}$						
Output low current (sink)		13	26		mA	V_{OL} = 0.4V
Output high current (source)		-21	-45		mA	V_{OH} = 2.4V
Output leakage current (A-E)				±10	μA	V_O V_{SS} -0.3 to V_{DD} + 0.3V pin 9 = V_{DD}
OSCOUT						
Output low voltage (sink)		1.0			mA	V_{IO} = 0.3V
Output high current (source)		-1.0			mA	V_{OH} = V_{DD} 0.3V

OPERATING NOTES

The MV601 is designed to operate in conjunction with the MV500 transmitter. When the rate inputs of MV500 and MV601 are programmed with the same binary input code and matched ceramic resonator frequencies are used (within 4%), the outputs of the MV601 will be set to the value of the PPM code transmitted. Two identical valid words must be received before an output response. A data ready signal, set after the output data has settled may be used to strobe data into an external register or generate an interrupt to a microprocessor.

When used in infra red systems, the PPM input will usually be derived from the output of an SL486 infra red amplifier, but direct connection to the transmitter is also possible. The PPM input is insensitive to pulse width.

The power clear input is generally connected to an external capacitor which holds the input momentarily low ensuring a reset of the outputs and internal logic at power on. The circuit can be reset at any time by taking the power clear input low.

The rate inputs have nominal 150kΩ pull up resistors and may therefore be left open circuit when a high input is required.

When more than 32 codes are required, the rate inputs on the MV500 transmitter can be switched and 2 or 3 MV601 circuits wired in parallel to the PPM signal. Only the MV601 with rate inputs identical to the transmitter will respond. An alternative method giving 64 possible codes from only one MV601 is shown in Fig. 7. The fastest and slowest rate settings from the transmitter should be used. In this circuit the three transistors produce a DC level dependent on the rate of the received PPM data. The DC level is used to provide the F output bit and to automatically switch the rate B input to the MV601 to correspond with the transmitter.

PIN FUNCTIONS

1. **PPM Input**
The serial PPM data is connected here. Pulse width is not critical but must remain high or low for at least one clock cycle.

2. **Power Clear**
A logic low resets the output register and internal logic ensuring full noise immunity from switch on. A capacitor to V_{SS} will normally be connected. A 150k (nom) resistor to V_{DD} is provided so that the input may be left open circuit if required.

3. **Rate Input B**
This input controls the received data rate according to table 1. Input state must match that on MV500. A 150k (nom) resistor pull up to V_{DD} is provided so that the input may be left open circuit if required.

4. **Rate Input A**
As pin 3.

5. **Momentary/Latched Input**
Controls the operational mode of the output register. When low, data will be retained at the output until updated by a newly validated code. When high, the data will only remain at the outputs whilst the valid code is present at the PPM input.

6. **Oscillator In**
The input to the oscillator circuit. A Pierce oscillator is formed by a ceramic resonator connected to pin 7 and capacitor connected to ground.

7. **Oscillator Out**
The output of the oscillator circuit. A capacitor connected to ground completes the Pierce oscillator circuit.

8. **V_{SS}**
The negative supply pin.

9. **Output Enable**
A logic low enables the A, B, C, D and E outputs. A logic high switches the output transistors off, providing a high impedance state.

10. **Data Ready**
Set low when valid data is present at the outputs.

11. **Output A**
Tri-state output set to the binary equivalent of the PPM input data.

12. **Output B**
As pin 11.

13. **Output C**
As pin 11.

14. **Output D**
As pin 11.

15. **Output E**
As pin 11.

16. **V_{DD}**
The positive supply pin.

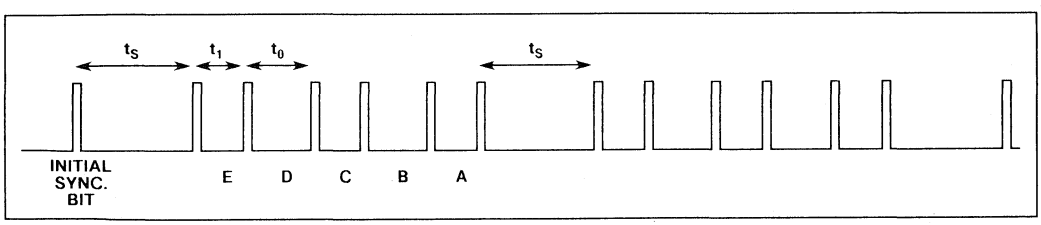


Fig.3 Typical Received PPM Data

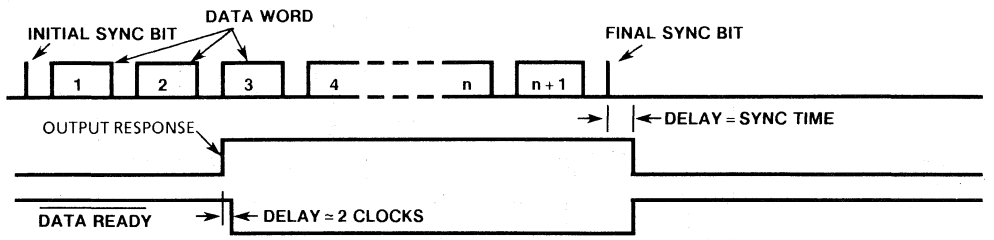
Rate inputs		Clock cycles		
B	A	t_1	t_0	t_S
0	0	NV	NV	NV
0	1	4096	6144	12288
1	0	2048	3072	6144
1	1	1024	1536	3072

Table 1 Rate control inputs

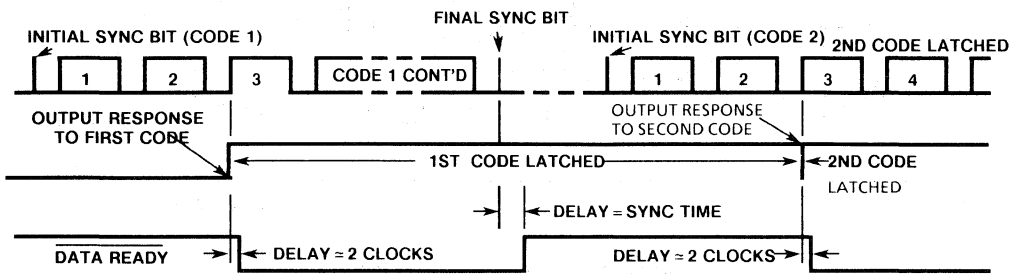
NV = Not Valid
NOTE: Rate inputs should match those on MV500

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD}	+7V
Input Voltage	V_{DD} + 0.3V to V_{SS}-0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to +125°C
Output Sink and Source Current	50mA
Humidity	85%



Timing diagram momentary mode



Timing diagram latched mode

Fig.4 Output timing

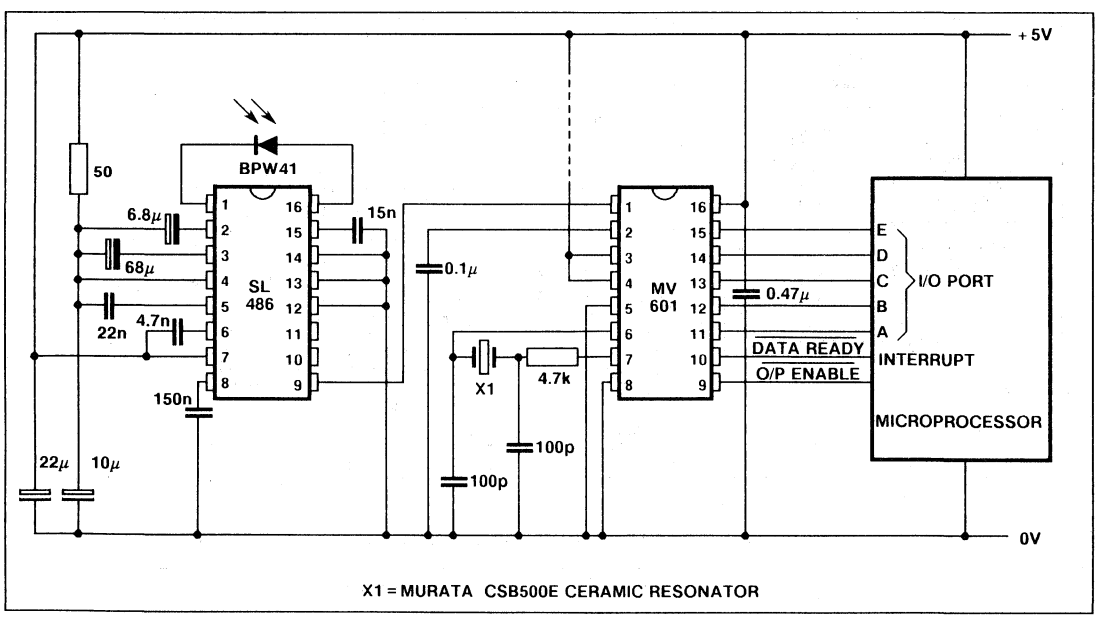


Fig.5 Interface to microprocessor and SL486 (latched mode)

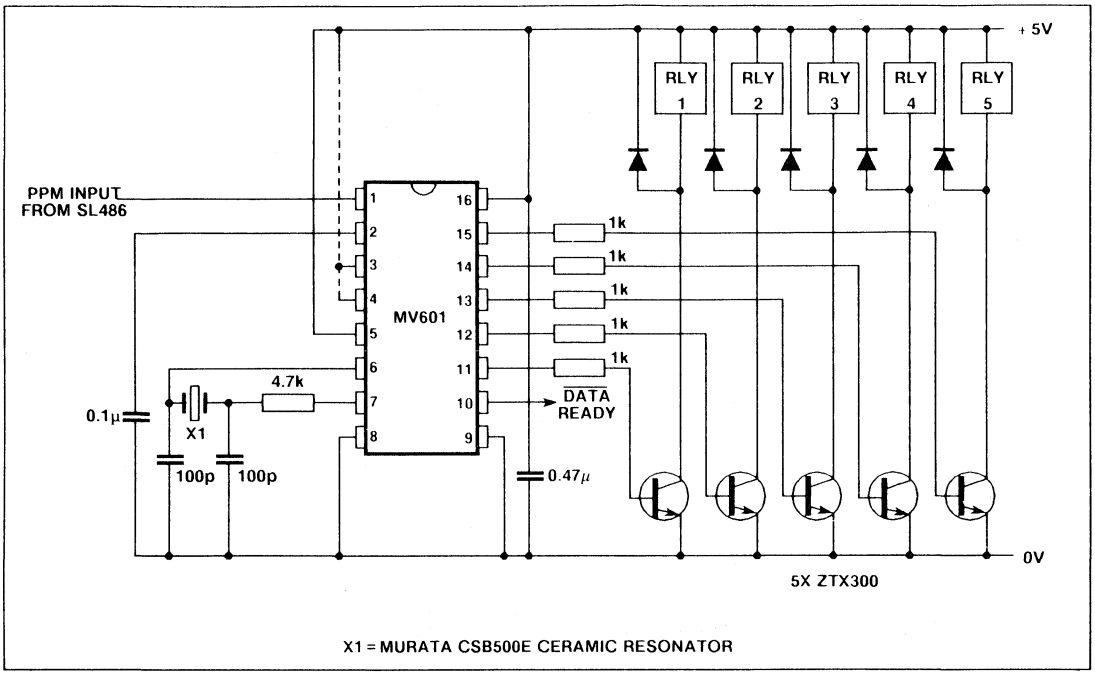


Fig.6 General purpose 5-function industrial remote control application (momentary mode)

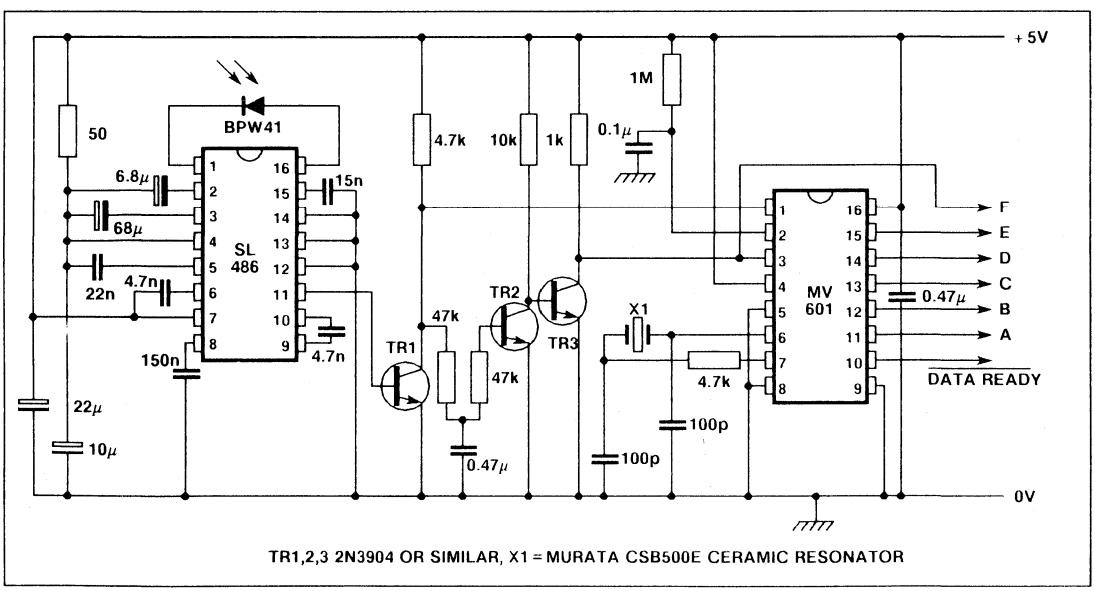


Fig.7 64-code application using a single MV601

MV2000

REMOTE KEYBOARD TRANSMITTER

The MV2000 is a fully integrated keyswitch encoder and pulse position modulation (PPM) transmitter, designed for the encoding of a keyboard with up to 88 switches.

Three seperate shift or control inputs are also provided to give up to eight functions for each keyswitch.

The PPM output may be used to drive an infra-red LED for remote keyboard operation or provide a simple direct wire link to a VDU.

The output codes are intended to be decoded directly by a microprocessor.

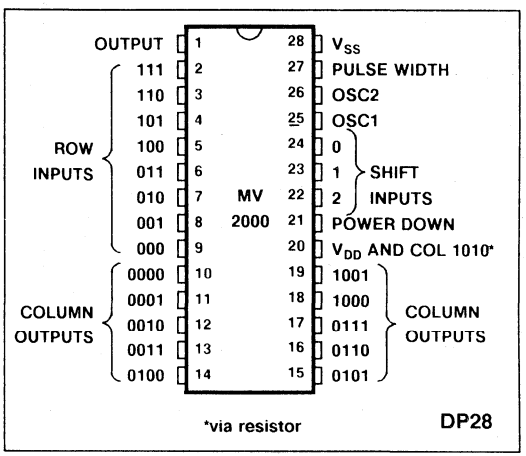


Fig 1 Pin connections (top view)

FEATURES

- Infra-red Transmission for Remote Operation
- Very Low Supply Current
- PPM Output gives Excellent Immunity from Noise and Multi-path Reflections
- Error Check Code for Data Integrity
- Few External Components

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-0.5V to 11V
Input voltage (all pins)	-0.5V to V_{DD} + 0.5V
Operating temperature range	0°C to + 70°C
Storage temperature range	-55°C to + 125°C

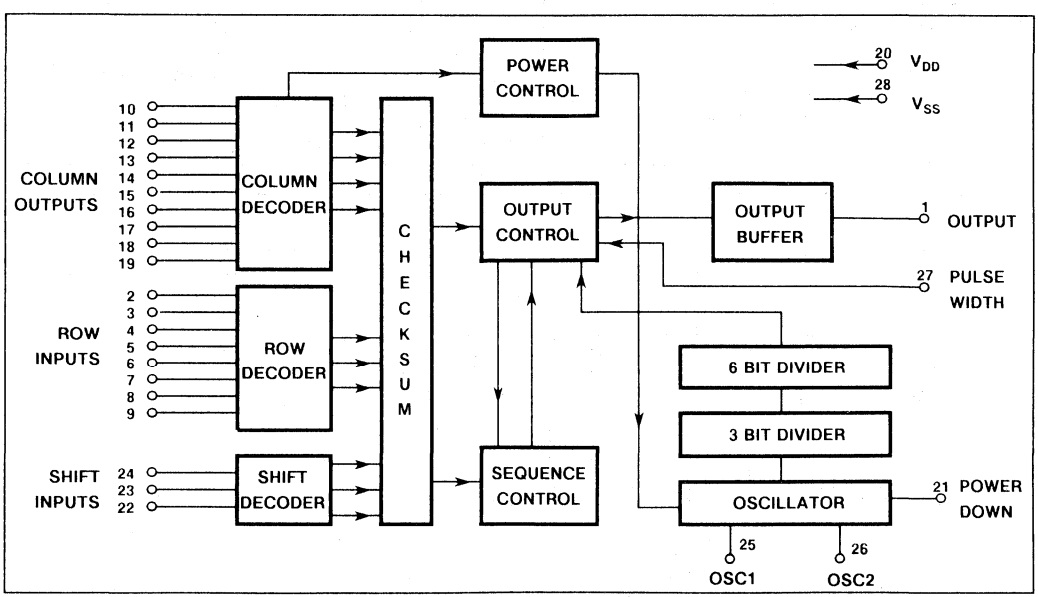


Fig MV2000 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0°C to 70°C, V_{DD} = +3V to +10.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Operating supply current	20		2.5	10	mA	Circuit Fig. 4
Standby supply current	20		0.1	2	μA	All inputs open circuit
Output source current	1	100	200	300	mA	V_{DD} = 9V, V_{OH} = 1V
		50	100	200	mA	V_{DD} = 6V, V_{OH} = 1V
Keyboard contact resistance	2-19					
Closed		0		20	kΩ	
Open		100		∞	kΩ	
Oscillator Frequency	25,26	200	500	4000	kHz	
				10	MHz	V_{DD} = 10.5V

PIN DESCRIPTIONS

Pin No.	Description
1	Totem pole output for driving NPN switching transistor
2-9	Keyboard matrix row inputs (7-0)
10-19	Keyboard matrix column outputs (0-9)
20	Positive supply, V_{DD}. Also column 10 via resistor
21	Power down input - normally held at V_{DD}. Taking this input low will force the device into its power down state

Pin No.	Description
22-24	Shift/Control inputs, may be pulled high or low by resistors or connected directly to V_{DD} or V_{SS}
25	Oscillator 1 - input to internally biased inverter. May be driven from external source
26	Oscillator 2 - output of internally biased inverter
27	Pulse Width input - time constant determines output pulse width
28	Negative supply, V_{SS}

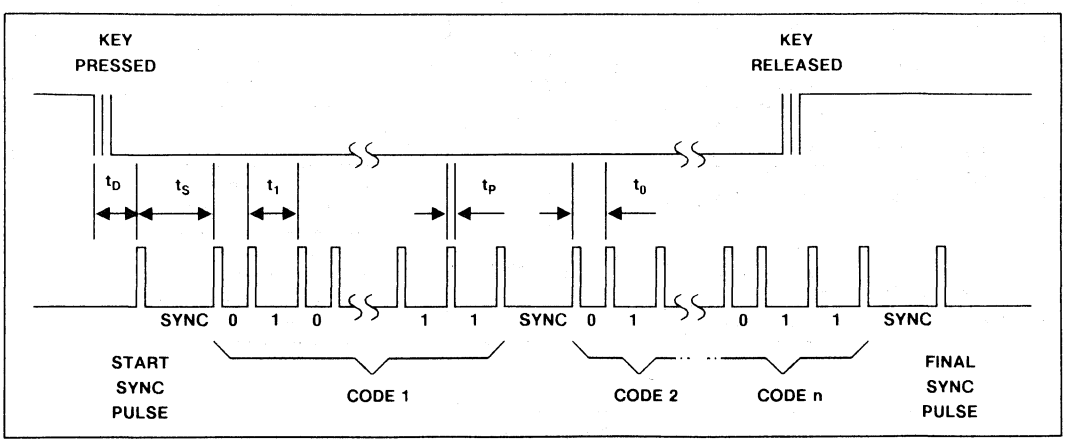


Fig. 3 PPM data timing

TIMING (see fig 3)

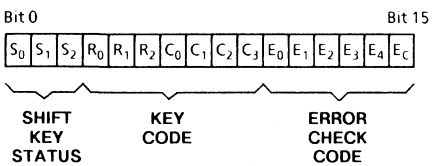
Delay time, t_d = 1024 clock cycles (min)
Sync time, t_s = 2560 clock cycles
Logic 0 time, t_0 = 1536 clock cycles
Logic 1 time, t_1 = 2048 clock cycles
Pulse time, t_p, determined by time constant on pin 27
Ratio $t_0:t_1:t_s$ = 3:4:5

CODE FORMAT

A sixteen bit code is output, consisting of a seven bit key code, three shift key status bits and a six bit error check code.

MSB LSB
Key Code = $C_3C_2C_1C_0\ R_2R_1R_0$
(COLUMN) (ROW)

Transmitted sequence:- (Bit 0 transmitted first)



The Error Check Code is obtained by first adding the two halves of the previous ten bits of the code (LSBs first) and then inverting the resultant 6-bit code (EC being the carry bit).

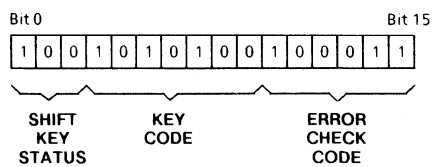
ie. $R_1\ R_0\ S_2\ S_1\ S_0$
$C_3\ C_2\ C_1\ C_0\ R_3$ +
$\overline{E_C}\ \overline{E_4}\ \overline{E_3}\ \overline{E_2}\ \overline{E_1}\ \overline{E_0}$

Example

Shift 0 input held at VDD
Shift 1 and 2 inputs held at VSS
Column 2 connected to Row 5

Key Code = 0 0 1 0 1 0 1
(COLUMN) (ROW)

Transmitted sequence:-



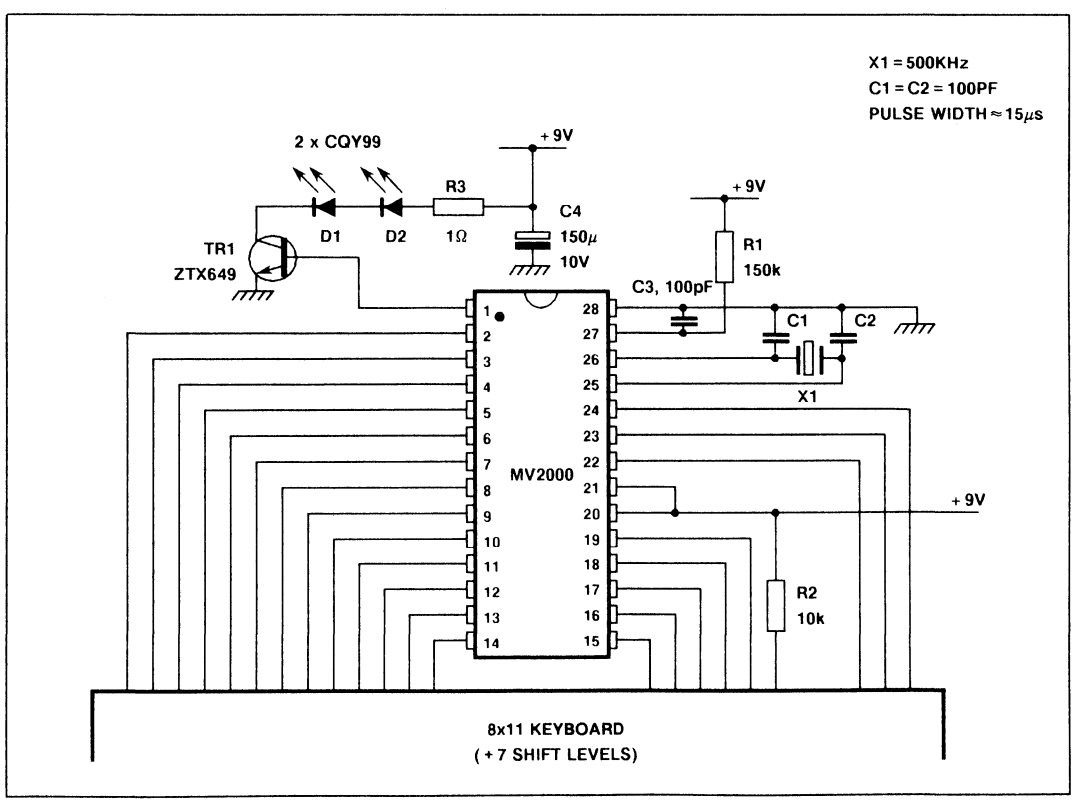


Fig. 4 Infra-red application circuit

OPERATION

The circuit diagram of Fig. 4 shows a typical application using the MV2000 with data being transmitted via an infra-red link. Until a key is pressed, the device remains in its standby mode with power internally disconnected from the oscillator and most of the logic to minimise the drain on the supply.

When a column and a row are connected by the pressing of a key, power is applied to the rest of the device, the oscillator started and a delay imposed before any change at the output occurs. After this time, an initial synchronising pulse is transmitted, followed by the code word, which is repeated, separated by sync bits, for as long as the key remains pressed (Fig. 3). When the key is released, the word being transmitted is completed. If another key is pressed, the code for this new key is transmitted immediately following the end of the code for the previous key, but separated from it by a sync bit.

If no other key is pressed, a final sync pulse is added to the end of the last word to be transmitted and the MV2000 then returns to its power down mode.

If more than one key is pressed at the same time, the code transmitted will be that corresponding to the first key detected in the matrix scan of the keyboard.

Pressing one or more of the "shift" keys on the keyboard in conjunction with another key changes the state of the corresponding shift bits in the code transmitted. Pressing a shift key on its own does not initiate a transmission.

In any design using the MV2000 for infra-red transmission, consideration must be given to the arrangement of diodes used, possibly using a small resistance in series to limit the current. The transistor TR1 must also be chosen such that its characteristics include high current gain and fast switching speeds.

3055-1.0

SL486

INFRA RED REMOTE CONTROL PREAMPLIFIER

The SL486 is a high gain preamplifier designed to form an interface between an infra-red receiving diode and the digital input of remote control receiving circuits. The device contains two other circuit elements, one to provide a stretched output pulse facility and a voltage regulator to allow operation from a wide range of supplies.

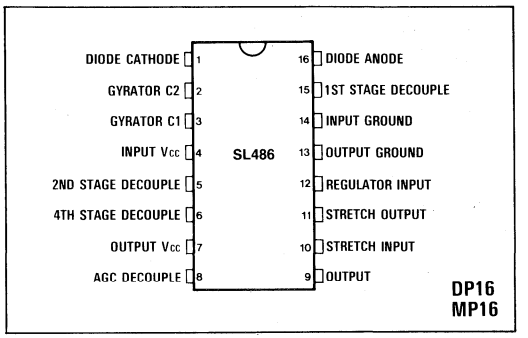


Fig.1 Pin connections (top view)

FEATURES

- Fast Acting AGC Improves Operation in Noisy Environments
- Differential Inputs Reduce Noise Pick-up and Improve Stability
- Gyrator Circuit Allows Operation in Environments with High Brightness Background Light Levels
- Output Pulse Stretcher for use with Microprocessor Decoders
- On-Chip Stabiliser Allows Operation with a Wide Range of Supply Voltages
- Low Noise Output

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V Pins 4 & 7)	+10V wrt V Pins 13 & 14
Regulator input voltage (V Pin 12)	-20V wrt V Pin 7
Output current	5mA
Stretch output current	5mA
Operating temperature range	0°C to +70°C
Storage temperature	-55°C to +125°C

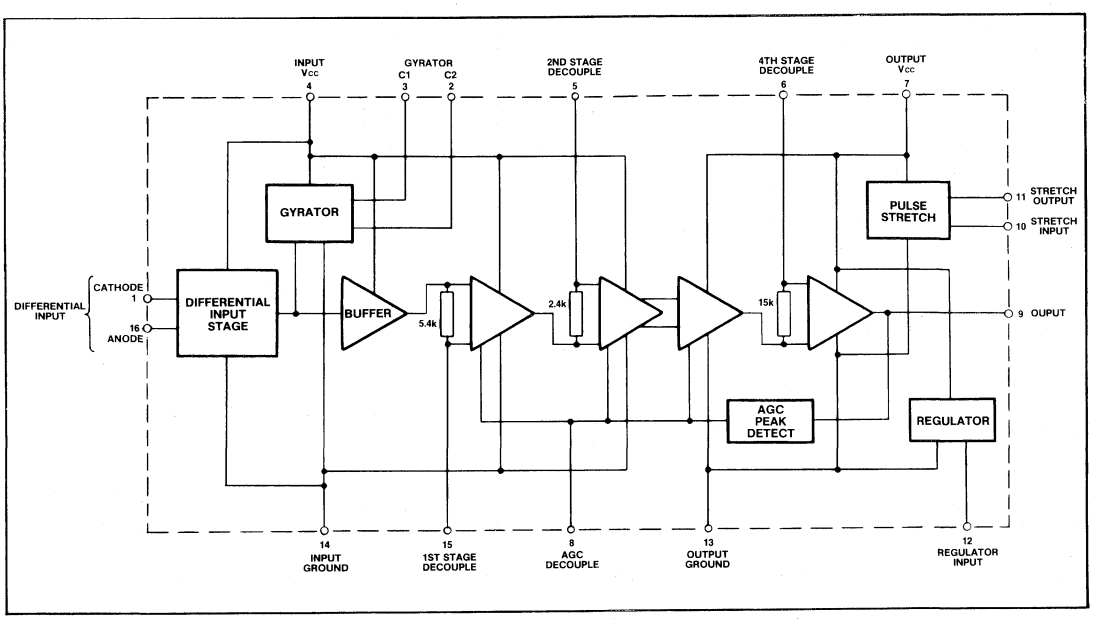


Fig.2 SL486 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25° C, V_{CC} = 4.5V to 7.0V

Characteristic	Pin	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply current (See Note 1)	4,7		6.5	9.0	mA	V_{CC} = 5.0V, I_{DIODE} = 1.0μA } Pins 13 & 14 ground
	4	3.5+3xI_D	4.2+3xI_D	5+3xI_D	mA	V_{CC} = 4.5V, $I_{DIODE} \leqslant$ 1.5mA } ground
	4,7		8.5	10	mA	V_{CC} = 18V, I_{DIODE} = 1.0μA Pin 12 ground
Low voltage supply (external)	4,7(+ve), 13,14(-ve)	4.5		9.5	V	Input and output V_{CC} commoned, input and output ground commoned
High voltage supply (external)	4,7(+ve), 12(-ve)	8.4		18.0	V	Input and output V_{CC} commoned, input and output ground at internal regulated voltage
Internal regulated voltage	13(wrt 7)	5.9	6.2	6.5	-V	V Pin 7(+) to V Pin 12(-) = +16V
Voltage between input and output V_{CC}	4,7			1.5	V	At room temperature
				1.1	V	At 70° C
Minimum sensitivity of differential input	1,16	9.0		2.3	nA	I_{DIODE} = 1.0μA
		74.0		18.5	nA	I_{DIODE} = 100μA
		168.0		42.0	nA	I_{DIODE} = 0.5mA
Common mode rejection	1,16		35.0		dB	
Maximum signal input	1,16	3.0	4.0		mA(peak)	
AGC range			68.0		dB	
Output and stretch output pull-up resistance (internal)	9,11		55.0		kΩ	At 25° C
Stretch output pulse width (T_P)	11		2.4		ms	Capacitance Pin 9 to Pin 10 = 10nF; $T_P \simeq$ -Rx C ln $\left\{\frac{1.5}{V_{CC}}\right\}$,
T co-efficient on Rx			0.7		%/° C	Where Rx = 200kΩ ± 25 % (internal resistance)
Output low	9			Output ground +0.35	V	0.2mA Sink, max.
Output high	9	Output V_{CC} -0.5			V	5μA Source
Stretch output low	11			Output ground +0.5	V	1.6mA Sink, max.
Stretch output high	11	Output V_{CC} -0.1			V	Output open circuit 5μA Source
Supply rejection, input V_{CC}	4		1.5		V(peak)	Ripple amplitude at 100Hz, Pin 12 ground
			0.8		V(peak)	Ripple amplitude at 100Hz, Pins 13 & 14 ground

NOTE
1. I_D = I_{DIODE} = IR diode forward current

APPLICATION NOTES - REFER TO FIGURE 4

Diode Anode and Cathode (Pins 1 and 16) The infra-red receiving diode is connected between pins 1 and 16. The input circuit is configured so as to reject signals common to both pins. This improves the stability of the device, and greatly reduces the sensitivity to radiated electrical noise. The diode is reverse biased by a nominal 0.65V.

Gyrator C2 and C1 (Pins 2 and 3) The decoupling, provided by gyrator C2 and C1, rolls off the gain of the feedback loop which balances the DC component of the infra-red diode current. The values of C2 and C1 are chosen to produce a low frequency cut-off characteristic below a nominal 2kHz. Hence, the gyrator produces approximately 20dB rejection at 100Hz.

The gyrator consists of two feedback loops operating in tandem. Only one feedback path is functional when the DC component of the diode current is less than 200μA. This loop is decoupled by gyrator C2. For diode currents between 200μA and 1.5mA the second control loop is operative, and this is decoupled by gyrator C1.

The decoupling capacitors, gyrator C2 and C1, must be connected between pins 2 and 3, to pin 4. The series impedance of C2 and C1 should be kept to a minimum.

First Stage Decouple (Pin 15) The capacitor on pin 15 decouples the signal from the non-inverting input of the first difference amplifier (see also Figure 2). The capacitance of 15nF is chosen to produce a 2kHz low frequency roll-off.

The capacitor must be connected between pins 15 and 14 (the input ground).

Second Stage Decouple (Pin 5) The capacitor on pin 5 decouples the signal from the non-inverting input of the second difference amplifier. The capacitance of 33nF is chosen to produce a 2kHz low frequency roll-off. The capacitor must be connected between pins 5 and 4 (the input V_{CC}).

Fourth Stage Decouple (Pin 6) The capacitor on pin 6 decouples the signal from the non-inverting input of the fourth difference amplifier. The capacitance of 4.7nF is chosen to produce a 2kHz low frequency roll-off. The capacitor must be connected between pins 6 and 7 (the output V_{CC}).

AGC Decouple/Delay Adjust (Pin 8) The output of the fourth difference amplifier is followed by a peak detector, which is used to provide an AGC control level. This produces a current source which is limited to 10mA at pin 8. The AGC decouple capacitor (C5 normally 150nF) filters the pulsed input, and the resultant level controls the gain of the first three difference amplifiers.

The AGC control level exhibits a fast attack/slow decay characteristic. Immediately infra-red pulses are detected, the gain will be reduced, so that any weaker noise pulses that are also received will not be seen at the output. Thus, provided the infra-red pulses are the most intense, it is possible to receive data in noisy environments. The slow decay keeps the AGC level intact during data reception, and produces a delay before any received noise may become present at the output, when transmission ceases.

Output (Pin 9) The output will be low, pulsing high with a source impedance of a nominal 55kΩ, for a received infra-red pulse. It is a linear amplification of the input and swings between output ground and output V_{CC}.

Stretch Input and Stretch Output (Pins 10 and 11) A typical infra-red PPM system transmits very narrow pulses. The duration of these pulses is typically 15μs, so in order to utilise a microprocessor based decoder system it is necessary to lengthen the received pulse. This stretched output can be obtained from pin 11 when a capacitor is connected between pins 9 and 10.

The width of the pulse is determined by the value of this coupling capacitor (C8 in Figure 3) and is given by:

$$T_p = -Rx\,C_8 \ln\left\{\frac{1.5}{(V_4 - V_{13})}\right\}$$

where T_p = pulse width in ms
Rx = 200kΩ (see electrical characteristics)
C_8 = coupling capacitance
and $(V_4 - V_{13})$ = potential between input V_{CC} and ground (pins 13 and 14)

The stretch output is normally high pulsing low for a received infra-red pulse, and swings between output V_{CC} and output ground.

Regulator Input (Pin 12) The device can be operated with supplies of between 4.5V and 9.0V connected between input/output ground (pins 14 and 13) and input and output V_{CC} (pins 4 and 7) as shown in Figure 3.

The device can be operated with supplies in excess of 9.0V by utilising the on-chip regulator. In this case connections are made between output V_{CC} (pin 7) and the regulator input (pin 12) as shown in Figure 4. A supply voltage of between 9.0V and 18V will then cause the output ground to be regulated at a level nominally 6.4V below the output V_{CC} (pin 7).

The regulator will, however, lose control with a potential difference of less than 9.0V. Below this level the voltage on pin 13 will track nominally 1.5V above the level of pin 12.

When the regulator is not used (low voltage operation), pin 12 must be shorted to output ground (pin 13).

OPERATING NOTES - REFER TO FIGURES 3 AND 4

Gyrator C1 (Pin 3) If the environment in which the device is operating, limits the background light such that the DC component of the diode current has a maximum of 200μA, it may be desirable to omit (see Figure 3) the more bulky and costly 68μF capacitor, gyrator C1 shown in Figure 4. In this case pin 3 can be left open circuit. The resultant application will then have a characteristic of greatly reduced gain when the ambient light causes the DC current to rise above this threshold.

The 68μF capacitor can alternatively be replaced by a resistor. The outcome of this is to further reduce the gain in ambient light levels above the 200μA threshold. Below this threshold the overall gain is slightly enhanced as the light level approaches the threshold value. If chosen this resistance should lie between 10kΩ and 200kΩ.

Noise Immunity The stretch output can also be used as a means of improving performance relating to a receiver system, over and above its main purpose of providing a stretched output facility. Including C8 (Figure 4) causes the output pulses (from pin 9) to be subjected to the stretch input threshold. Thus any noise pulses from pin 9 that are below this threshold will not be seen at the stretch output (pin 11).

A further improvement can be made, utilising this stretch input threshold by including some additional filtering of the output (C10 in Figure 4). This can be adjusted in value (typically 100pF) to reduce some of the noise pulses that otherwise cross the threshold, to a level below the threshold.

It must be noted that the stretch output logic sense is inverse (for microprocessor applications) from that of the output (pin 9), and the cost of re-inversion may be deemed uneconomical for the improvements gained.

Screening Use of screening for the device, and associated components, improves the performance and immunity to externally radiated noise. The screening method used must protect the sensitive front-end of the device; provided that

the diode, pin 1, pin 16, C2 (pin 2) and the first stage decouple (pin 15) are screened, it may be found that for the application considered, the remaining circuitry need not be so protected.

In applications where externally radiated noise is minimal, it may be possible to reduce any screening to pins 1 and 16, and the diode connections, only. In some instances, no screening may be necessary, but this largely depends on the level of radiated noise, the decoupling/filtering employed and the receivers decoding technique.

Decoupling Typical decoupling arrangements for use with or without the regulator, are given in Figures 4 and 3 respectively. When using the regulator, further improvements in high frequency supply rejection are possible by the inclusion of R2. The value can be chosen so as to keep the pin 12 end of R2 within the -9.0 to -18V (w.r.t. pin 7) specified voltage range. For example if using the 920 series remote control receivers, on a supply of 16V, a typical value for R2 would be 200Ω.

Note that the regulator is a low impedance point between pins 12 and 13. C7 thus maintains a low impedance path between pins 4 and 12 at high frequencies.

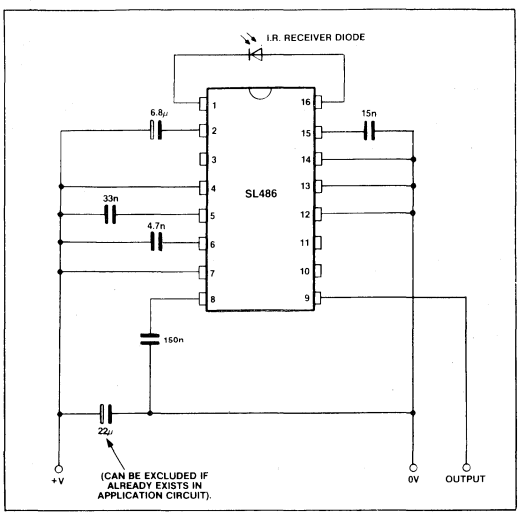


Fig.3 Circuit diagram of minimum component application (showing low voltage operation)

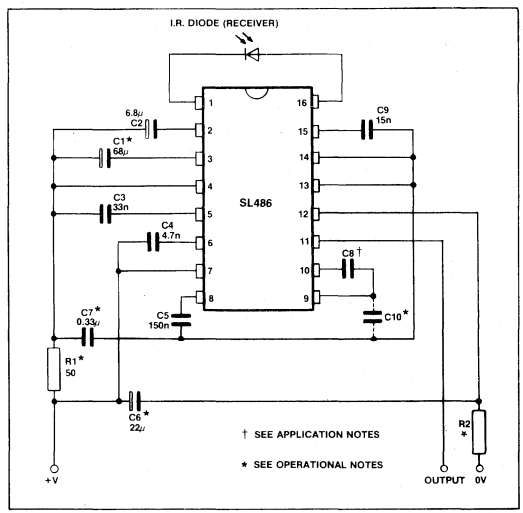
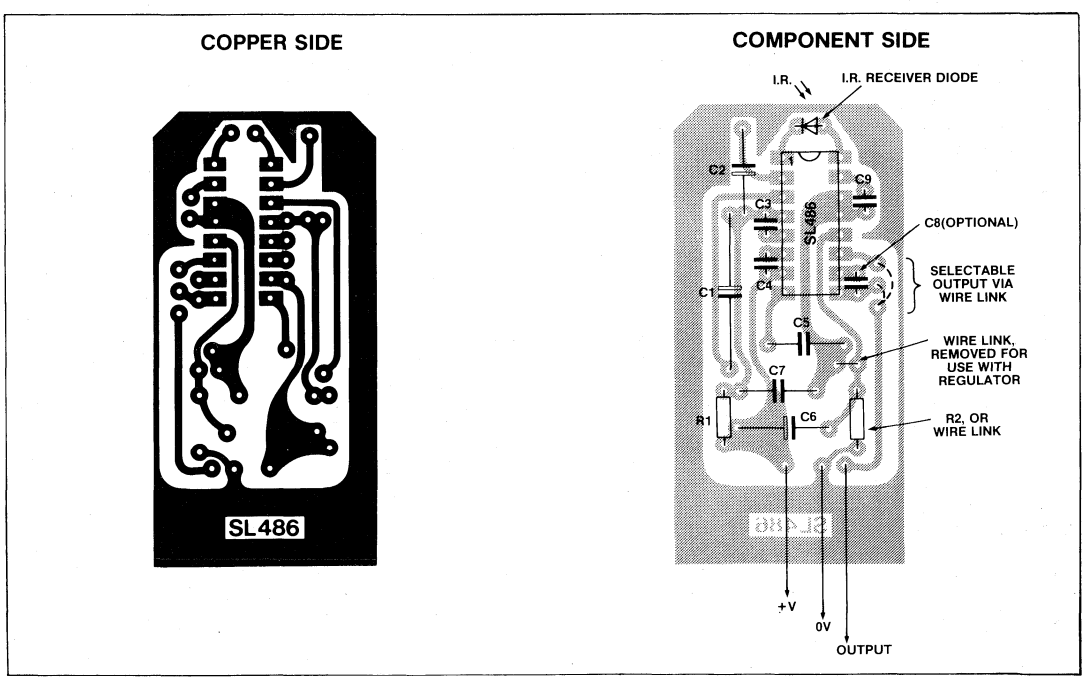


Fig.4 SL486 application diagram showing all optional circuitry (Note: Supply decoupling and connections for use of voltage regulator; also pulse stretched output)



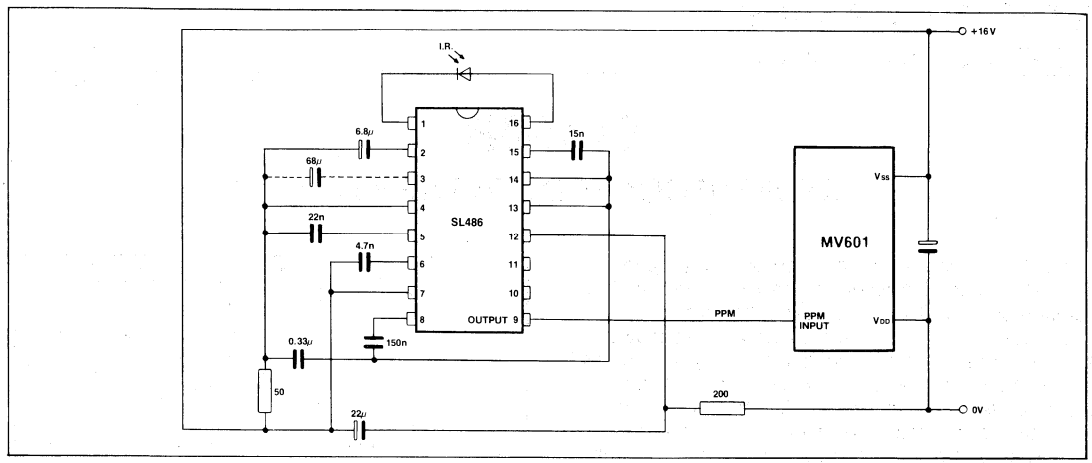


Fig.6 Application diagram for use with the MV601 remote control receiver, utilising on-chip supply stabiliser

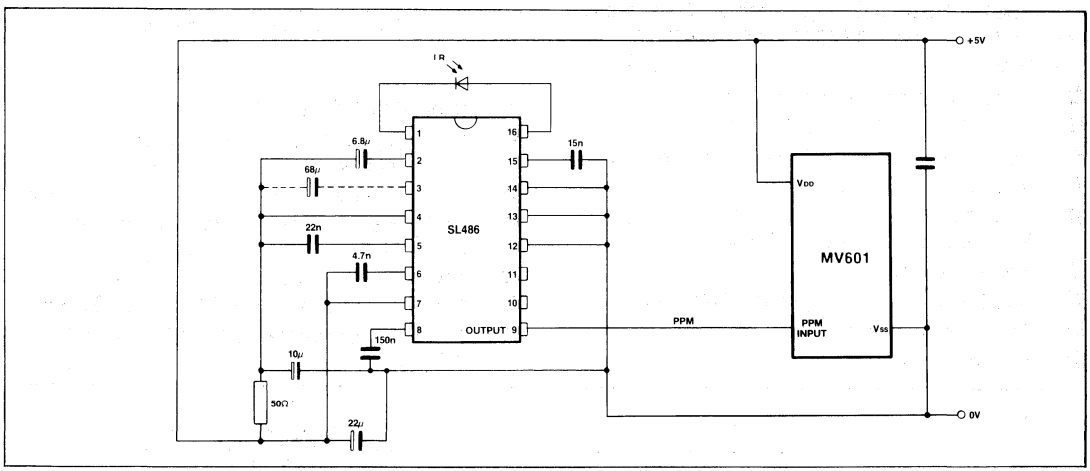


Fig.7 Circuit diagram of interface with MV601 remote control receiver

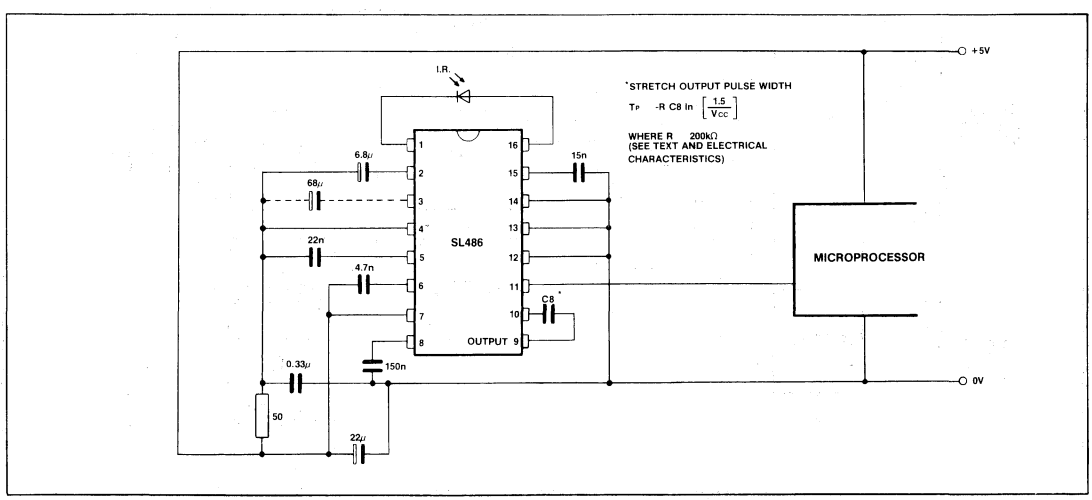


Fig.8 Circuit diagram of microprocessor interface, utilising on-chip pulse stretching facility

3056-1.0

SL490B

REMOTE CONTROL TRANSMITTER

GPS has developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra-red transmission, cable, radio or telephone links may also be used. Pulse Position Modulation (PPM) is used with or without carrier and automatic error detection is incorporated. Initially designed with TV remote control in mind, the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The SL490B is an easily extendable, 32-command, PPM transmitter drawing negligible standy current.

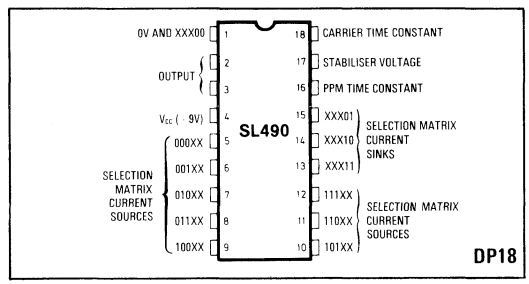


Fig.1 Pin connections - top view

FEATURES

- Ultrasonic or Infra-red Transmission
- Direct Drive for Ultrasonic Transducer
- Direct Drive of Visible LED when using Infra-red
- Very Low Power Requirements
- Pulse Position Modulation gives Excellent Immunity from Noise and Multipath Reflections
- Single Pole Key Matrix
- Switch Resistance up to 1kohms Tolerated
- Few External Components
- Anti-bounce Circuitry On Chip

QUICK REFERENCE DATA

- Power Supply: 9V, Standby 6microamps, Operating 8mA
- Modulation: Pulse Position with or without Carrier
- Coding: 5 Bit Word giving a Primary Command Set of 32 Commands
- Key Entry: 8 x 4 Single Pole Key Matrix
- Data Rate: Selectable 1 Bit/Sec to 10k Bit/Sec.
- Carrier Frequency: Selectable 0Hz (No Carrier) to 200kHz

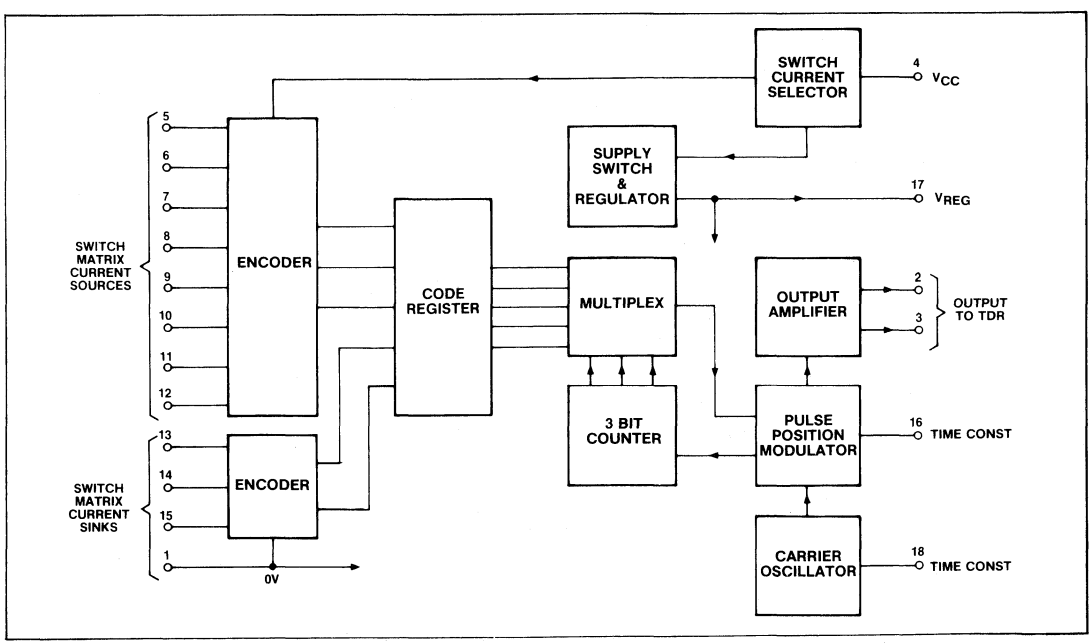


Fig.2 SL490B transmitter block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 25° C V_{CC} = +7V to +10.5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply current	4		9.5	16	mA	V_{CC} = 9.5V
Standby supply current	4			10	μA	
Stabilised voltage	17	4.1		4.9	V	
Output current available from stabilised supply	17			1	mA	
Output voltage swing	2,3	V_{CC} -1			V	Unloaded
Output voltage	2			1	V	I_2 = 10mA } Peak value < 1ms
Output voltage	3			1	V	I_3 = 5mA }
External switch resistance	5-15			5	kΩ	
External carrier resistor R2	18	20	40	80	kΩ	C2 = 680pF fc = 40kHz
t_1 deviation from calculated value	2,3			±10	%	R1 = 15k } t_1 = 0.95 C1 R1
using fixed timing components	2,3			±10	%	R1 = 60k } See Fig.4
PPM resistor	16	15	30	60	kΩ	
Variation of t_1 and t_0 with V_{CC} t_1 with V_{CC} = 7V/t_1 with V_{CC} = 10.5V	2,3			±4	%	
t_0 with V_{CC} = 7V/t_0 with V_{CC} = 10.5V	2,3			±4	%	
Ratio t_0/t_1	2,3	1.4		1.6		
Pulse width t_p	2,3	0.11 t_1		0.22 t_1		
Interword gap	2,3		3			The interword gap is 3 times t_1 derived by counting

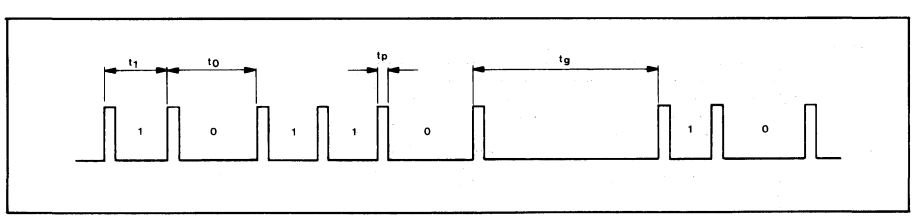


Fig.3 PPM word notation

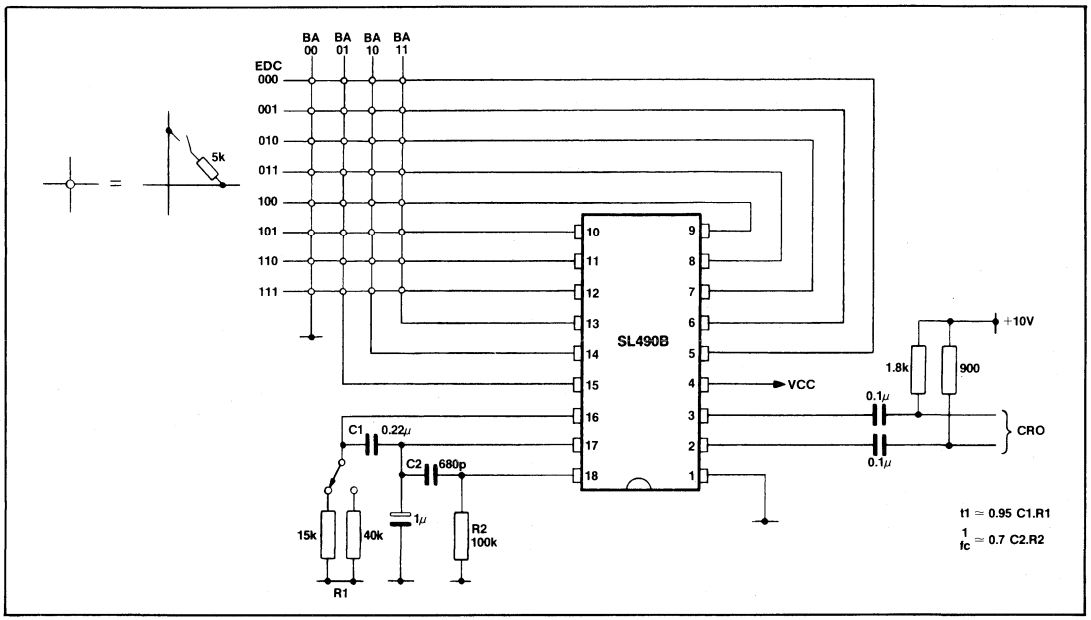


Fig.4 Test circuit

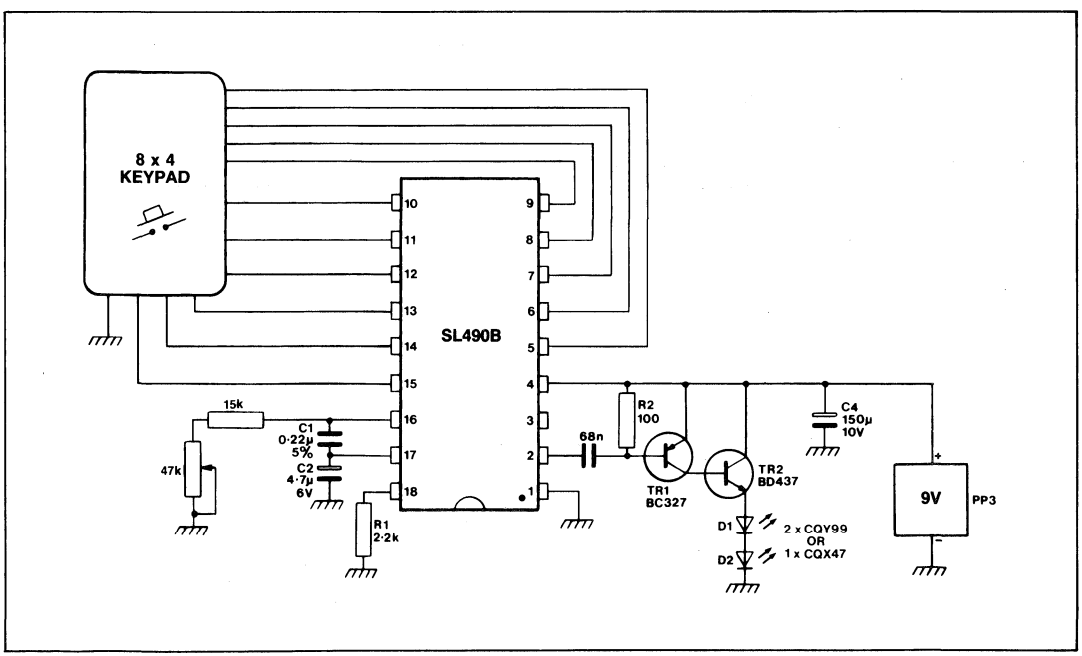


Fig.5 Infra-red application circuit

OPERATING NOTES

Fig.5 shows the circuit for a simple infra-red transmitter where the PPM output from pin 2 of the SL490B is fed to the base of the PNP transmitter TR1, producing an amplified current pulse about 15μsec wide. This pulse is further amplified by TR2 and applied to the infra-red diodes D1 and D2.

The current in the diodes and the infra-red output is controlled by the quantity, type, and connection method of the diodes and also by the gain at high currents of the transistors.

The most common solution where cost is important is to use 2 single-chip diodes, such as the CQY99 connected in series.

Improved output can be obtained by using four CQY99 diodes in a series parallel arrangement, but it is usually simpler to use 2 multichip diodes such as the CQX47 connected in parallel or a single CQX19 which gives similar results.

A significant increase in range can be obtained by using diodes such as the CQY99 in conjunction with a plated plastic parabolic reflector.

When building the transmitter, care should be taken with the choice of the capacitor C4 and with the circuit layout, particularly when multi-chip diodes are being used, as the current pulses can be as high as 6 to 8Amps.

Transistor choice is also important and any substitutes should have high current gain characteristics and switching speeds similar to those specified in Fig.3.

An increase in output can be obtained by connecting TR2 in common emitter configuration, but care should be taken not to exceed the rating of the diodes.

Choice of PPM Frequencies

When the transmitter is being used with an infra-red link, with high current pulses fed to the diodes as in Fig.5, power consumption will increase with frequency. It is thus advisable that with a battery power supply, the slowest PPM rate consistent with adequate response time should be chosen.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7V to 9.5V
Total power dissipation	600mW
Operating temperature range	-10°C to +60°C
Storage temperature range	-55°C to +125°C

Section 6
PWM Waveform Generators

C10402FDS-1.1

MA818

THREE-PHASE PULSE WIDTH MODULATION WAVEFORM GENERATOR

The MA818 PWM generator has been designed to provide waveforms for the control of variable speed AC machines, uninterruptible power supplies and other forms of power electronic devices which require pulse width modulation as a means of efficient power control.

The six TTL level PWM outputs (Fig.2) control the six switches in a three-phase inverter bridge. This is usually via an external isolation and amplification stage.

Rotational frequency is defined to 12 bits for high accuracy and a zero setting is included in order to implement DC-injection braking with no software overhead. Any power waveform can be implemented as this is user-defined in the external ROM/EPROM. For users requiring an on-chip pre-programmed waveform, the functionally identical MA828 is recommended.

Information contained within the pulse width modulated sequences controls the shape, power frequency, amplitude, and rotational direction (as defined by the red-yellow-blue phase sequence) of the output waveform. Parameters such as the carrier frequency, minimum pulse width, and pulse delay time may be defined during the initialisation of the device. The pulse delay time (underlap) controls the delay between turning on and off the two power switches in each output phase of the inverter bridge, in order to accomodate variations in the turn-on and turn-off times of families of power devices.

The MA818 is easily controlled by a microprocessor and its fully-digital generation of PWM waveforms gives unprecedented accuracy and temperature stability. Precision pulse shaping capability allows optimum efficiency with any power circuitry. The device operates as a stand-alone microprocessor peripheral, reading the power waveform directly from a PROM/EPROM and requiring microprocessor intervention only when operating parameters need to be changed.

An 8-bit multiplexed data bus is used to receive addresses and data from the microprocessor/controller. This is a standard MOTEL™ bus, compatible with most microprocessors/controllers.

The MA818 is fabricated in CMOS for low power consumption.

FEATURES

- Fully Digital Operation
- Interfaces with most Microprocessors
- Wide Power-Frequency Range
- Carrier Frequency Selectable up to 24kHz
- Waveform Stored in External ROM/EPROM
- Double Edged Regular Sampling
- Selectable Minimum Pulse Width and Underlap Time
- DC Injection Braking

MOTEL is a registered trademark of Intel corp. and Motorola corp.

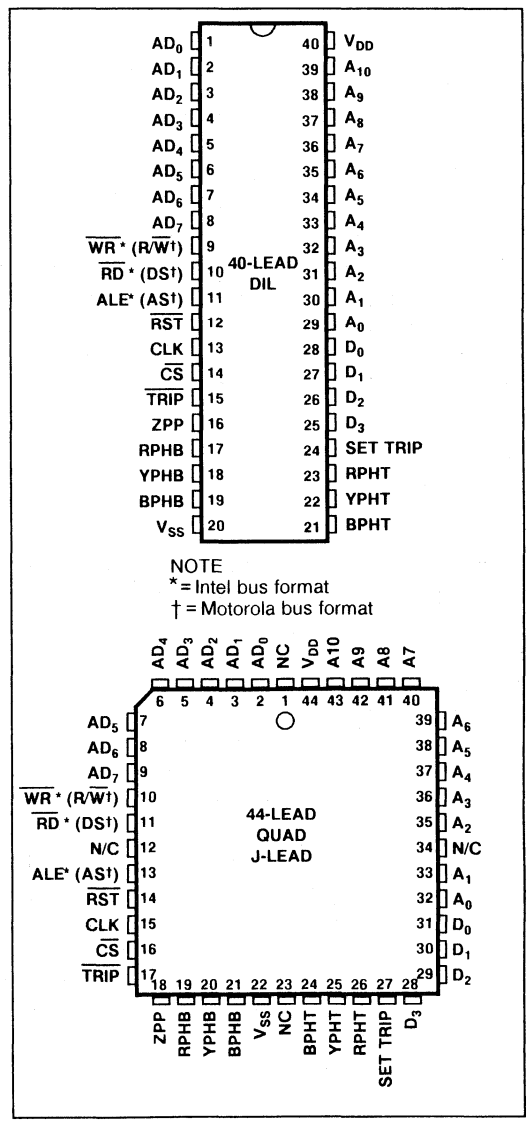


Fig.1 Pin connections - top view (not to scale)

PIN DESCRIPTIONS

40 Lead DIL Pin no.	44 Lead Quad Pin no.	Name	Type	Function
1	2	AD_0	I	Multiplexed Address/Data (LSB)
2	3	AD_1	I	Multiplexed Address/Data
3	4	AD_2	I	Multiplexed Address/Data
4	5	AD_3	I	Multiplexed Address/Data
5	6	AD_4	I	Multiplexed Address/Data
6	7	AD_5	I	Multiplexed Address/Data
7	8	AD_6	I	Multiplexed Address/Data
8	9	AD_7	I	Multiplexed Address/Data (MSB)
9	10	INTEL: $\overline{WR}$ MOTOROLA: R/$\overline{W}$	I	Bus control INTEL Write Strobe MOTOROLA Read/Write Select
10	11	INTEL: $\overline{RD}$ MOTOROLA: DS	I	Bus control INTEL Read Strobe MOTOROLA Data Strobe
11	13	INTEL: ALE MOTOROLA: AS	I	Bus control INTEL Address Latch Enable MOTOROLA Address Strobe
12	14	$\overline{RST}$	I	Resets Internal Counters
13	15	CLK	I	Clock Input
14	16	$\overline{CS}$	I	Chip Select Input
15	17	$\overline{TRIP}$	O	Output Trip Status
16	18	ZPP	O	Zero Phase Pulse
17	19	RPHB	O	Red Phase (Bottom power switch)
18	20	YPHB	O	Yellow Phase (Bottom power switch)
19	21	BPHB	O	Blue Phase (Bottom power switch)
20	22	V_{SS}	I	Negative power supply (0V)
21	24	BPHT	O	Blue Phase (Top power switch)
22	25	YPHT	O	Yellow Phase (Top power switch)
23	26	RPHT	O	Red Phase (Top power switch)
24	27	SET TRIP	I	Set Output Trip. 90kΩ internal pull-up resistor.
25	28	D_3	I	Eprom Data (MSB)
26	29	D_2	I	Eprom Data
27	30	D_1	I	Eprom Data
28	31	D_0	I	Eprom Data (LSB)
29	32	A_0	O	Eprom Address (MSB)
30	33	A_1	O	Eprom Address
31	35	A_2	O	Eprom Address
32	36	A_3	O	Eprom Address
33	37	A_4	O	Eprom Address
34	38	A_5	O	Eprom Address
35	39	A_6	O	Eprom Address
36	40	A_7	O	Eprom Address
37	41	A_8	O	Eprom Address
38	42	A_9	O	Eprom Address
39	43	A_{10}	O	Eprom Address (LSB)
40	44	V_{DD}	O	Positive power supply

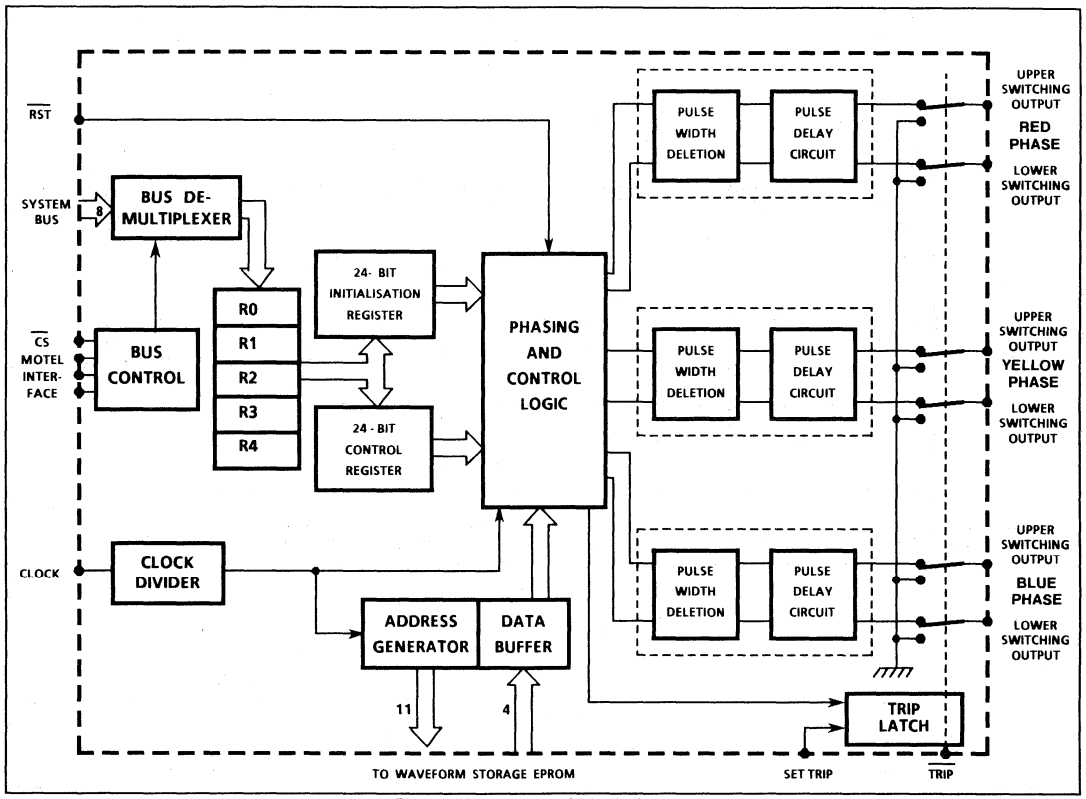


Fig.2: MA818 internal block diagram

FUNCTIONAL DESCRIPTION

An asynchronous method of PWM generation is used with uniform or 'double-edged' regular sampling of the waveform stored in the PROM/EPROM as illustrated in Fig.3. The use of an external PROM/EPROM allows the user to define the optimum power waveform for the particular motor being used.

The triangle carrier wave frequency is selectable up to 24 kHz (assuming the maximum clock frequency of 12.5MHz is used) enabling ultrasonic operation for noise critical applications. Power frequency ranges of up to 4kHz (with 12.5MHz clock) are possible, with the actual output frequency resolved to 12-bit accuracy within the chosen range in order to give precise motor speed control and smooth frequency changing. The output phase sequence of the PWM outputs can also be changed to allow both forward and reverse motor operation.

PWM output pulses can be 'tailored' to the inverter characteristics by defining the minimum allowable pulse width (the MA818 will delete all shorter pulses from the 'pure' PWM pulse train) and the pulse delay (underlap) time without the need for external circuitry. This gives cost advantages on both component savings and in allowing the same PWM circuitry to be used for control of a number of different motor drive circuits simply by changing the microprocessor software.

Power frequency amplitude control is also provided with an overmodulation option to assist in rapid motor braking.

An asynchronous trip input allowes the PWM outputs to be shut down immediately, overriding the microprocessor control in the event of an emergency.

Other possible MA818 applications are as a 3-phase waveform generator as part of a switched-mode power supply (SMPS) or of an uninterruptable power supply (UPS). In such applications the high carrier frequency allows a very small switching transformer to be used.

MICROPROCESSOR INTERFACE

The MA818 interfaces to the controlling microprocessor by means of a multiplexed bus of the MOTEL format. This interface bus has the ability to adapt itself automatically to the format and timing of both MOTorola and IntEL interface buses (hence MOTEL). Internally, the detection circuitry latches the status of the DS/$\overline{RD}$ line when AS/ALE goes high. If the result is high, then the Intel mode is used; if the result is low then the Motorola mode is used. This procedure is carried out each time that AS/ALE goes high. In practice this mode selection is transparent to the user. For bus connection and timing information just read the description relevant to the type of microprocessor/controller that you are using.

Industry standard microprocessors such as the 8085, 8088, etc., and microcontrollers such as the 8051, 8052 and 6805 are all compatible with the interface on the MA818. This interface consists of 8 data lines, AD_0 - AD_7 (write-only in this instance) which are multiplexed to carry both the address and data information, 3 bus control lines, labelled $\overline{WR}$,$\overline{RD}$ and ALE in Intel mode and R/$\overline{W}$,DS and AS in Motorola mode, and a Chip Select input, $\overline{CS}$, which allows the MA818 to share the same bus as other microprocessor peripherals. It should be noted that all bus timings are derived from the microprocessor and are independent of the MA818 clock input.

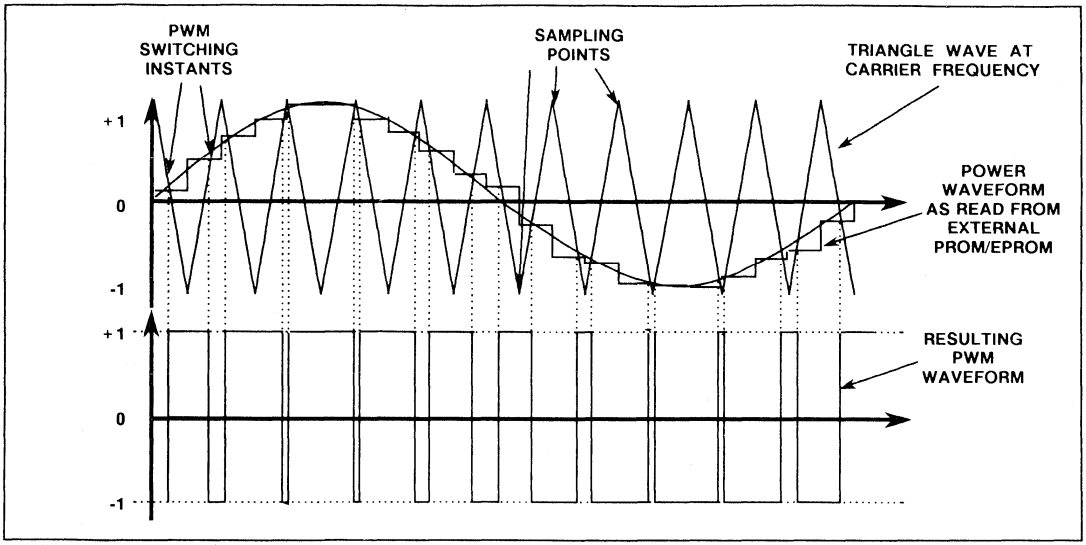


Fig.3 Asynchronous PWM generation with 'double-edged' regular sampling as used on the MA818

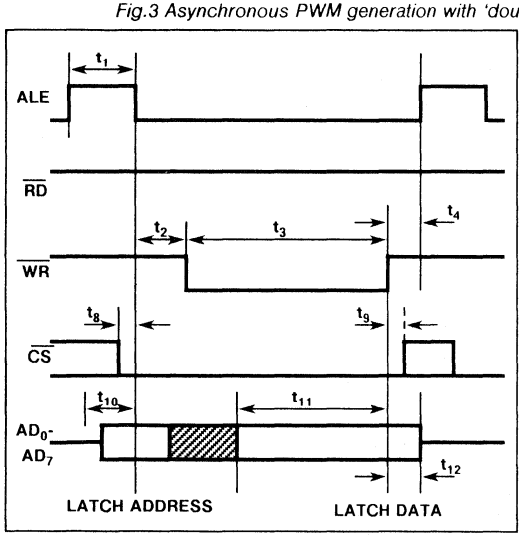


Fig.4 Intel bus timing definitions

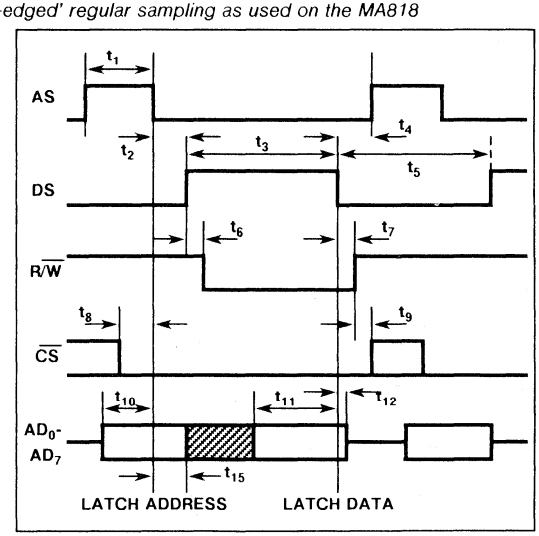


Fig.5 Motorola bus timing definitions

Parameter	Symbol	Min	Units
ALE high period	t_1	70	ns
Delay time , ALE to $\overline{WR}$	t_2	40	ns
$\overline{WR}$ low period	t_3	200	ns
Delay time, $\overline{WR}$ high to ALE high	t_4	40	ns
$\overline{CS}$ setup time	t_8	20	ns
$\overline{CS}$ hold time	t_9	0	ns
Address setup time	t_{10}	30	ns
Address hold time	t_{15}	30	ns
Data setup time	t_{11}	100	ns
Data hold time	t_{12}	25	ns

Table 1 Intel bus timings at V_{DD} = 5V, T_{AMB} = +25°C

Parameter	Symbol	Min	Units
AS high period	t_1	90	ns
Delay time , AS low to DS high	t_2	40	ns
DS high period	t_3	210	ns
Delay time, DS low to AS high	t_4	40	ns
DS low period	t_5	200	ns
DS high to R/$\overline{W}$ low setup time	t_6	10	ns
R/$\overline{W}$ hold time	t_7	10	ns
$\overline{CS}$ setup time	t_8	20	ns
$\overline{CS}$ hold time	t_9	0	ns
Address setup time	t_{10}	30	ns
Address hold time	t_{15}	30	ns
Write data setup time	t_{11}	110	ns
Write data hold time	t_{12}	30	ns

Table 2 Motorola bus timings at V_{DD} = 5V, T_{AMB} = +25°C

MICROPROCESSOR BUS TIMING

Intel Mode (Fig. 4 and Table 1)

The address is latched by the falling edge of ALE. Data is written from the bus into the MA818 on the rising edge of $\overline{WR}$. $\overline{RD}$ is not used in this mode because the registers in the MA818 are write only. However this pin must be connected to $\overline{RD}$ (or tied high) to enable the MA818 to select the correct interface format.

Motorola Mode (Fig. 5 and Table 2)

The address is latched on the falling edge of the AS line. Data is written from the bus into the MA818 (only when R/$\overline{W}$ is low) on the falling edge of DS (providing $\overline{CS}$ is low).

CONTROLLING THE MA818

The MA818 is controlled by loading data into two 24-bit registers via the microprocessor interface. These registers are the initialisation register and the control register.

The initialisation register would normally be loaded before motor operation (i.e. prior to the PWM outputs being activated) and sets up the basic operating parameters associated with the motor and inverter.This data would not normally be updated during motor operation.

The control register is used to control the PWM outputs (and hence the motor) during operation, e.g. stop/start, speed, forward/reverse etc. and would normally be loaded and changed only after the initialisation register has been loaded.

As the MOTEL bus interface is restricted to an 8-bit wide format, data to be loaded into either of the 24-bit register is first written to three 8-bit temporary registers denoted R0, R1, and R2 before being transferred to the desired 24-bit register. The data is accepted (and acted upon) only when transferred to one of the 24-bit registers.

Transfer of data from the temporary registers to either the initialisation register or the control register is achieved by a write instruction to a 'dummy' register. Writing to dummy register R3 results in data transfer from R0, R1 and R2 to the control register while writing to dummy register R4 transfers data from R0, R1 and R2 to the initialisation register. It does not matter what data is 'written' to the dummy registers R3 and R4 as they are not real registers. It is merely the write instruction to either of these registers which is acted apon in order to load the initialisation and control registers.

AD_2	AD_1	AD_0	Register	Comment
0	0	0	R0	Temporary register R0
0	0	1	R1	Temporary register R1
0	1	0	R2	Temporary register R2
0	1	1	R3	Transfers control data
1	0	0	R4	Transfers initialisation data

Table 3 MA818 register addressing

Initialisation Register Function

The 24-bit initialisation register contains parameters which, under normal operation, will be defined during the power up sequence. These parameters are particular to the drive circuitry used, and therefore changing these parameters during a PWM cycle is not recommended. Information in this register should only be modified whilst $\overline{RST}$ is active (i.e. low) so that the PWM outputs are inhibited (low) during the updating process.

The parameters set in the initialisation register are as follows:

Carrier frequency

Low carrier frequencies reduce switching losses whilst high carrier frequencies increase waveform resolution and can allow ultrasonic operation.

Power frequency range

This sets the maximum power frequency that can be carried within the PWM output waveforms. This would normally be set to a value to prevent the motor system being operated outside its design parameters .

Pulse delay time ('underlap')

For each phase of the PWM cycle there are two control signals, one for the top switch connected to the positive inverter DC supply and one for the bottom switch connected to the negative inverter DC supply. In theory the states of these two switches are always complementary. However, due to the finite and non-equal turn-on and turn-off times of power devices, it is desirable when changing the state of the output pair, to provide a short delay time during which both outputs are off in order to avoid a short circuit through the switching elements.

Pulse deletion time

A pure PWM sequence produces pulses which can vary in width between 0% and 100% of the duty cycle. Therefore, in theory, pulse widths can become infinitessimally narrow. In practice this causes problems in the power switches due to storage effects and therefore a minimum pulse width time is required. All pulses shorter than the minimum specified are deleted.

Counter reset

This facility allows the internal power frequency counter of the MA818 to be set to zero, disabling the normal frequency control and giving a 50% output duty cycle.

Initialisation Register Programming

The initialisation register data is loaded in 8-bit segments into the three 8-bit temporary registers R0-R2. When all the initialisation data has been loaded into these registers it is transferred into the 24-bit initialisation register by 'writing' to the dummy register R4.

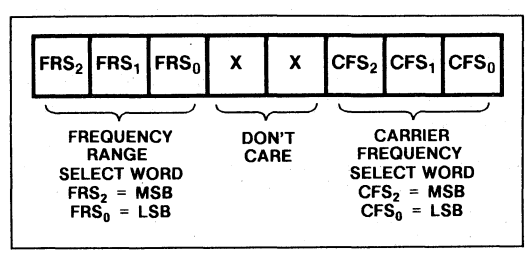


Fig.6 Temporary register R1

Carrier frequency selection

The carrier frequency is a function of the externally applied clock frequency and a division ratio, n, determined by the 3-bit CFS word set during initialisation. The values of n are selected as shown in Table 4.

CFS word	101	100	011	010	001	000
Value of n	32	16	8	4	2	1

Table 4 Values of clock division ratio n

The carrier frequency , f_{CARR}, is then given by:

$$f_{CARR} = \frac{k}{512 \times n}$$

where k = clock frequency and n = 1, 2, 4, 8, 16, or 32 (as set by CFS)

Power frequency range selection

The power frequency range selected here defines the maximum limit of the power frequency. The operating power frequency is controlled by the 12-bit Power Frequency Select (PFS) word in the control register but may not exceed the value set here.

The power frequency range is a function of the carrier waveform frequency (f_{CARR}), and a multiplication factor, m, determined by the 3-bit FRS word. The value of m is determined as shown in Table 5.

FRS word	110	101	100	011	010	001	000
Value of m	64	32	16	8	4	2	1

Table 5 Values of carrier frequency multiplication factor m

The power frequency range , f_{RANGE}, is then given by:

$$f_{RANGE} = \frac{f_{CARR}}{384} \times m$$

where f_{CARR} = carrier frequency and m = 1, 2, 4, 8, 16, 32 or 64 (as set by CFS).

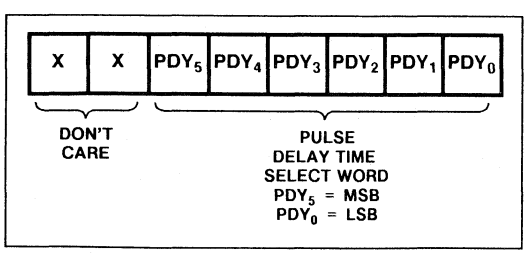


Fig.7 Temporary register R2

Pulse delay time

The pulse delay time affects all six PWM outputs by delaying the rising edges of each of the outputs by an equal amount.

The pulse delay time is a function of the carrier waveform frequency and pdy, defined by the 6-bit pulse delay time select word (PDY). The value of pdy is selected as shown in Table 6.

PDY word	111111	111110	...etc...	000000
Value of pdy	1	2	...etc...	64

Table 6 Values of pdy

The pulse delay time, t_{PDY}, is then given by:

$$t_{pdy} = \frac{pdy}{f_{CARR} \times 512}$$

where pdy = 1-64 (as set by PDY) and f_{CARR} = carrier frequency.

Fig. 8 shows the effect of the pulse delay circuit.

It should be noted that as the pulse delay circuit follows the pulse deletion circuit (see Fig.2); the minimum pulse width seen at the PWM outputs will be shorter than the pulse deletion time set in the initialisation register. The actual shortest pulse generated is given by t_{pd} - t_{pdy}.

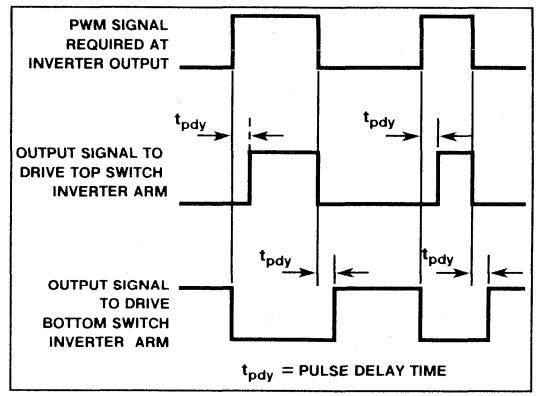


Fig. 8 Effect of pulse delay on PWM pulse train

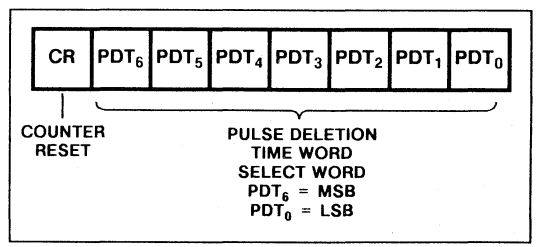


Fig.9 Temporary register R0

Pulse deletion time

To eliminate short pulses the true PWM pulse train is passed through a pulse deletion circuit. The pulse deletion circuit compares pulse widths with the pulse deletion time set in the initialisation register.If a pulse (either +ve or -ve) is greater than or equal to the pulse deletion time, it is passed through unaltered, otherwise the pulse is deleted.

The pulse deletion time, t_{pd} is a function of the carrier wave frequency and pdt, defined by the 7-bit pulse deletion time word (PDT). The value of pdt is selected as shown in Table 7.

PDT word	1111111	1111110	...etc...	0000000
Value of pdt	1	2	...etc...	128

Table 7 Values of pdt

The pulse deletion time, t_{pd}, is then given by:

$$t_{pd} = \frac{pdt}{f_{CARR} \times 512}$$

where pdt = 1-128 (as set by PDT) and f_{CARR} = carrier frequency.

Fig. 10 shows the effect of pulse deletion on a pure PWM waveform.

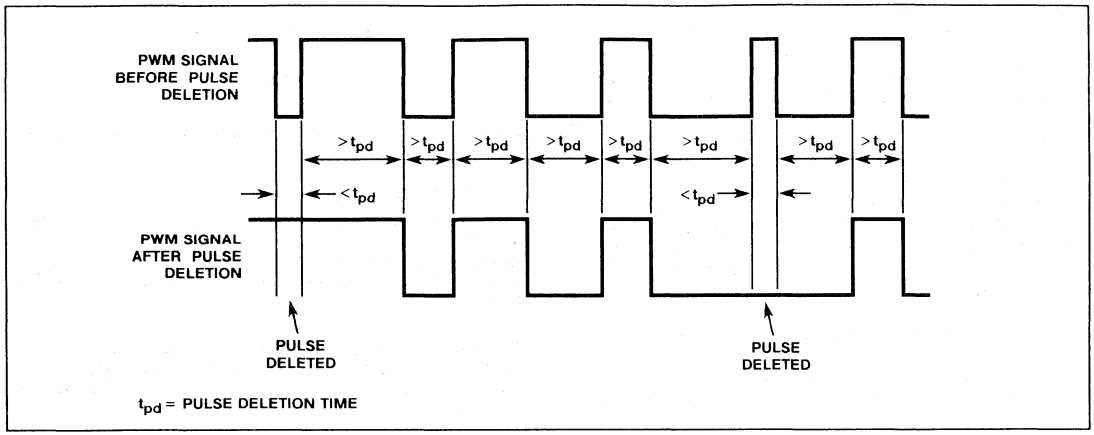


Fig. 10 The effect of the pulse deletion circuit

Counter reset

When the CR bit is active (i.e. low) the internal power frequency phase counter is set to 0 degrees for the red phase. The power frequency is then set to 0 and cannot be changed via the normal frequency control.

Control Register Function

This 24-bit register contains the parameters that would normally be modified during PWM cycles, in order to control the operation of the motor.

The parameters set in the control register are as follows:

Power frequency (speed)

Allows the power frequency of the PWM outputs to be adjusted within the range specified in the initialisation register.

Forward / reverse

Allows the direction of rotation of the AC motor to be changed by changing the phase sequence of the PWM outputs.

Power frequency amplitude

By altering the widths of the PWM output pulses while maintaining their relative widths, the amplitude of the power waveform is effectively altered whilst maintaining the same power frequency.

Overmodulation

Allows the output waveform amplitude to be doubled so that a quasi-square wave is produced. A combination of overmodulation and a lower power frequency can be used to achieve rapid braking in AC motors.

Output inhibit

Allows the outputs to be set to the low state while the PWM generation continues internally. Useful for temporarily inhibiting the outputs without having to to change other register contents.

Control Register Programming

The control register should only be programmed once the initialisation register contains the basic operating parameters of the MA818.

As with the initialisation register, control register data is loaded into the 3, 8-bit temporary registers R0 - R2. When all the data has been loaded into these registers it is transferred into the 24-bit control register by 'writing' to the dummy register R3. It is recommended that all three temporary registers are updated before writing to R3 in order to ensure that a conformal set of data is transferred to the control register for execution.

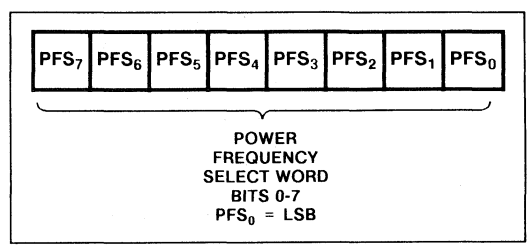


Fig.11 Temporary register R0

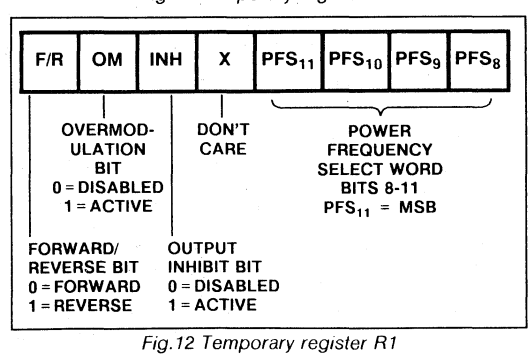


Fig.12 Temporary register R1

Power frequency selection

The power frequency is selected as a proportion of the power frequency range (defined in the initialisation register) by the 12-bit power frequency select word, PFS, allowing the power frequency to be defined in 4096 equal steps. As the PFS word spans the two temporary registers R0 and R1 it is therefore essential, when changing the power frequency, that both these registers are updated before writing to R3 .

The power frequency (f_{POWER}) is given by:

$$f_{POWER} = \frac{f_{RANGE}}{4096} \times pfs$$

where pfs = decimal value of the 12-bit PFS word and f_{RANGE} = power frequency range set in the initialisation register.

Output inhibit selection

When active (i.e., low) the output inhibit bit sets all the PWM outputs to the off (low) state. No other internal operation of the device is affected. When the inhibit is released the PWM outputs continue immediately. Note that as the inhibit is asserted after the pulse deletion and pulse delay circuits, pulses shorter than the normal minimum pulse width may be produced initially.

Overmodulation selection

The overmodulation bit is, in effect, the ninth bit (MSB) of the amplitude word. When active (i.e., high) the output waveform will be controlled in the 100% to 200% range by the amplitude word. The percentage amplitude control is now given by:

$$\text{Overmodulated Amplitude} = A_{POWER} + 100\%$$

where A_{POWER} = the power amplitude.

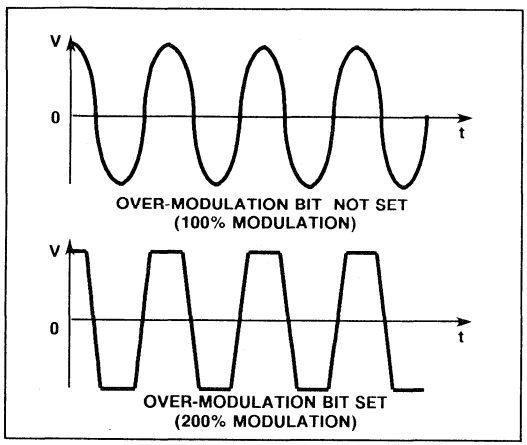


Fig.13 Voltage waveforms as seen at the motor terminals, showing the effect of setting the overmodulation bit.

Forward / reverse selection

The phase sequence of the three-phase PWM output waveforms is controlled by the Forward/Reverse bit.

The actual effect of changing this bit from 0 (forward) to 1 (reverse) is to reverse the power frequency phase counter from incrementing the phase angle to decrementing it. The required output waveforms are all continuous with time during a forward/reverse change.

In the forward mode the output phase sequence is red-yellow-blue and in the reverse mode the sequence is blue-yellow-red.

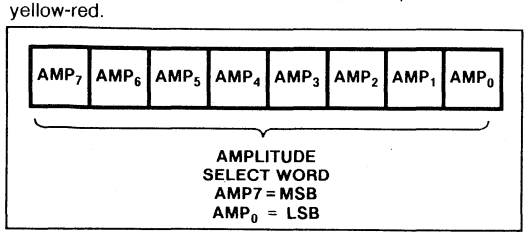


Fig.14 Temporary register R2

Amplitude Selection

The power waveform amplitude is determined by scaling the amplitude of the waveform samples stored in the external PROM/EPROM by the value of the 8-bit amplitude select word (AMP).

The percentage amplitude control is given by:

$$\text{Power Amplitude, } A_{POWER} = \frac{A}{255} \times 100\%$$

where A = decimal value of the 8-bit amplitude select word (AMP).

MA818 PROGRAMMING EXAMPLE

The following example assumes that a master clock of 12.288 MHz is used (12.288 MHz crystals are readily available). This clock frequency will allow a maximum carrier frequency of 24 kHz and a maximum power frequency of 4 kHz.

Initialisation Register Programming Example

A power waveform range of up to 250Hz is required with a carrier frequency of 6kHz, a pulse deletion time of 10μs and an underlap of 5μs.

1. Setting the carrier frequency

The carrier frequency should be set first as the power frequency, pulse deletion time and pulse delay time are all defined relative to the carrier frequency.

We must calculate the value of n which will give the required carrier frequency:

$$f_{CARR} = \frac{k}{512 \times n}$$

$$\Rightarrow \mathbf{n} = \frac{k}{512 \times f_{CARR}} = \frac{12.288 \times 10^6}{512 \times 6 \times 10^3} = \mathbf{4}$$

From Table 4, $n = 4$ corresponds to a 3-bit CFS word of 010 in temporary register R1.

2. Setting the power frequency range

We must calculate the value of m which will give the required power frequency:

$$f_{RANGE} = \frac{f_{CARR}}{512} \times m$$

$$\Rightarrow \mathbf{m} = \frac{f_{RANGE} \times 384}{f_{CARR}} = \frac{250 \times 384}{6 \times 10^3} = \mathbf{16}$$

From Table 5, $m = 16$ corresponds to a 3-bit FRS word of 100 in temporary register R1.

3. Setting the pulse delay time

As the pulse delay time affects the actual minimum pulse width seen at the PWM outputs, it is sensible to set the pulse delay time before the pulse deletion time, so that the effect of the pulse delay time can be allowed for when setting the pulse deletion time.

We must calculate the value of pdy which will give the required pulse delay time:

$$t_{pdy} = \frac{pdy}{f_{CARR} \times 512}$$

$$\Rightarrow \mathbf{pdy} = t_{pdy} \times f_{CARR} \times 512$$

$$= 5 \times 10^{-6} \times 6 \times 10^3 \times 512 = \mathbf{15.4}$$

However, the value of pdy must be an integer. As the purpose of the pulse delay is to prevent 'shoot-through' (where both top and bottom arms of the inverter are on simultaneously), it is sensible to round the pulse delay time up to a higher, rather than a lower figure.

Thus, if we assign the value 16 to pdy this gives a delay time of 5.2μs. From Table 6, pdy = 16 corresponds to a 6-bit PDY word of 110000 in temporary register R2.

4. Setting the pulse deletion time

In setting the pulse deletion time (i.e., the minimum pulse width) account must be taken of the pulse delay time, as the actual minimum pulse width seen at the PWM outputs is equal to $t_{pd} - t_{pdy}$.

Therefore, the value of the pulse deletion time, must, in this instance, be set to 5.2μs longer than the minimum pulse length required.

Minimum pulse length required = 10μs

$\therefore t_{PD}$ to be set = 10μs + 5.2μs = 15.2μs

Now,

$$f_{pd} = \frac{pdt}{f_{CARR} \times 512}$$

$$\Rightarrow \mathbf{pdt} = f_{pd} \times f_{CARR} \times 512$$

$$= 15.2 \times 10^{-6} \times 6 \times 10^{3} \times 512 = \mathbf{46.7}$$

Again, *pdt* must be an integer and so must be either rounded up or down - the choice of which will depend on the application. Assuming we choose in this case the value 46 for pdt, this gives a value of t_{pd} of 15 μs and an actual minimum pulse width of 15 - 5.2 μs = 9.8 μs.

From Table 7, *pdt* = 46 corresponds to a value of PDT, the 7-bit word in temporary register R0 of 1010010.

The data which must be programmed into the three temporary registers R0, R1 and R2 (for transfer into the initialisation register) in order to achieve the parameters in the example given, is shown in Fig. 15.

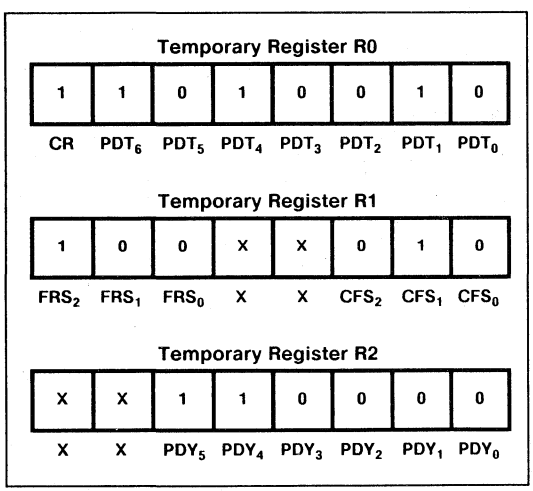


Fig.15

Control Register Programming Example

The control register would normally be updated many times whilst the motor is running, but just one example is given here. It is assumed that the initialisation register has already been programmed with the parameters given in the previous example.

A power waveform of 100 Hz is required with a PWM waveform amplitude of 80% of that stored in the EPROM. The phase sequence should be set to give forward motor rotation. The outputs should be enabled and no overmodulation is required.

1. Setting the power frequency

The power frequency, f_{POWER}, can be selected to 12-bit accuracy (i.e. 4096 equal steps) from 0 Hz to f_{RANGE} as defined in the initialisation register. In this case, with f_{RANGE} = 250Hz the power frequency can be adjusted in increments of 0.06 Hz.

$$f_{POWER} = \frac{f_{RANGE}}{4096} \times pfs$$

$$\Rightarrow \mathbf{pfs} = \frac{f_{POWER} \times 4096}{f_{RANGE}} = \frac{100 \times 4096}{250} = \mathbf{1638.4}$$

We can only have pfs as an integer, so if we assign pfs = 1638 this gives f_{POWER} = 99.97 Hz. The 12-bit binary equivalent of this value gives a PFS word of 011001100110 in temporary registers R0 and R1.

2. Setting overmodulation, forward/reverse, output inhibit

Overmodulation is not required therefore overmodulation bit = 0.

Forward motor control is required, (i.e., the phase sequence of the PWM outputs should be red-yellow-blue) therefore forward/reverse bit = 0.

Output inhibit should be inactive (i.e., the outputs should be active), therefore the output inhibit bit = 1.

These bits are all set in temporary register R1.

3. Setting the power waveform amplitude

$$A_{POWER} = \frac{A}{255} \times 100\%$$

$$\Rightarrow \mathbf{A} = \frac{A_{POWER} \times 255}{100} = \frac{80 \times 255}{100} = \mathbf{204}$$

The 8-bit binary equivalent of this value gives an AMP word of 11001100 in temporary register R2.

The data which must be programmed into the three temporary registers R0, R1 and R2 (for transfer into the control register) in order to achieve the parameters in the example given, is shown in Fig. 16.

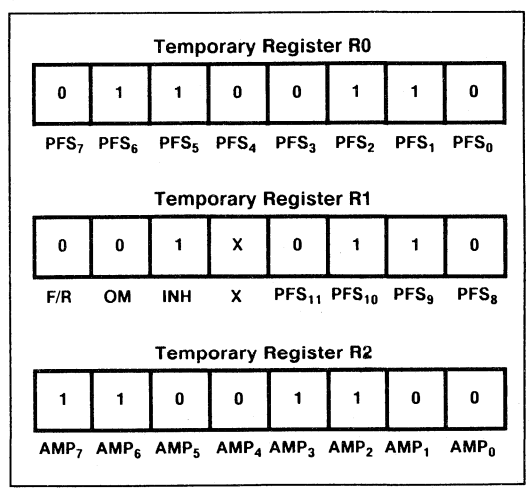


Fig.16

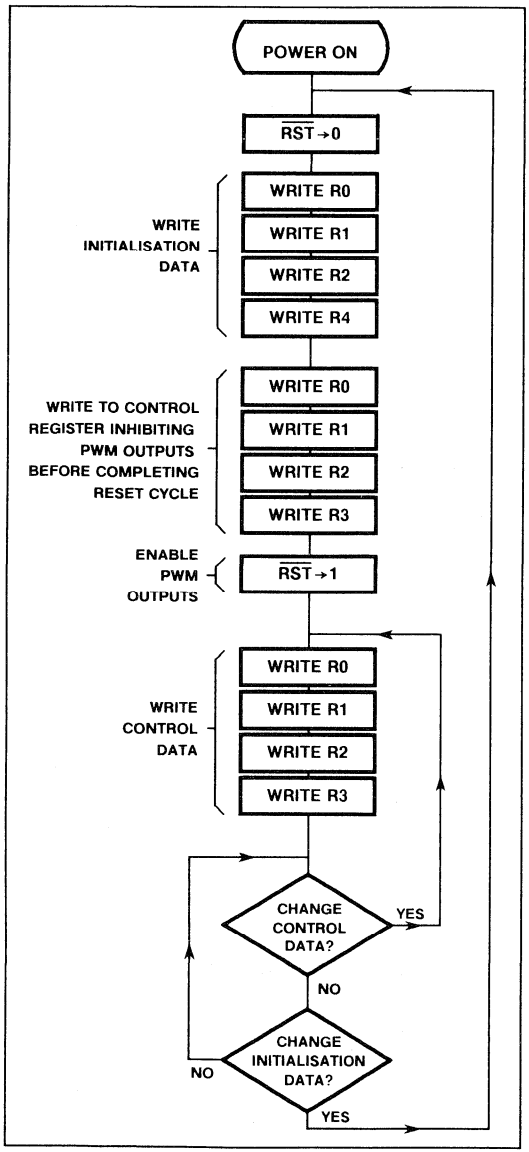


Fig.17 Typical MA818 programming routine

HARDWARE INPUT/OUTPUT FUNCTIONS

Set Output Trip (SET TRIP input)

The SET TRIP input is provided separately from the microprocessor interface in order to allow an external source to override the microprocessor and provide a rapid shutdown facility. For example, logic signals from overcurrent sensing circuitry or the microprocessor 'watchdog' might be used to activate this input.

When the SET TRIP input is taken to a logic high, the output trip latch is activated. This results in the $\overline{\text{TRIP}}$ output and the six PWM outputs being latched low immediately. This condition can only be cleared by applying a reset cycle to the $\overline{\text{RST}}$ input.

Because of the asynchronous nature of this input, it is inportant that when not in use it is tied low and isolated from potential sources of noise. On no account should this input be left floating.

Output Trip Status ($\overline{\text{TRIP}}$ output)

The $\overline{\text{TRIP}}$ output indicates the status of the output trip latch and is active low.

Reset ($\overline{\text{RST}}$ input)

The $\overline{\text{RST}}$ input is active low and performs the following functions:

1. All PWM outputs are forced low (if not already low), thereby turning off the drive switches.
2. All internal counters are reset to zero (this corresponds to 0° for the red phase output).
3. When released, the rising edge reactivates the PWM outputs, resetting the output trip and setting the $\overline{\text{TRIP}}$ output high - assuming that the SET TRIP input is inactive (i.e. low).

Zero Phase Pulse (ZPP output)

The ZPP output provides pulses at the same frequency as the power frequency with a 1:2 mark-space ratio. When in the forward mode of operation the falling edge of ZPP corresponds to 0° for the red phase PWM output. In the reverse mode, the rising edge of ZPP corresponds to 0° for the red phase PWM output.

Clock (CLK input)

The CLK input provides a timing reference used by the MA818 for all timings related to the PWM outputs.

The microprocessor interface, however, derives all its timings from the microprocessor and therefore the microprocessor and the MA818 may be run either from the same or from different clocks.

PWM WAVEFORM ASSIGNMENT

The waveform amplitude data used to construct the PWM output sequences is read by the MA818 from an external 2K×8 PROM/EPROM. The use of an external PROM/EPROM allows the user to define the exact waveform required.

Waveform Definition

Good waveform resolution is achieved by storing 768 8-bit amplitude samples representing the positive 180° span of the waveform. It is assumed that the data is symmetrical around the 90° axis. The MA818 constructs the full 360° waveform by assigning negative values to the same samples for the second half of the cycle.

The MA818 uses these samples to calculate the three instantaneous amplitudes for all three phases. The 768 8-bit samples are linearly spaced over the 0° to 180° span giving an angular resolution of approximately 0.23°.

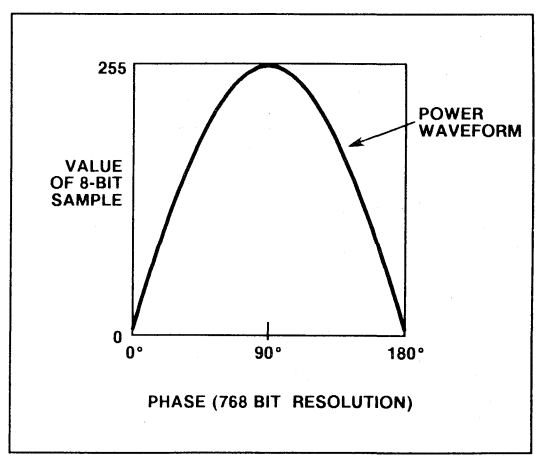


Fig.18 180° sample of typical power waveform

Waveform segment	Sample number
0° - 60°	0 - 256
60.23° - 120°	257 - 512
120.23° - 179.77°	513 - 767

Table 8. 180° of the 360° cycle is divided into 768 8-bit samples

WAVEFORM STORAGE

An industry standard 2K×8 PROM or EPROM (2716 or 27C16) is needed for waveform storage. As less than half the memory capacity of the PROM/EPROM is needed to store the waveform, this is used to advantage in order to minimise the pin count of the MA818. Each 8-bit data word representing a sample of the waveform is stored as 2, 4-bit nibbles in the least significant nibble position of the 8-bit PROM/EPROM locations. Hence the most significant nibble is unused (and may therefore be left unprogrammed) so only 4 data lines (D_0 - D_3) are required.

The 768 waveform samples are therefore stored as 1546 4-bit samples. Fig. 19 illustrates the method in which the data is mapped into the PROM/EPROM. The least significant nibbles are stored sequentially from location 0_H to 300_H , whilst the most significant nibbles are stored from 400_H to 700_H.

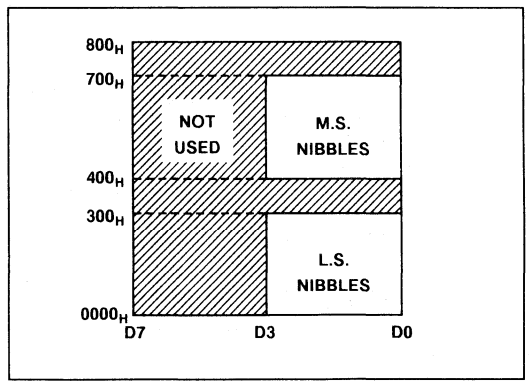


Fig.19 Waveform PROM/EPROM memory map

The MA818 reads the data by accessing the two 4-bit nibbles (using A10 to select the high and low nibble memory areas) and then concatenates them internally to form the 8-bit waveform sample byte.

The reading of data from the the PROM/EPROM is performed automatically by the MA818 without microprocessor intervention whenever the PWM generation is active.

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{DD} = 5V ± 5%, T_{amb} = 25°C

Characteristic	Symbol	Min.	Typ.	Max.	Units	Conditions
Input high voltage	V_{IH}	2		-	V	
Input low voltage	V_{IL}	-		0.8	V	
Input leakage Current	I_{in}	-		10	µA	V_{IN} = V_{SS} or V_{DD}
Output high voltage	V_{OH}	4.0	>4.5	-	V	I_{OH} = -4mA
Output low voltage	V_{OL}	-	<0.2	0.4	V	I_{OL} = 4mA
Supply current (static) (dynamic)	$I_{DD\ (static)}$ $I_{DD\ (dynamic)}$		<10	100 20	µA mA	All outputs open cct. CLK = 10MHz.
Supply Voltage	V_{DD}	4.75	5.0	7.5	V	

NOTE 1. The SET TRIP input has an internal pull-up resistor with an approximate value of 90kΩ

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{DD} = 5V ± 5%, T_{amb} = 25°C

Characteristic	Symbol	Min.	Typ.	Max.	Units	Conditions
Clock frequency	f_{CLK}			12.5	MHz	M:S ratio 1:1 ± 20%
SET TRIP = 0 →Outputs tripped →$\overline{TRIP}$ = 0	t_{TRIP}		<1 <1	3 3	µs µs	
EPROM Address to output delay	t_{ACC}			450	ns	

NOTE 2. For microprocessor interface timings see Intel and Motorola bus timings (Tables 1 and 2).

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	10V
Voltage on any pin	V_{SS}-0.3V to V_{DD}+0.3V
Current through any I/O pin	±10mA
Storage temperature	-65°C to +125°C
Operating temperature range	0°C to +70°C

Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

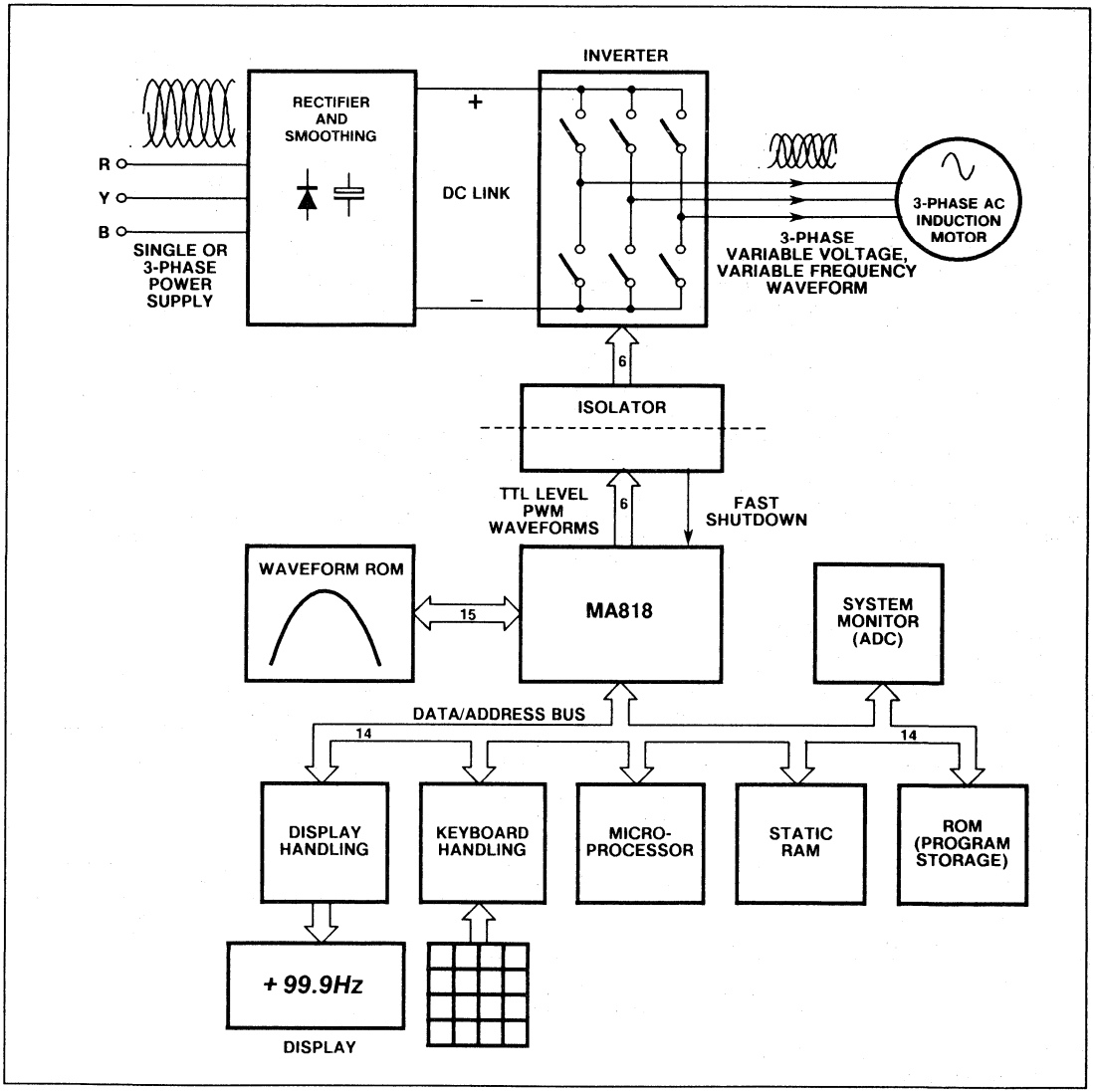


Fig.20 Typical MA818 application

MA828 FAMILY

THREE-PHASE PULSE WIDTH MODULATION WAVEFORM GENERATOR

The MA828 PWM generator has been designed to provide waveforms for the control of variable speed AC machines, uninterruptible power supplies and other forms of power electronic devices which require pulse width modulation as a means of efficient power control.

The six TTL level PWM outputs (Fig.2) control the six switches in a three-phase inverter bridge. This is usually via an external isolation and amplification stage.

Information contained within the pulse width modulated sequences controls the shape, power frequency, amplitude, and rotational direction (as defined by the red-yellow-blue phase sequence) of the output waveform. Parameters such as the carrier frequency, minimum pulse width, and pulse delay time may be defined during the initialisation of the device. The pulse delay time (underlap) controls the delay between turning on and off the two power switches in each output phase of the inverter bridge, in order to accomodate variations in the turn-on and turn-off times of families of power devices.

The MA828 is easily controlled by a microprocessor and its fully-digital generation of PWM waveforms gives unprecedented accuracy and temperature stability. Precision pulse shaping capability allows optimum efficiency with any power circuitry. The device operates as a stand-alone microprocessor peripheral, reading the power waveform directly from an internal ROM and requiring microprocessor intervention only when operating parameters need to be changed.

An 8-bit multiplexed data bus is used to receive addresses and data from the microprocessor/controller. This is a standard MOTEL™ bus, compatible with most microprocessors/controllers.

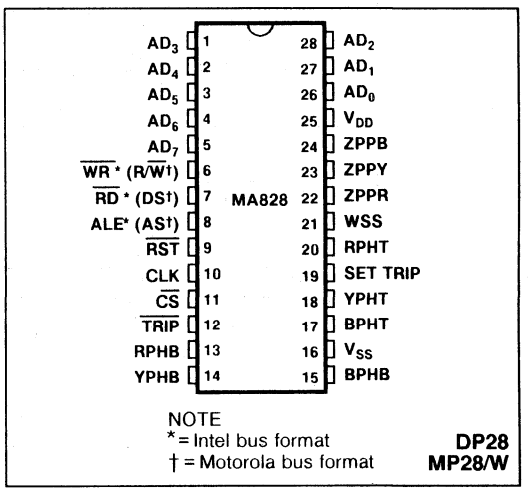


Fig.1 Pin connections - top view

Rotational frequency is defined to 12 bits for high accuracy and a zero setting is included in order to implement DC-injection braking with no software overhead.

This family is functionally identical to the proven MA818 PWM generator IC except that the waveform ROM is integrated on-chip. Two standard waveshapes are available to cover most applications. In addition, any symmetrical waveshape may be integrated on-chip to order.

The MA828 is fabricated in CMOS for low power consumption.

FEATURES

- Fully Digital Operation
- Interfaces with most Microprocessors
- Wide Power-Frequency Range
- 12-Bit Speed Control Accuracy
- Carrier Frequency Selectable up to 24kHz
- Waveform Stored in Internal ROM
- Double Edged Regular Sampling
- Selectable Minimum Pulse Width and Underlap Time
- DC Injection Braking

MOTEL is a registered trademark of Intel corp. and Motorola corp.

PIN DESCRIPTIONS

Pin no.	Name	Type	Function
26	AD_0	I	Multiplexed Address/Data (LSB)
27	AD_1	I	Multiplexed Address/Data
28	AD_2	I	Multiplexed Address/Data
1	AD_3	I	Multiplexed Address/Data
2	AD_4	I	Multiplexed Address/Data
3	AD_5	I	Multiplexed Address/Data
4	AD_6	I	Multiplexed Address/Data
5	AD_7	I	Multiplexed Address/Data (MSB)
6	Intel $\overline{WR}$ Motorola R/$\overline{W}$	I	Intel Write Strobe Motorola Read/Write Select
7	Intel $\overline{RD}$ Motorola DS	I	Intel Read Strobe Motorola Data Strobe
8	Intel ALE Motorola AS	I	Intel Address Latch Enable Motorola Address Strobe
9	$\overline{RST}$	I	Resets Internal Counters
10	CLK	I	Clock Input
11	$\overline{CS}$	I	Chip Select Input
12	$\overline{TRIP}$	O	Output Trip Status
22	ZPPR	O	Zero Phase Pulse-Red Phase
23	ZPPY	O	Zero Phase Pulse-Yellow Phase
24	ZPPB	O	Zero Phase Pulse-Blue Phase
13	RPHB	O	Red Phase (Bottom power switch)
14	YPHB	O	Yellow Phase (Bottom power switch)
15	BPHB	O	Blue Phase (Bottom power switch)
17	BPHT	O	Blue Phase (Top power switch)
18	YPHT	O	Yellow Phase (Top power switch)
20	RPHT	O	Red Phase (Top power switch)
19	SET TRIP	I	Set Output Trip.
21	WSS	O	Waveform Sampling Synchronisation.
25	V_{DD}	S	Positive power supply
16	V_{SS}	S	Negative power supply (0V)

FUNCTIONAL DESCRIPTION

An asynchronous method of PWM generation is used with uniform or 'double-edged' regular sampling of the waveform stored in the internal ROM as illustrated in Fig.3. Two standard waveshape options exist so that the device can be adapted to particular applications (see page 6-25 for product designation). In addition, any symmetrical waveshape may be integrated on-chip, to order.

The triangle carrier wave frequency is selectable up to 24 kHz (assuming the maximum clock frequency of 12.5MHz is used) enabling ultrasonic operation for noise critical applications. Power frequency ranges of up to 4kHz (with 12.5MHz clock) are possible, with the actual output frequency resolved to 12-bit accuracy within the chosen range in order to give precise motor speed control and smooth frequency changing. The output phase sequence of the PWM outputs can also be changed to allow both forward and reverse motor operation.

PWM output pulses can be 'tailored' to the inverter characteristics by defining the minimum allowable pulse width (the MA828 will delete all shorter pulses from the 'pure' PWM pulse train) and the pulse delay (underlap) time without the need for external circuitry.

This gives cost advantages on both component savings and in allowing the same PWM circuitry to be used for control of a number of different motor drive circuits simply by changing the microprocessor software.

Power frequency amplitude control is also provided with an overmodulation option to assist in rapid motor braking. Alternatively, braking may be implemented by setting the rotational speed to 0Hz. This is termed DC injection braking which opposes the rotation of the machine by allowing a DC current flow in the windings.

A trip input allows the PWM outputs to be shut down immediately, overriding the microprocessor control in the event of an emergency.

The Waveform Sampling Synchronisation (WSS) output may be used in conjunction with the ZPP signals to provide feedback of the actual rotational speed from the rotor. This is of particular use in slip compensated systems.

Other possible MA828 Family applications include a 3-phase waveform generator as part of a switched-mode power supply (SMPS) or as part of an uninterruptible power supply (UPS). In such applications the high carrier frequency allows a very small switching transformer to be used.

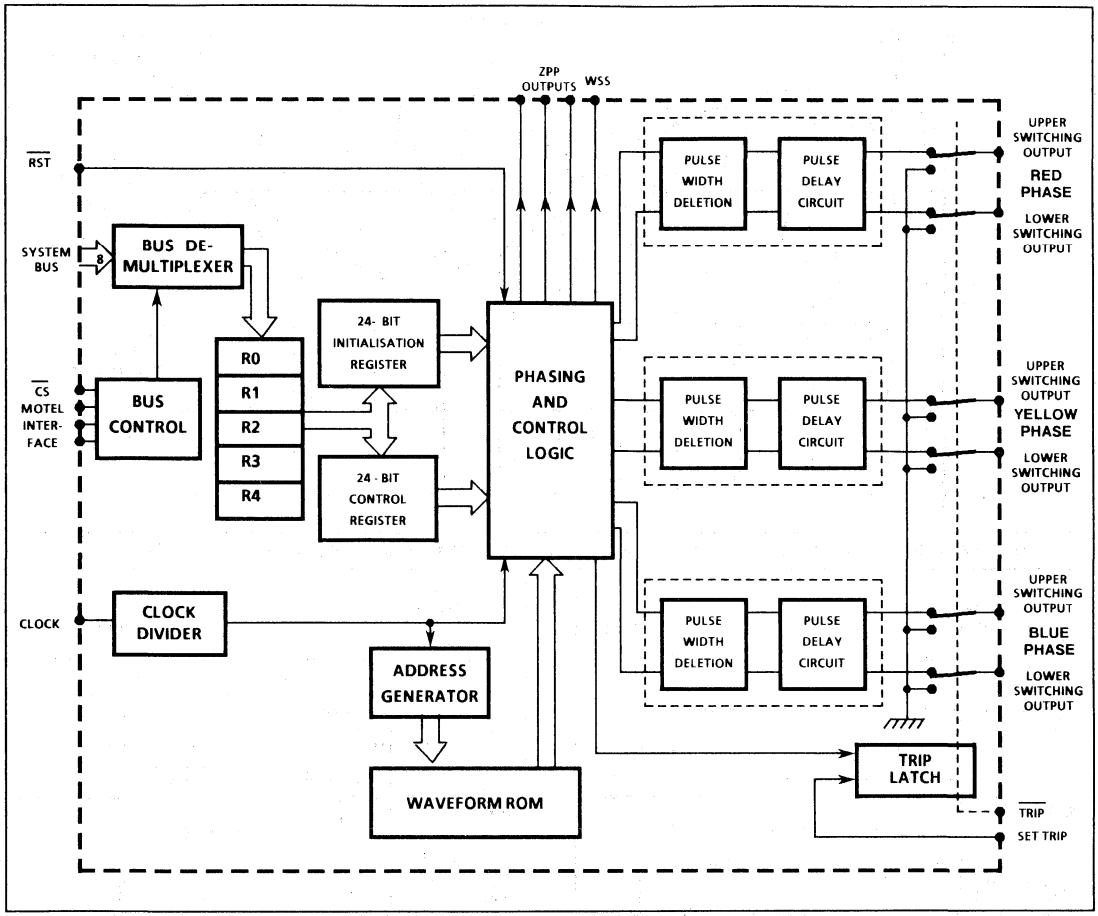


Fig.2: MA828 internal block diagram

MICROPROCESSOR INTERFACE

The MA828 interfaces to the controlling microprocessor by means of a multiplexed bus of the MOTEL format. This interface bus has the ability to adapt itself automatically to the format and timing of both MOTorola and IntEL interface buses (hence MOTEL). Internally, the detection circuitry latches the status of the DS/$\overline{RD}$ line when AS/ALE goes high. If the result is high, then the Intel mode is used; if the result is low then the Motorola mode is used. This procedure is carried out each time that AS/ALE goes high. In practice this mode selection is transparent to the user. For bus connection and timing information just read the description relevant to the type of microprocessor/controller that you are using.

Industry standard microprocessors such as the 8085, 8088, etc., and microcontrollers such as the 8051, 8052 and 6805 are all compatible with the interface on the MA828. This interface consists of 8 data lines, AD_0 - AD_7 (write-only in this instance) which are multiplexed to carry both the address and data information, 3 bus control lines, labelled $\overline{WR}$,$\overline{RD}$ and ALE in Intel mode and R/$\overline{W}$,DS and AS in Motorola mode, and a Chip Select input, $\overline{CS}$, which allows the MA828 to share the same bus as other microprocessor peripherals. It should be noted that all bus timings are derived from the microprocessor and are independent of the MA828 clock input.

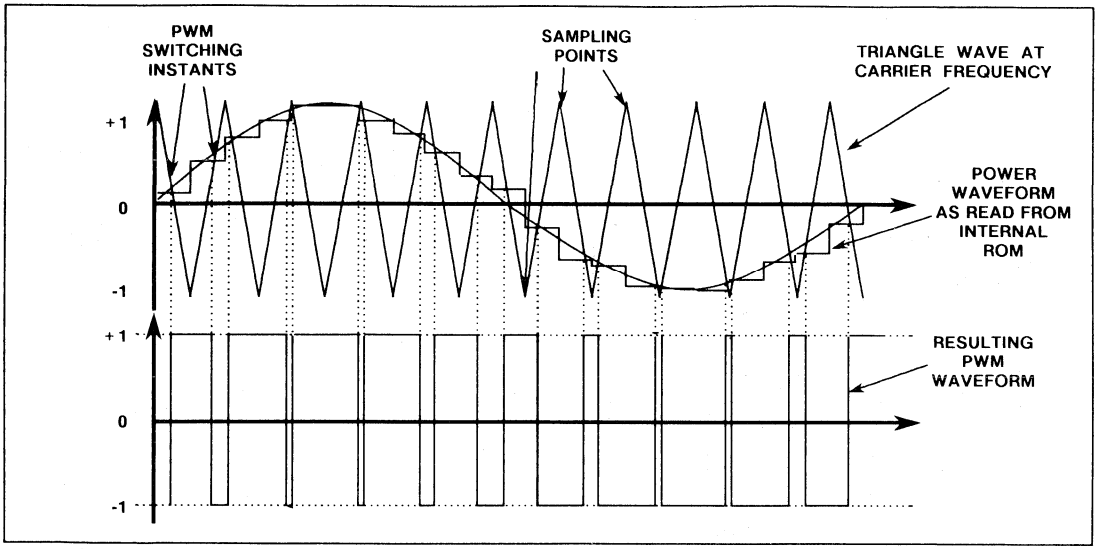


Fig.3 Asynchronous PWM generation with uniform or 'double-edged' regular sampling as used on the MA828

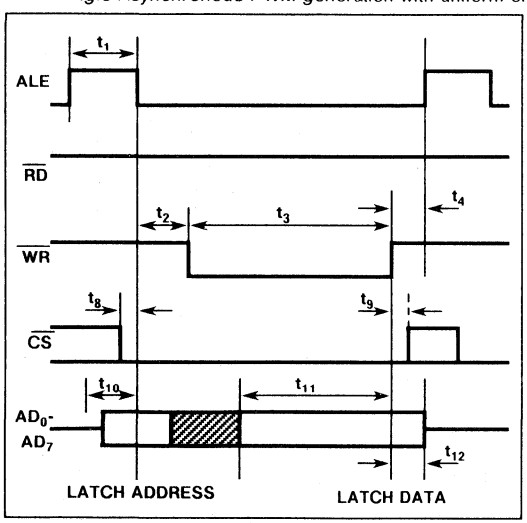


Fig.4 Intel bus timing definitions

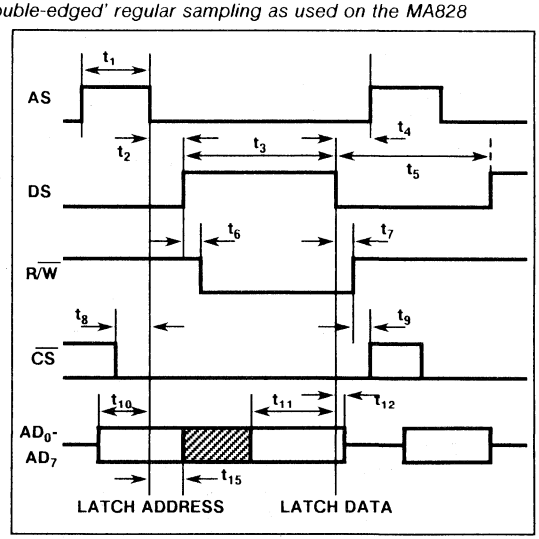


Fig.5 Motorola bus timing definitions

Parameter	Symbol	Min	Units
ALE high period	t_1	70	ns
Delay time , ALE to $\overline{WR}$	t_2	40	ns
$\overline{WR}$ low period	t_3	200	ns
Delay time, $\overline{WR}$ high to ALE high	t_4	40	ns
$\overline{CS}$ setup time	t_8	20	ns
$\overline{CS}$ hold time	t_9	0	ns
Address setup time	t_{10}	30	ns
Address hold time	t_{15}	30	ns
Data setup time	t_{11}	100	ns
Data hold time	t_{12}	25	ns

Table 1 Intel bus timings at V_{DD} = 5V, T_{AMB} = +25°C

Parameter	Symbol	Min	Units
AS high period	t_1	90	ns
Delay time , AS low to DS high	t_2	40	ns
DS high period	t_3	210	ns
Delay time, DS low to AS high	t_4	40	ns
DS low period	t_5	200	ns
DS high to R/$\overline{W}$ low setup time	t_6	10	ns
R/$\overline{W}$ hold time	t_7	10	ns
$\overline{CS}$ setup time	t_8	20	ns
$\overline{CS}$ hold time	t_9	0	ns
Address setup time	t_{10}	30	ns
Address hold time	t_{15}	30	ns
Write data setup time	t_{11}	110	ns
Write data hold time	t_{12}	30	ns

Table 2 Motorola bus timings at V_{DD} = 5V, T_{AMB} = +25°C

MICROPROCESSOR BUS TIMING

Intel Mode (Fig. 4 and Table 1)

The address is latched by the falling edge of ALE. Data is written from the bus into the MA818 on the rising edge of $\overline{WR}$. $\overline{RD}$ is not used in this mode because the registers in the MA818 are write only. However this pin must be connected to $\overline{RD}$ (or tied high) to enable the MA818 to select the correct interface format.

Motorola Mode (Fig. 5 and Table 2)

The address is latched on the falling edge of the AS line. Data is written from the bus into the MA818 (only when R/$\overline{W}$ is low) on the falling edge of DS (providing $\overline{CS}$ is low).

CONTROLLING THE MA828

The MA828 is controlled by loading data into two 24-bit registers via the microprocessor interface. These registers are the initialisation register and the control register.

The initialisation register would normally be loaded before motor operation (i.e. prior to the PWM outputs being activated) and sets up the basic operating parameters associated with the motor and inverter.This data would not normally be updated during motor operation.

The control register is used to control the PWM outputs (and hence the motor) during operation, e.g. stop/start, speed, forward/reverse etc. and would normally be loaded and changed only after the initialisation register has been loaded.

As the MOTEL bus interface is restricted to an 8-bit wide format, data to be loaded into either of the 24-bit register is first written to three 8-bit temporary registers denoted R0, R1, and R2 before being transferred to the desired 24-bit register. The data is accepted (and acted upon) only when transferred to one of the 24-bit registers.

Transfer of data from the temporary registers to either the initialisation register or the control register is achieved by a write instruction to a 'dummy' register. Writing to dummy register R3 results in data transfer from R0, R1 and R2 to the control register while writing to dummy register R4 transfers data from R0, R1 and R2 to the initialisation register. It does not matter what data is 'written' to the dummy registers R3 and R4 as they are not real registers. It is merely the write instruction to either of these registers which is acted apon in order to load the initialisation and control registers.

AD_2	AD_1	AD_0	Register	Comment
0	0	0	R0	Temporary register R0
0	0	1	R1	Temporary register R1
0	1	0	R2	Temporary register R2
0	1	1	R3	Transfers control data
1	0	0	R4	Transfers initialisation data

Table 3 MA828 register addressing

Initialisation Register Function

The 24-bit initialisation register contains parameters which, under normal operation, will be defined during the power up sequence. These parameters are particular to the drive circuitry used, and therefore changing these parameters during a PWM cycle is not recommended. Information in this register should only be modified whilst $\overline{RST}$ is active (i.e. low) so that the PWM outputs are inhibited (low) during the updating process.

The parameters set in the initialisation register are as follows:

Carrier frequency

Low carrier frequencies reduce switching losses whilst high carrier frequencies increase waveform resolution and can allow ultrasonic operation.

Power frequency range

This sets the maximum power frequency that can be carried within the PWM output waveforms. This would normally be set to a value to prevent the motor system being operated outside its design parameters .

Pulse delay time ('underlap')

For each phase of the PWM cycle there are two control signals, one for the top switch connected to the positive inverter DC supply and one for the bottom switch connected to the negative inverter DC supply. In theory the states of these two switches are always complementary. However, due to the finite and non-equal turn-on and turn-off times of power devices, it is desirable when changing the state of the output pair, to provide a short delay time during which both outputs are off in order to avoid a short circuit through the switching elements.

Pulse deletion time

A pure PWM sequence produces pulses which can vary in width between 0% and 100% of the duty cycle. Therefore, in theory, pulse widths can become infinitessimally narrow. In practice this causes problems in the power switches due to storage effects and therefore a minimum pulse width time is required. All pulses shorter than the minimum specified are deleted.

Counter reset

This facility allows the internal power frequency counter of the MA828 to be set to zero, disabling the normal frequency control and giving a 50% output duty cycle.

Initialisation Register Programming

The initialisation register data is loaded in 8-bit segments into the three 8-bit temporary registers R0-R2. When all the initialisation data has been loaded into these registers it is transferred into the 24-bit initialisation register by 'writing' to the dummy register R4.

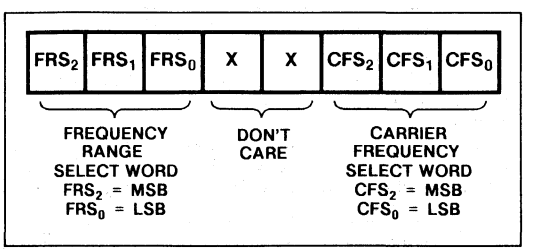


Fig.6 Temporary register R1

Carrier frequency selection

The carrier frequency is a function of the externally applied clock frequency and a division ratio, *n*, determined by the 3-bit CFS word set during initialisation. The values of *n* are selected as shown in Table 4.

CFS word	101	100	011	010	001	000
Value of n	32	16	8	4	2	1

Table 4 Values of clock division ratio n

The carrier frequency , f_{CARR}, is then given by:

$$f_{CARR} = \frac{k}{512 \times n}$$

where k = clock frequency and n = 1, 2, 4, 8, 16, or 32 (as set by CFS)

Power frequency range selection

The power frequency range selected here defines the maximum limit of the power frequency. The operating power frequency is controlled by the 12-bit Power Frequency Select (PFS) word in the control register but may not exceed the value set here.

The power frequency range is a function of the carrier waveform frequency (f_{CARR}), and a multiplication factor, *m*, determined by the 3-bit FRS word. The value of *m* is determined as shown in Table 5.

FRS word	110	101	100	011	010	001	000
Value of m	64	32	16	8	4	2	1

Table 5 Values of carrier frequency multiplication factor m

The power frequency range , f_{RANGE}, is then given by:

$$f_{RANGE} = \frac{f_{CARR}}{384} \times m$$

where f_{CARR} = carrier frequency and m = 1, 2, 4, 8, 16, 32 or 64 (as set by CFS).

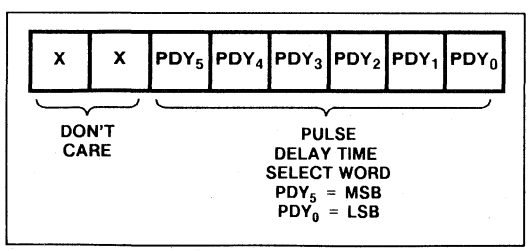


Fig.7 Temporary register R2

Pulse delay time

The pulse delay time affects all six PWM outputs by delaying the rising edges of each of the outputs by an equal amount.

The pulse delay time is a function of the carrier waveform frequency and pdy, defined by the 6-bit pulse delay time select word (PDY). The value of pdy is selected as shown in Table 6.

PDY word	111111	111110	...etc...	000000
Value of pdy	1	2	...etc...	64

Table 6 Values of pdy

The pulse delay time, t_{PDY}, is then given by:

$$t_{pdy} = \frac{pdy}{f_{CARR} \times 512}$$

where pdy = 1-64 (as set by PDY) and f_{CARR} = carrier frequency.

Fig. 8 shows the effect of the pulse delay circuit.

It should be noted that as the pulse delay circuit follows the pulse deletion circuit (see Fig.2); the minimum pulse width seen at the PWM outputs will be shorter than the pulse deletion time set in the initialisation register. The actual shortest pulse generated is given by $t_{pd} - t_{pdy}$.

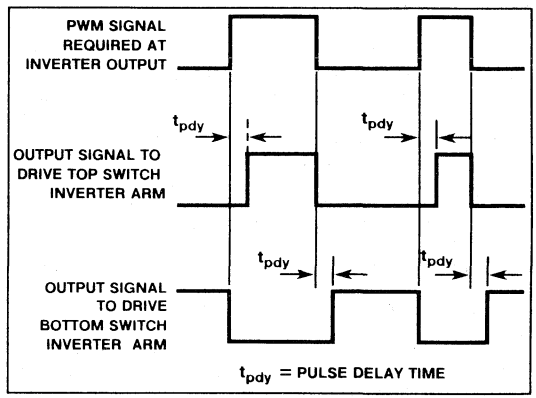


Fig. 8 Effect of pulse delay on PWM pulse train

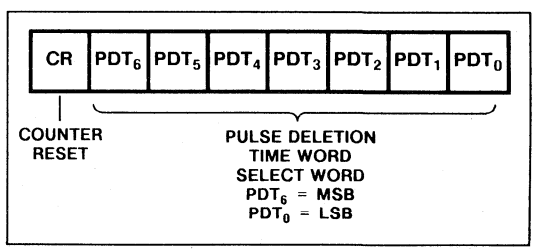


Fig.9 Temporary register R0

Pulse deletion time

To eliminate short pulses the true PWM pulse train is passed through a pulse deletion circuit. The pulse deletion circuit compares pulse widths with the pulse deletion time set in the initialisation register.If a pulse (either +ve or -ve) is greater than or equal to the pulse deletion time, it is passed through unaltered, otherwise the pulse is deleted.

The pulse deletion time, t_{pd} is a function of the carrier wave frequency and *pdt*, defined by the 7-bit pulse deletion time word (PDT). The value of *pdt* is selected as shown in Table 7.

PDT word	1111111	1111110	...etc...	0000000
Value of pdt	1	2	...etc...	128

Table 7 Values of pdt

The pulse deletion time, t_{pd}, is then given by:

$$t_{pd} = \frac{pdt}{f_{CARR} \times 512}$$

where pdt = 1-128 (as set by PDT) and f_{CARR} = carrier frequency.

Fig. 10 shows the effect of pulse deletion on a pure PWM waveform.

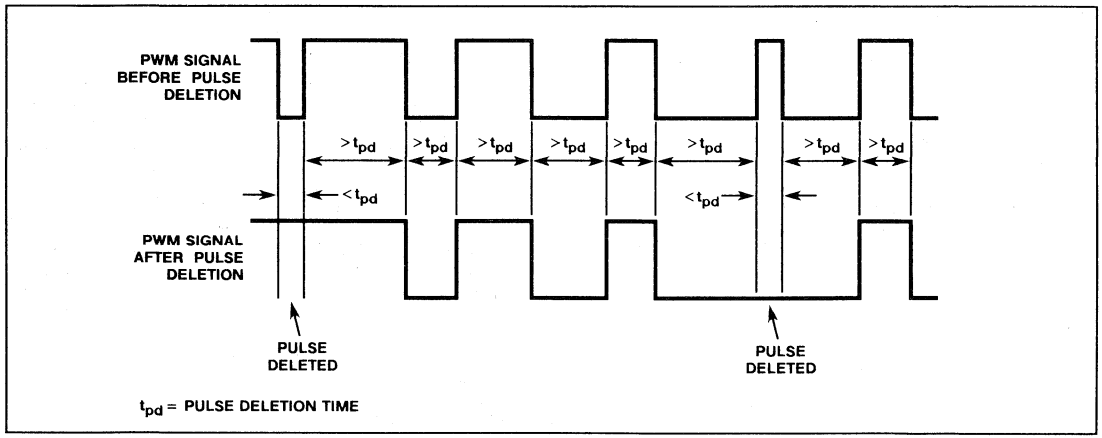


Fig. 10 The effect of the pulse deletion circuit

Counter reset

When the CR bit is active (i.e. low) the internal power frequency phase counter is set to 0 degrees for the red phase. The power frequency is then set to 0 and cannot be changed via the normal frequency control.

Control Register Function

This 24-bit register contains the parameters that would normally be modified during PWM cycles, in order to control the operation of the motor.

The parameters set in the control register are as follows:

Power frequency (speed)

Allows the power frequency of the PWM outputs to be adjusted within the range specified in the initialisation register.

Forward / reverse

Allows the direction of rotation of the AC motor to be changed by changing the phase sequence of the PWM outputs.

Power frequency amplitude

By altering the widths of the PWM output pulses while maintaining their relative widths, the amplitude of the power waveform is effectively altered whilst maintaining the same power frequency.

Overmodulation

Allows the output waveform amplitude to be doubled so that a quasi-square wave is produced. A combination of overmodulation and a lower power frequency can be used to achieve rapid braking in AC motors.

Output inhibit

Allows the outputs to be set to the low state while the PWM generation continues internally. Useful for temporarily inhibiting the outputs without having to to change other register contents.

Control Register Programming

The control register should only be programmed once the initialisation register contains the basic operating parameters of the MA828.

As with the initialisation register, control register data is loaded into the 3, 8-bit temporary registers R0 - R2. When all the data has been loaded into these registers it is transferred into the 24-bit control register by 'writing' to the dummy register R3. It is recommended that all three temporary registers are updated before writing to R3 in order to ensure that a conformal set of data is transferred to the control register for execution.

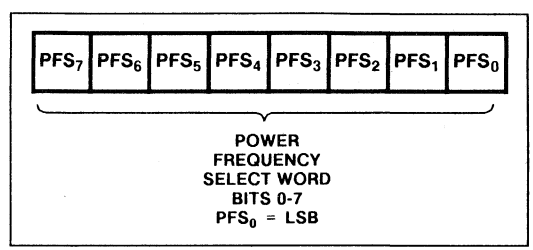


Fig.11 Temporary register R0

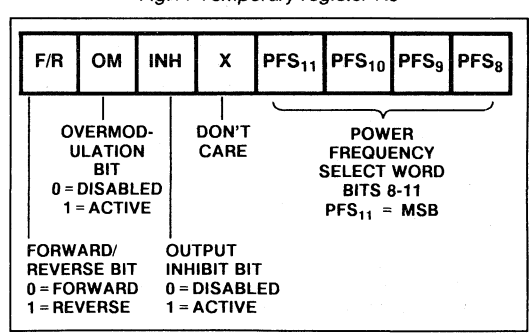


Fig.12 Temporary register R1

Power frequency selection

The power frequency is selected as a proportion of the power frequency range (defined in the initialisation register) by the 12-bit power frequency select word, PFS, allowing the power frequency to be defined in 4096 equal steps. As the PFS word spans the two temporary registers R0 and R1 it is therefore essential, when changing the power frequency, that both these registers are updated before writing to R3 .

The power frequency (f_{POWER}) is given by:

$$f_{POWER} = \frac{f_{RANGE}}{4096} \times pfs$$

where pfs = decimal value of the 12-bit PFS word and f_{RANGE} = power frequency range set in the initialisation register.

Output inhibit selection

When active (i.e., low) the output inhibit bit sets all the PWM outputs to the off (low) state. No other internal operation of the device is affected. When the inhibit is released the PWM outputs continue immediately. Note that as the inhibit is asserted after the pulse deletion and pulse delay circuits, pulses shorter than the normal minimum pulse width may be produced initially.

Overmodulation selection

The overmodulation bit is, in effect, the ninth bit (MSB) of the amplitude word. When active (i.e., high) the output waveform will be controlled in the 100% to 200% range by the amplitude word. The percentage amplitude control is now given by:

$$\text{Overmodulated Amplitude} = A_{POWER} + 100\%$$

where A_{POWER} = the power amplitude.

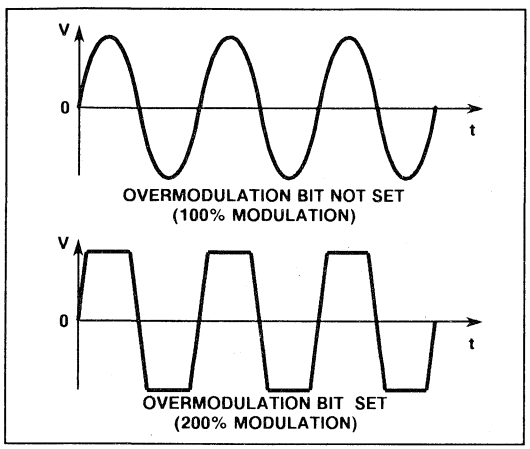


Fig.13 Voltage waveforms as seen at the motor terminals, showing the effect of setting the overmodulation bit.

Forward / reverse selection

The phase sequence of the three-phase PWM output waveforms is controlled by the Forward/Reverse bit.

The actual effect of changing this bit from 0 (forward) to 1 (reverse) is to reverse the power frequency phase counter from incrementing the phase angle to decrementing it. The required output waveforms are all continuous with time during a forward/reverse change.

In the forward mode the output phase sequence is red-yellow-blue and in the reverse mode the sequence is blue-yellow-red.

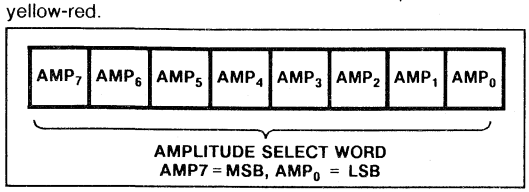


Fig.14 Temporary register R2

Amplitude Selection

The power waveform amplitude is determined by scaling the amplitude of the waveform samples stored in the external PROM/EPROM by the value of the 8-bit amplitude select word (AMP).

The percentage amplitude control is given by:

$$\text{Power Amplitude, } A_{POWER} = \frac{A}{255} \times 100\%$$

where A = integer value of 8-bit amplitude select word, AMP.

POWER-UP CONDITIONS

All bits in both the Initialisation and Control Registers power up in the low state. This means that Counter Reset ($\overline{CR}$) is active and a 50% duty cycle will be output from all PWM outputs until further initialising action is taken. Holding $\overline{RST}$ low or using the SET TRIP input will ensure that the PWM outputs remain inactive (i.e. low) during this period.

MA828 PROGRAMMING EXAMPLE

The following example assumes that a master clock of 12.288 MHz is used (12.288 MHz crystals are readily available).This clock frequency will allow a maximum carrier frequency of 24 kHz and a maximum power frequency of 4 kHz.

Initialisation Register Programming Example

A power waveform range of up to 250Hz is required with a carrier frequency of 6kHz, a pulse deletion time of 10μs and an underlap of 5μs.

1. Setting the carrier frequency

The carrier frequency should be set first as the power frequency, pulse deletion time and pulse delay time are all defined relative to the carrier frequency.

We must calculate the value of n which will give the required carrier frequency:

$$f_{CARR} = \frac{k}{512 \times n}$$

$$\Rightarrow \mathbf{n} = \frac{k}{512 \times f_{CARR}} = \frac{12.288 \times 10^6}{512 \times 6 \times 10^3} = \mathbf{4}$$

From Table 4, $n = 4$ corresponds to a 3-bit CFS word of 010 in temporary register R1.

2. Setting the power frequency range

We must calculate the value of m which will give the required power frequency:

$$f_{RANGE} = \frac{f_{CARR}}{512} \times m$$

$$\Rightarrow \mathbf{m} = \frac{f_{RANGE} \times 384}{f_{CARR}} = \frac{250 \times 384}{6 \times 10^3} = \mathbf{16}$$

From Table 5, $m = 16$ corresponds to a 3-bit FRS word of 100 in temporary register R1.

3. Setting the pulse delay time

As the pulse delay time affects the actual minimum pulse width seen at the PWM outputs, it is sensible to set the pulse delay time before the pulse deletion time, so that the effect of the pulse delay time can be allowed for when setting the pulse deletion time.

We must calculate the value of pdy which will give the required pulse delay time:

$$t_{pdy} = \frac{pdy}{f_{CARR} \times 512}$$

$$\Rightarrow \mathbf{pdy} = t_{pdy} \times f_{CARR} \times 512$$

$$= 5 \times 10^{-6} \times 6 \times 10^3 \times 512 = \mathbf{15.4}$$

However, the value of pdy must be an integer. As the purpose of the pulse delay is to prevent 'shoot-through' (where both top and bottom arms of the inverter are on simultaneously), it is sensible to round the pulse delay time up to a higher, rather than a lower figure.

Thus, if we assign the value 16 to pdy this gives a delay time of 5.2μs. From Table 6, pdy = 16 corresponds to a 6-bit PDY word of 110000 in temporary register R2.

4. Setting the pulse deletion time

In setting the pulse deletion time (i.e., the minimum pulse width) account must be taken of the pulse delay time, as the actual minimum pulse width seen at the PWM outputs is equal to t_{pd} - t_{pdy}.

Therefore, the value of the pulse deletion time, must, in this instance, be set to 5.2μs longer than the minimum pulse length required.

Minimum pulse length required = 10μs

$\therefore t_{PD}$ to be set = 10μs + 5.2μs = 15.2μs

Now,

$$f_{pd} = \frac{pdt}{f_{CARR} \times 512}$$

$$\Rightarrow \mathbf{pdt} = f_{pd} \times f_{CARR} \times 512$$

$$= 15.2 \times 10^{-6} \times 6 \times 10^{3} \times 512 = \mathbf{46.7}$$

Again, *pdt* must be an integer and so must be either rounded up or down - the choice of which will depend on the application. Assuming we choose in this case the value 46 for pdt, this gives a value of t_{pd} of 15 μs and an actual minimum pulse width of 15 - 5.2 μs = 9.8 μs.

From Table 7, *pdt* = 46 corresponds to a value of PDT, the 7-bit word in temporary register R0 of 1010010.

The data which must be programmed into the three temporary registers R0, R1 and R2 (for transfer into the initialisation register) in order to achieve the parameters in the example given, is shown in Fig. 15.

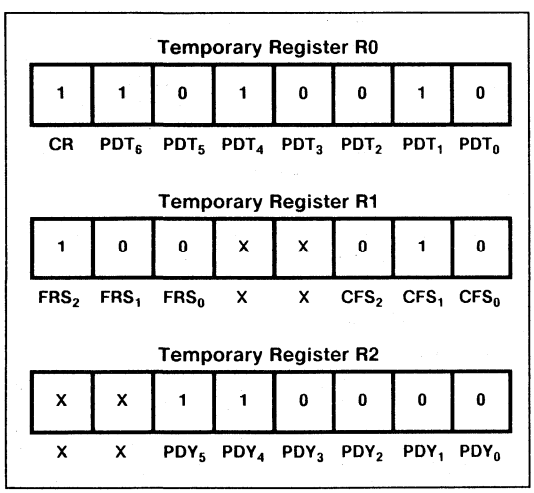


Fig.15

Control Register Programming Example

The control register would normally be updated many times whilst the motor is running, but just one example is given here. It is assumed that the initialisation register has already been programmed with the parameters given in the previous example.

A power waveform of 100 Hz is required with a PWM waveform amplitude of 80% of that stored in the EPROM. The phase sequence should be set to give forward motor rotation. The outputs should be enabled and no overmodulation is required.

1. Setting the power frequency

The power frequency, f_{POWER}, can be selected to 12-bit accuracy (i.e. 4096 equal steps) from 0 Hz to f_{RANGE} as defined in the initialisation register. In this case, with f_{RANGE} = 250Hz the power frequency can be adjusted in increments of 0.06 Hz.

$$f_{POWER} = \frac{f_{RANGE}}{4096} \times pfs$$

$$\Rightarrow \mathbf{pfs} = \frac{f_{POWER} \times 4096}{f_{RANGE}} = \frac{100 \times 4096}{250} = \mathbf{1638.4}$$

We can only have pfs as an integer, so if we assign pfs = 1638 this gives f_{POWER} = 99.97 Hz. The 12-bit binary equivalent of this value gives a PFS word of 011001100110 in temporary registers R0 and R1.

2. Setting overmodulation, forward/reverse, output inhibit

Overmodulation is not required therefore overmodulation bit = 0.

Forward motor control is required, (i.e., the phase sequence of the PWM outputs should be red-yellow-blue) therefore forward/reverse bit = 0.

Output inhibit should be inactive (i.e., the outputs should be active), therefore the output inhibit bit = 1.

These bits are all set in temporary register R1.

3. Setting the power waveform amplitude

$$A_{POWER} = \frac{A}{255} \times 100\%$$

$$\Rightarrow \mathbf{A} = \frac{A_{POWER} \times 255}{100} = \frac{80 \times 255}{100} = \mathbf{204}$$

The 8-bit binary equivalent of this value gives an AMP word of 11001100 in temporary register R2.

The data which must be programmed into the three temporary registers R0, R1 and R2 (for transfer into the control register) in order to achieve the parameters in the example given, is shown in Fig. 16.

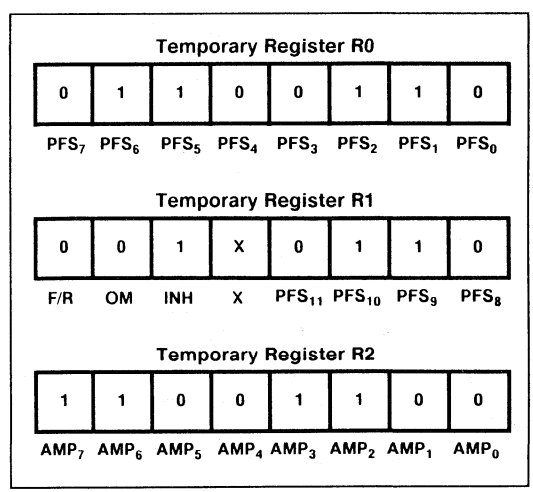


Fig.16

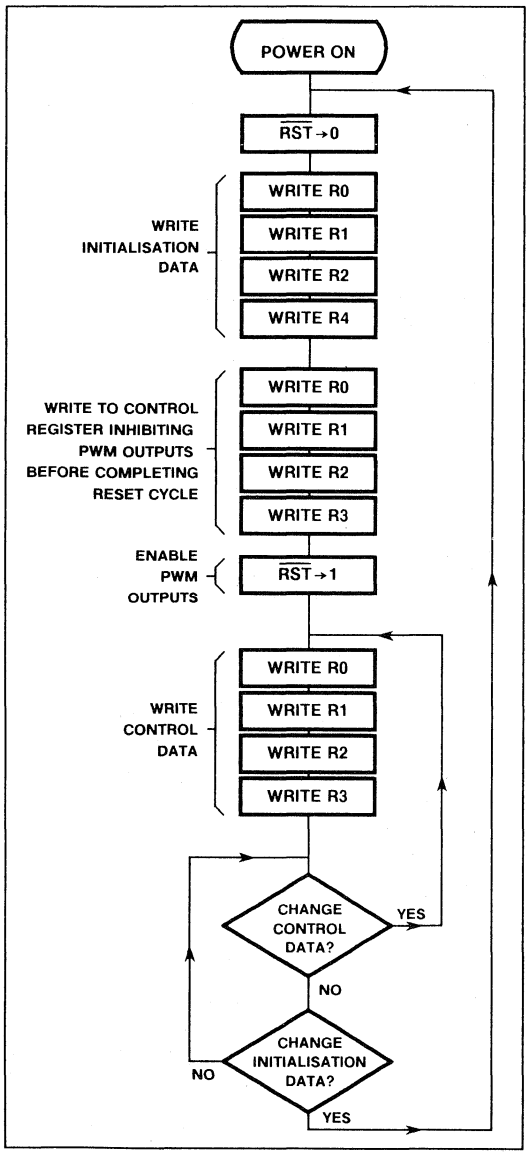


Fig.17 Typical MA828 programming routine

HARDWARE INPUT/OUTPUT FUNCTIONS

Set Output Trip (SET TRIP input)

The SET TRIP input is provided separately from the microprocessor interface in order to allow an external source to override the microprocessor and provide a rapid shutdown facility. For example, logic signals from overcurrent sensing circuitry or the microprocessor 'watchdog' might be used to activate this input.

When the SET TRIP input is taken to a logic high, the output trip latch is activated. This results in the $\overline{\text{TRIP}}$ output and the six PWM outputs being latched low immediately. This condition can only be cleared by applying a reset cycle to the $\overline{\text{RST}}$ input.

It is essential that when not in use, this pin is tied low and isolated from potential sources of noise. On no account should this input be left floating.

The SET TRIP input is latched internally at the master clock rate in order to reduce noise sensitivity.

Output Trip Status ($\overline{\text{TRIP}}$ output)

The $\overline{\text{TRIP}}$ output indicates the status of the output trip latch and is active low.

Reset ($\overline{\text{RST}}$ input)

The $\overline{\text{RST}}$ input is active low and performs the following functions:

1. All PWM outputs are forced low (if not already low), thereby turning off the drive switches.
2. All internal counters are reset to zero (this corresponds to 0° for the red phase output).
3. When released, the rising edge reactivates the PWM outputs, resetting the output trip and setting the $\overline{\text{TRIP}}$ output high - assuming that the SET TRIP input is inactive (i.e. low).

Zero Phase Pulses (ZPPR, ZPPY, ZPPB outputs)

The zero phase pulse outputs provide pulses at the same frequency as the power frequency with a 1:2 mark-space ratio. When in the forward mode of operation the falling edge of ZPPR corresponds to 0° for the red phase, the falling edge of ZPPY corresponds to 0° for the yellow phase and the falling edge of ZPPB corresponds to the falling edge of the blue phase. In the reverse mode, the rising edge of ZPP corresponds to 0° for the relevant phase PWM output.

Waveform Sampling Synchronisation (WSS output)

This output provides a square-wave signal of 50% duty cycle at a frequency 1536 times higher than the fundamental of the power waveform. Each successive pulse of WSS corresponds to the MA828 reading the next location of the internal waveform ROM. It may be used, in conjunction with the ZPP signals, to monitor the position of the machine rotor and may form part of a closed loop speed control system such as slip compensation.

Clock (CLK input)

The CLK input provides a timing reference used by the MA828 for all timings related to the PWM outputs.

The microprocessor interface, however, derives all its timings from the microprocessor and therefore the microprocessor and the MA828 may be run either from the same or from different clocks.

WAVEFORM DEFINITION

The waveform amplitude data used to construct the PWM output sequences is read from an internal 384×8 ROM. This contains the positive 90° span of the waveform as shown in Fig. 18. Each successive 8-bit sample linearly represents the instantaneous amplitude of the waveform. It is assumed that the data is symmetrical about the 90°,180° and 270° axes. The MA828 reconstructs the full 360° waveform by reading the 0-90° section held in ROM four times and also assigning negative values for the second half of the cycle.

The MA828 uses these samples to calculate the three instantaneous amplitudes for all three phases, which will be 120° transposed in the normal R-Y-B orientation for forward rotation or in the B-Y-R orientation for reverse rotation. The 384 eight-bit samples are regularly spaced over the 0° to 90° span giving an angular resolution of approximately 0.23°.

Waveform segment	Sample number
0° - 30°	0 - 128
30.23° - 60°	129 - 256
60.23° - 89.77°	257 - 383

Table 8. 180° of the 360° cycle is divided into 768 8-bit samples

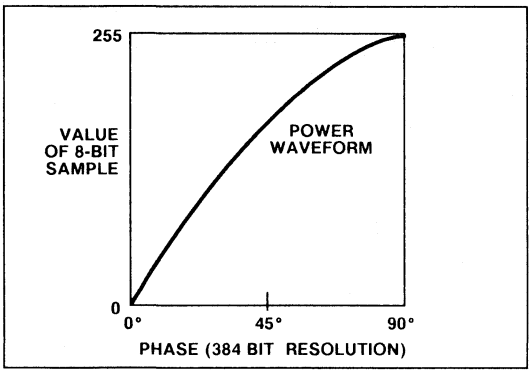


Fig.18 90° sample of typical power waveform

PRODUCT DESIGNATION

Two standard options exist defining waveform shape. These are designated the MA828-1 and MA828-2 as follows:

MA828-1

Sine + third harmonic at one sixth the amplitude of the fundamental:

$$x(t) = A\left[\sin(\omega t) + \frac{1}{6}\sin(3\omega t)\right]$$

MA828-2

Pure sinewave:

$$x(t) = A\sin(\omega t)$$

Additional wave shapes may be implemented to order, provided they are symmetrical about the 90°, 180° and 270° axes. Contact GEC Plessey Semiconductors for further details.

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{DD} = 5V ± 5%, T_{amb} = 25°C

Characteristic	Symbol	Min.	Typ.	Max.	Units	Conditions
Input high voltage	V_{IH}	2		-	V	
Input low voltage	V_{IL}	-		0.8	V	
Input leakage Current	I_{in}	-		10	µA	$V_{IN} = V_{SS}$ or V_{DD}
Output high voltage	V_{OH}	4.0	>4.5	-	V	I_{OH} = -4mA
Output low voltage	V_{OL}	-	<0.2	0.4	V	I_{OL} = 4mA
Supply current (static) (dynamic)	$I_{DD\ (static)}$ $I_{DD\ (dynamic)}$		<10	100 20	µA mA	All outputs open cct. CLK = 10MHz.
Supply Voltage	V_{DD}	4.75	5.0	7.5	V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{DD} = 5V ± 5%, T_{amb} = 25°C

Characteristic	Symbol	Min.	Typ.	Max.	Units	Conditions
Clock frequency	f_{CLK}			12.5	MHz	M:S ratio 1:1 ± 20%
SET TRIP = 0 →Outputs tripped →$\overline{TRIP}$ = 0	t_{TRIP}		$2/f_{CLK}$ $2/f_{CLK}$	$3/f_{CLK}$ $3/f_{CLK}$	s s	

NOTE 1. For microprocessor interface timings see Intel and Motorola bus timings (Tables 1 and 2).

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	10V
Voltage on any pin	V_{SS}-0.3V to V_{DD} + 0.3V
Current through any I/O pin	± 10mA
Storage temperature (see note)	-65°C to + 125°C
Operating temperature range (see note)	0°C to + 70°C

NOTE: These temperature ranges apply to all package types. Many package types are available and extended temperature ranges can be offered for some packages. Further information is available on request.

Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

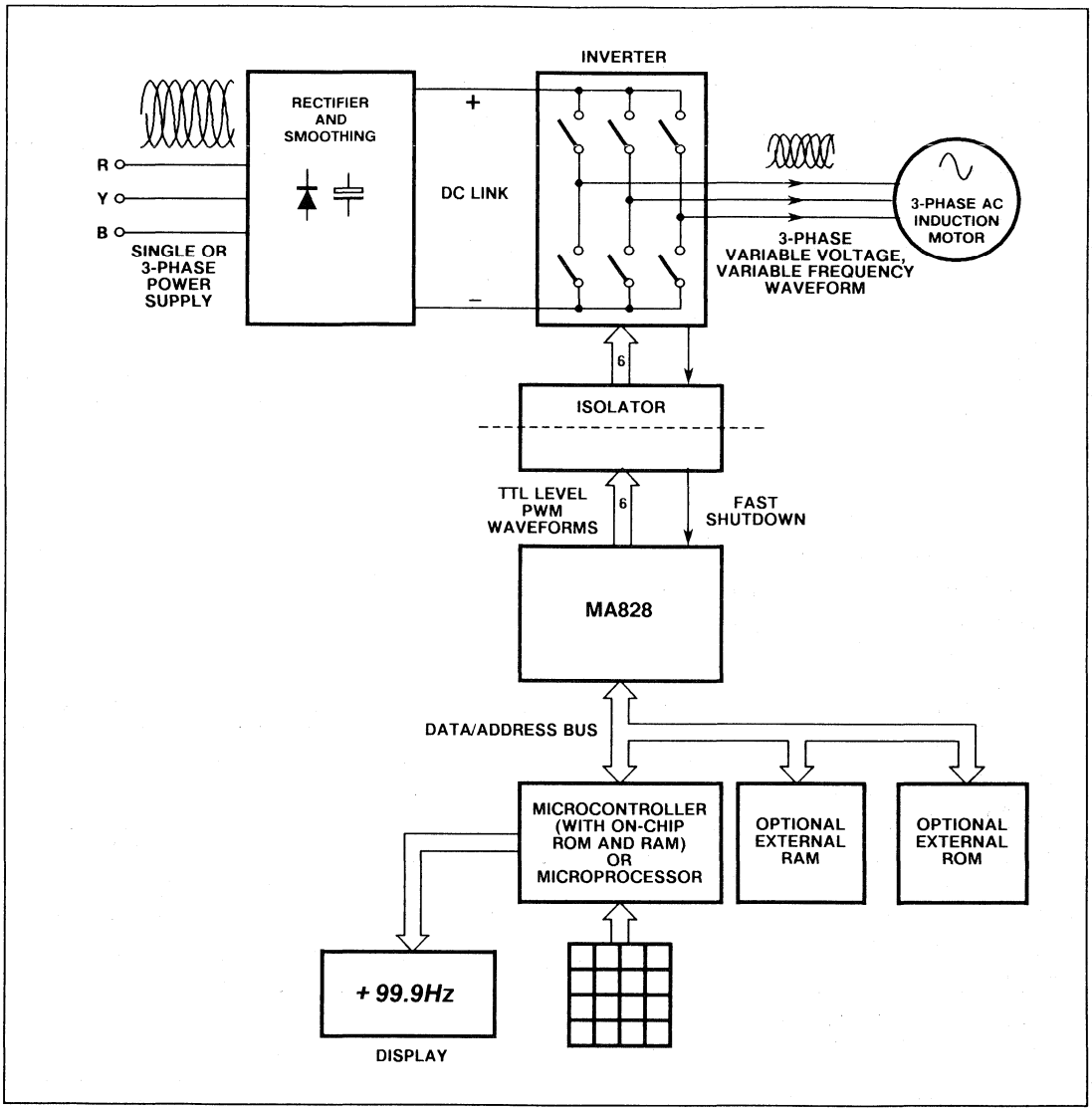


Fig.20 Typical MA828 application

MA838 FAMILY

SINGLE PHASE PULSE WIDTH MODULATION WAVEFORM GENERATOR

The MA838 PWM generator has been designed to provide waveforms for the control of variable speed AC machines, uninterruptible power supplies and other forms of power electronic devices which require pulse width modulation as a means of efficient power control.

Two TTL level PWM outputs control the upper and lower switches in an inverter arm. This is usually via an external isolation and amplification stage.

Information contained within the pulse width modulated sequences controls the shape, power frequency and amplitude of the output waveform. Parameters such as the carrier frequency, minimum pulse width, and pulse delay time may be defined during the initialisation of the device. The pulse delay time (underlap) controls the delay between turning on and off the two power switches in the inverter, in order to accomodate variations in the turn-on and turn-off times of families of power devices.

The MA838 is easily controlled by a microprocessor and its fully-digital generation of PWM waveforms gives unprecedented accuracy and temperature stability. Precision pulse shaping capability allows optimum efficiency with any power circuitry. The device operates as a stand-alone microprocessor peripheral, reading the power waveform directly from an internal ROM and requiring microprocessor intervention only when operating parameters need to be changed.

An 8-bit multiplexed data bus is used to receive addresses and data from the microprocessor/controller. This is a standard MOTEL™ bus, compatible with most microprocessors/controllers.

FEATURES

- Fully Digital Operation
- Interfaces with most Microprocessors
- Wide Power-Frequency Range
- 12-Bit Speed Control Accuracy
- Carrier Frequency Selectable up to 24kHz
- Waveform Stored in Internal ROM
- Double Edged Regular Sampling
- Selectable Minimum Pulse Width and Underlap Time
- DC Injection Braking

MOTEL is a registered trademark of Motorola corp. and Intel corp.

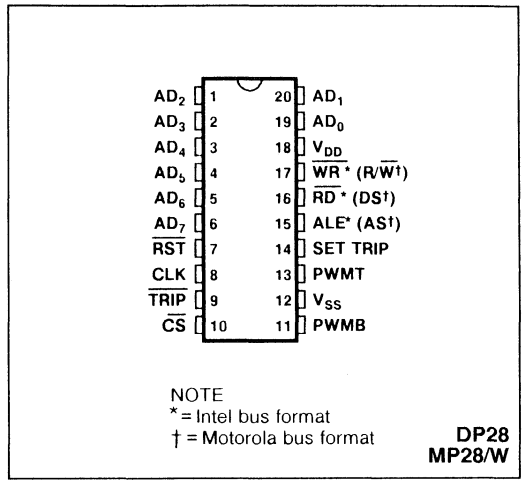


Fig.1 Pin connections - top view

Rotational frequency is defined to 12 bits for high accuracy and a zero setting is included in order to implement DC-injection braking with no software overhead.

This family is functionally identical to the MA828 PWM generator IC except that only one PWM channel is provided. Two standard waveshapes are available to cover most applications:

MA838-1
Sine plus third harmonic at one sixth the fundamental amplitude (Drive Systems).

MA838-2
Pure sinewave (Waveform Generation)

In addition, any symmetrical waveshape may be integrated on-chip to order. More detailed information on the MA838 may be obtained by referring to the MA828 data sheet.

The MA838 is fabricated in CMOS for low power consumption.

Section 7
Precision Timers

3093-1.0

ZN1034D, ZN1034E

PRECISION COUNTER TIMER

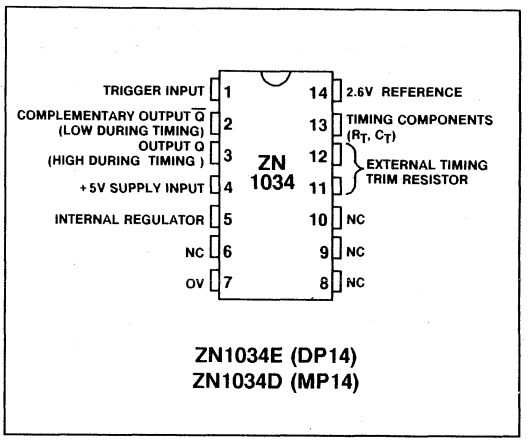
By combining complex linear and digital functions on the same chip, the ZN1034 enables the construction of simple precision timers using low cost components.

The frequency of an on-chip oscillator is determined by an externally connected capacitor and resistor. Fine adjustment of the frequency can be achieved by varying the value of an external trimming resistor. Pulses from the oscillator are fed into a 12 stage binary divider and the output changes state after 4095 pulses.

In this way precise time periods can be defined by timing capacitors and resistors of much smaller values than would be required by a single RC time constant timer.

A control circuit enables the division, or count, to begin when either (a) with trigger input LO the supply goes HI (supply initiation), or (b) with supply HI the trigger input goes LO (trigger initiation).

The IC can operate from normal +5V logic supplies or from any higher voltage by using a suitable voltage dropping resistor and by connecting the internal shunt regulator to the supply pin.



ZN1034E (DP14)
ZN1034D (MP14)

Fig.1 Pin connections - top view

FEATURES

- Time Periods up to 7500 CR
- Time Period Trimming Facility
- Repetitive Timing 0.01%
- Temperature Stability 0.01%/°C
- Complementary TTL Compatible Outputs
- Supply or Trigger Input Timing Initiation
- On-Chip Regulator or TTL Supply Option
- Available in Miniature Plastic DIL (MP14) Package

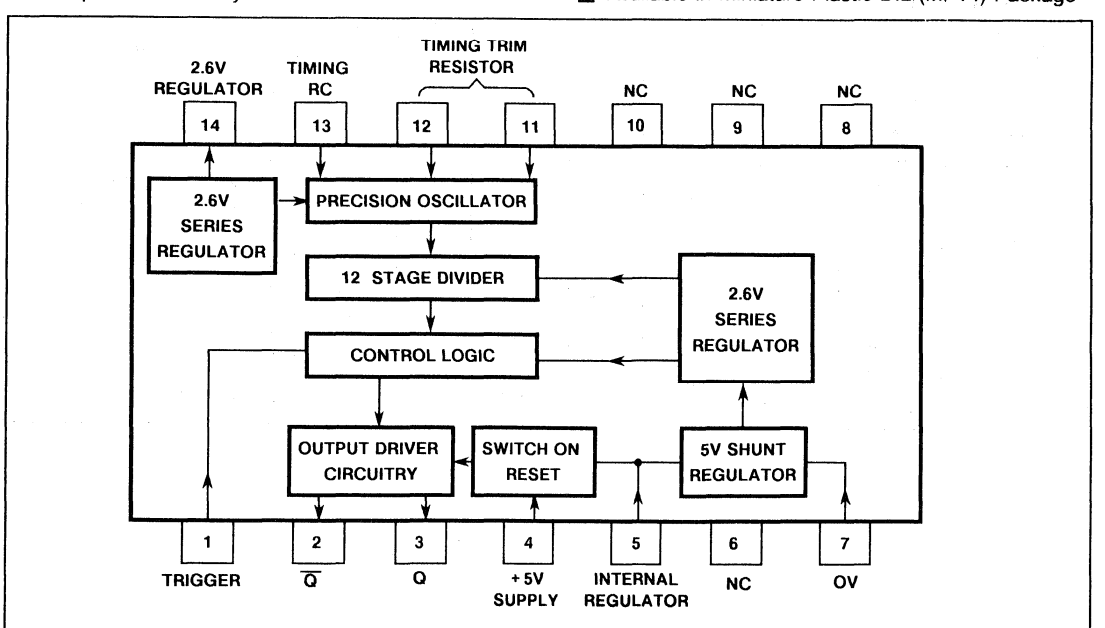


Fig.2 System diagram

ABSOLUTE MAXIMUM RATINGS

Dissipation	250mW derate above 30°C at 5mW/°C
Output source current	25mA
Output sink current	25mA
Operating temperature range	0°C to +70°C
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions unless otherwise :

T_{amb} = 25°C

		Value				
Characteristic	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
Timing section						See Note 1
Timing resistor	R_T	3.3k		5M	Ω	See Figs.6 and 7
Timing capacitor	C_T	1			nF	See Figs.6 and 7
Time multiplying factor	K_0		2800			R_{TRIM} = 0
	K_{50}		3700			R_{TRIM} = 50kΩ
						R_T > 12kΩ, C_T > 33nF
Multiplying factor time resistor	R_{TRIM}	0		500	kΩ	See Note 2
Trimming range	T_P		±50		%	R_{TRIM} = 0 to 500kΩ
			±25		%	R_{TRIM} = 0 to 100kΩ
			±12		%	R_{TRIM} = 0 to 50kΩ
Multiplying factor temperature coefficient			±0.01		%/°C	R_{TRIM} = 0
			±0.08		%/°C	R_{TRIM} = 500kΩ
Repetitive timing error			0.01		%	
Multiplying factor linearity			±2		%	1MΩ > R_T > 12kΩ See Fig.7
Multiplying factor/supply voltage coefficient			1		%/V	
External clock input						
Frequency				250	kHz	Clock input to pin 12 via a 10kΩ resistor
Drive current	I_{clk}		0.1		mA	
Pulse width	t_{clk}	1			μs	
Pulse amplitude	V_{clk}	3.0		6	V	
Timing initiation and reset						
(a) Supply voltage initiation						
Voltage to initiate timing	V_{CC}	4.7			V	Supply applied to pin 4 with pin 1 connected to pin 7
Rate of change of V_{CC}				0.25	V/μs	
(b) Trigger input initiation						
Voltage to initiate timing	$V_{T(LO)}$			1	V	Trigger input applied to pin 1
Voltage to prevent initiation of timing	$V_{T(HI)}$	2.2			V	
Minimum pulse to trigger			2		μs	
(c) Supply voltage reset						
Voltage to reset	V_{CC}		3.6		V	See Note 3

ELECTRICAL CHARACTERISTICS (cont.)

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Output drive Q to $\bar{Q}$						V_{CC} = 5V
Output voltage	$V_{O(HI)}$	2.5	3.6		V	$I_{O(HI)}$ = –25mA
	$V_{O(LO)}$		0.2	0.4	V	$I_{O(LO)}$ = 25mA
Output current	$I_{O(HI)}$			–25	mA	Source
	$I_{O(LO)}$			25	mA	Sink
Rise time	t_r		300		ns	I_O = 5mA, V_{CC} = 5V
Fall time	t_f		100		ns	I_O = 5mA, V_{CC} = 5V
Propagation delay V_T Low to V_O High	t_p		2		μs	
Power supply						
(a) Externally regulated						Connected to pin 4
Supply voltage	V_{CC}	4.7	5.0	5.3	V	
Supply current	I_{CC}		3.5	5.0	mA	V_{CC} = 5V Output unloaded
(b) Internally regulated (5V shunt regulator)						Connect pin 4 to pin 5
Operating current range	I_R	7		55	mA	See Note 4
Regulated voltage	V_R	4.7	5.0	5.3	V	I_R = 10mA
Slope resistance			1		Ω	I_R = 7 – 55mA
Regulated voltage change with temperature			35		mV	I_R = 7 – 55mA t = 0°C to +70°C
Reference voltage (2.6V series regulator)						
Regulated voltage	V_{REF}	2.4	2.6	2.8	V	V_{CC} = 5V pin 14 unloaded
Load current	I_{REF}			5	mA	V_{CC} = 5V
Output resistance			15	40	Ω	
Regulated voltage change with temperature			10		mV	V_{CC} = 5V, t = 0°C to +70°C pin 14 unloaded

NOTES
1. With R_{TRIM} = 100kΩ maximum.
2. For R_{TRIM} > 100kΩ the maximum value of R_T is 1MΩ.
3. In order to reset the timer the supply voltage should be reduced to 2V although reset may be typically achieved at 3.6V. Reset will not occur with the supply greater than 4V.
4. Since the +5V regulator cannot be used on its own without the rest of the circuit, the minimum operating current includes the 5mA maximum supply current taken by the timer circuits.

THE TIMING FUNCTION

Fixed Time Period

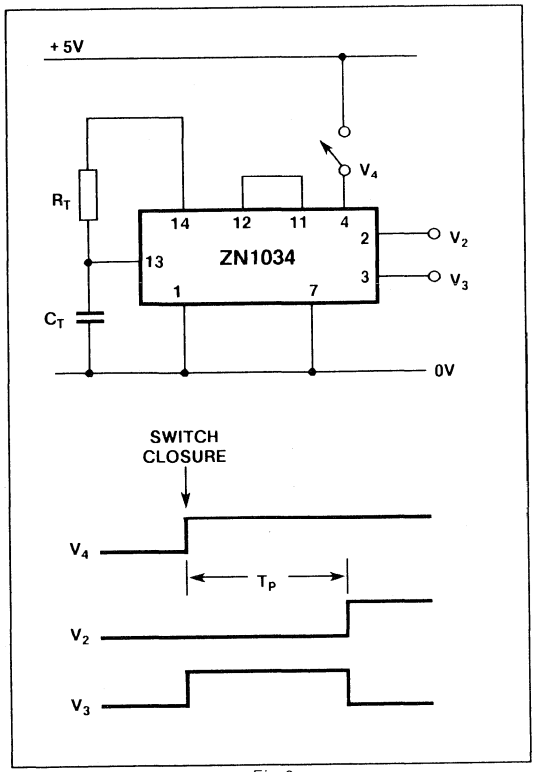


Fig.3

External components R_T and C_T determine the length of the period T_p and if values of R_T > 12kΩ and C_T > 33nF are used then the relationship $T_p = K C_T R_T$ applies and the time multiplying factor K = 2800 ± 10%.

(The timing components set the period of an internal oscillator to 0.68 $C_T R_T$ ± 10% and an internal divider causes a change in the output state after 4095 oscillator cycles).

When the time period is initiated pin 3 goes HI for a time period T_p. On completion of the time period, pin 3 goes LO and pin 2, which was previously LO goes HI and remains HI until the timing sequence is re-initiated.

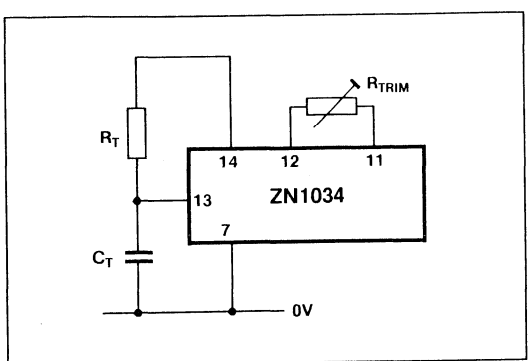


Fig.4

Trimming the Time Period

The time period multiplier K varies with the value of external resistance between pins 11 and 12 (R_{TRIM}). Hence the time period for given values of timing components R_T and C_T can be independently trimmed.

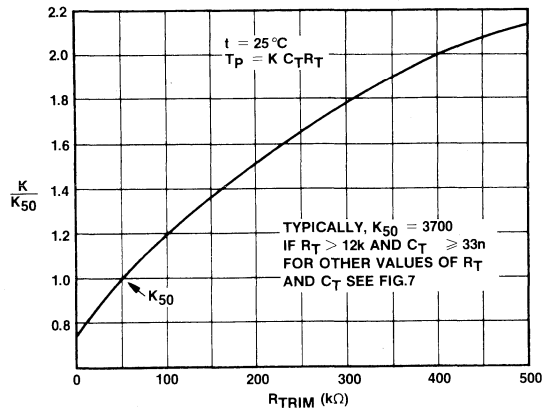


Fig.5

The graph Fig.5 gives the variation of time period multiplier with R_{TRIM} normalised to the value of multiplier obtained for R_{TRIM} = 50kΩ (referred to as K_{50}).

For values of R_T > 12kΩ and C_T > 33nF

Typically K_{50} = 3700 ± 10%

Choosing R_{TRIM} = 50kΩ makes it possible to provide a ±25% trim on the time period obtained when a 100kΩ potentiometer connected between pins 11 and 12 is set at mid-point. Such a trim would enable inexpensive wide tolerance timing components to be used in an accurate timer.

Design of Variable Period Timers

Time periods from 16ms to infinity theoretically may be obtained using the ZN1034 integrated timer circuit. However the designer is usually limited by component availability and other restrictions to a narrower range than this. The following section should enable the designer to get the best possible circuit configuration to be achieved within the design limits. The necessary information is presented below in the form of a Timing component guide and a graph of Time period multiplier variation with the time period. All graphs have been plotted using a 100k variable resistor set at mid-point for R_{TRIM}.

For the component guide and the graph of multiplier against time period the value of R_{TRIM} has been chosen as a 100kΩ variable resistor at mid-point setting thus giving a possible change of approximately ±25% on time periods obtained from the graph.

Timing Component Guide

The graph, Fig.6, gives an idea of the values of timing components necessary for a given time period. It is plotted assuming a 100kΩ variable resistor between pins 11 and 12 is set at mid-point. The periods obtained with the timing components selected from the graph may be trimmed with the variable resistors to the exact time required.

The maximum range possible for a particular value of timing capacitor can easily be obtained from the graph. For example, a range of 50ms to 75 seconds can be achieved with a 3.3nF capacitor or 40 seconds to 1000 minutes with 3.3μF.

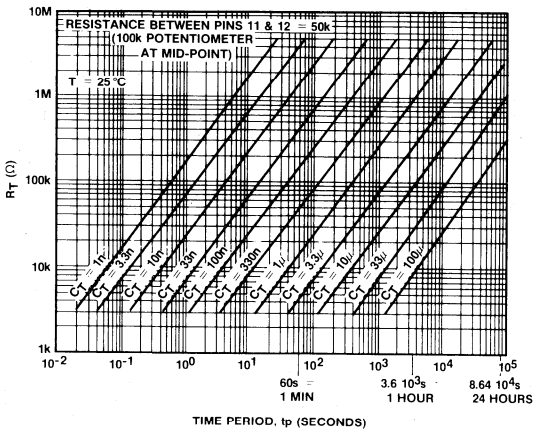


Fig.6

Variation of Time Period Multiplier with Time Period

The linear relationship implied by the equation

$$T_P = K C_T R_T$$

is modified when extreme values of timing components are used. Typical variations in the multiplier, K, are shown in Fig.7, again assuming that a 100kΩ variable resistor set at mid-point is connected between pins 11 and 12. Using this graph the example of the 3.3nF capacitor which was used to illustrate the timing component guide graph above will be seen to give a slightly different range, 52ms to 74 seconds for a 3.3kΩ to 5MΩ change in R_T.

The multiplier (K_{50}), for this example, varies from a minimum of 4200 to a maximum of 4975, a total variation of ±8.5%.

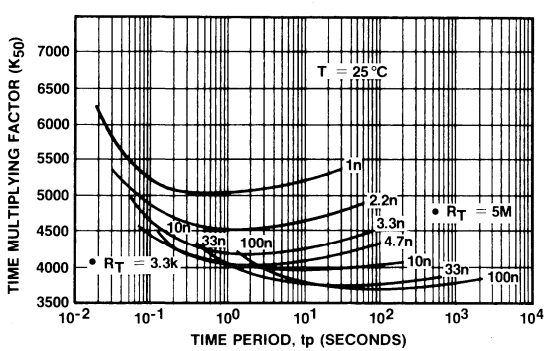


Fig.7

Fig.7 may be used to determine the linearity of the time period variation with timing resistance for various values of timing capacitor and for various ranges of time period as illustrated by the following examples.

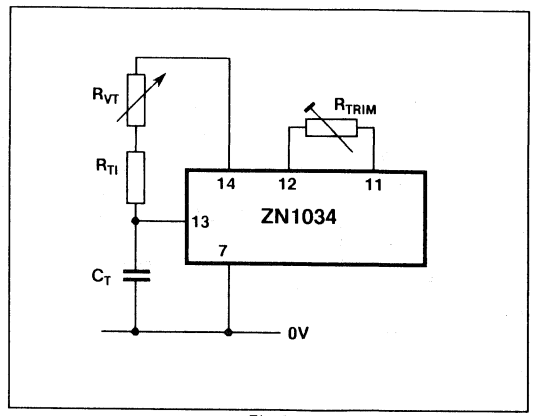


Fig.8

Designing a 1500 : 1 Variable Timer

A wide range continuously variable timer circuit is shown in Fig.8 and if the values of the above example are used then a variation of approximately 1 : 1500 is obtained (or 50ms : 75 seconds).

For $R_{TI} = 3.3k\Omega$

$R_{VT} = 5M\Omega$

$R_{TRIM} = 50k\Omega$ (100kΩ variable resistor set to mid-point)

$C_T = 3.3nF$

The maximum period $T_{P(MAX)} = K C_T (R_{VT} + R_{TI})$ and the minimum period $T_{P(MIN)} = K C_T R_{TI}$

Hence the range is $1 : \dfrac{T_{P(MAX)}}{T_{P(MIN)}}$

i.e. $1 : \dfrac{R_{VT}}{R_{TI}} + 1$

approximately $1 : \dfrac{R_{VT}}{R_{TI}}$

If the variable resistor R_{VT} is scaled linearly in terms of time period then the predicted linearity error for Fig.7 will be ±8.5%.

A 400 : 1 Linearly Variable Timer

Restricting the range to about 400 : 1 enables the designer to achieve a better linearity than the 1500 : 1 timer. The design of the circuit of Fig.9 illustrates this point.

$R_{T(MAX)} = 5M\Omega$

$R_{T(MIN)} = 12k\Omega$

$C_T = 33nF$

$R_{TRIM} = 50k\Omega$

range is $1 : \dfrac{5 \times 10^6}{12 \times 10^3} + 1$

i.e. 1:418

The values selected are such as to give approximately

$T_{P(MIN)} = 1.5$ seconds from graph, Fig.6

and $T_{P(MAX)} = 10$ minutes from graph, Fig.6

These values are used to obtain those of K_{50} from the graph of Fig.7.

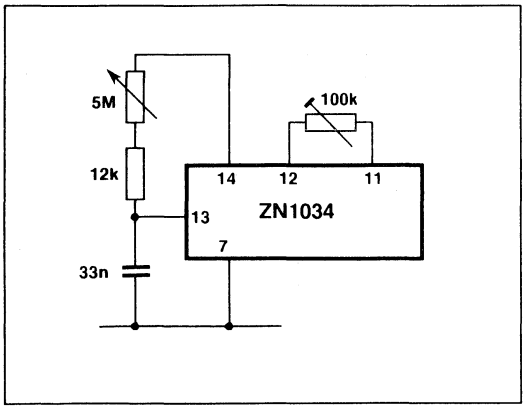


Fig.9

The maximum value of K_{50} = 3950 from Fig.7 and the minimum value of K_{50} = 3800 from Fig.7.

This indicates that the maximum linearity error is ±2%. (Excluding errors due to R_{VT} end resistance at minimum settings).

A wide range timer with switched timing resistors can be designed in a similar manner to the circuit shown in Fig.8.

Switched resistors are preferable in some circumstances for setting the time period of timer circuits. In addition to the ability to set a time precisely, advantage can be taken of the capability of the ZN1034 circuit of operating linearly over a wide range of values of timing resistor up to 5M. There is also the possibility of correcting for errors at the extremes of the range if this is thought worthwhile.

The design of the timer illustrated in Fig.10 can be taken as an example. Here the aim is to achieve a 0.1 to 99.9 second range with an accuracy consistent with the use of 1% resistors.

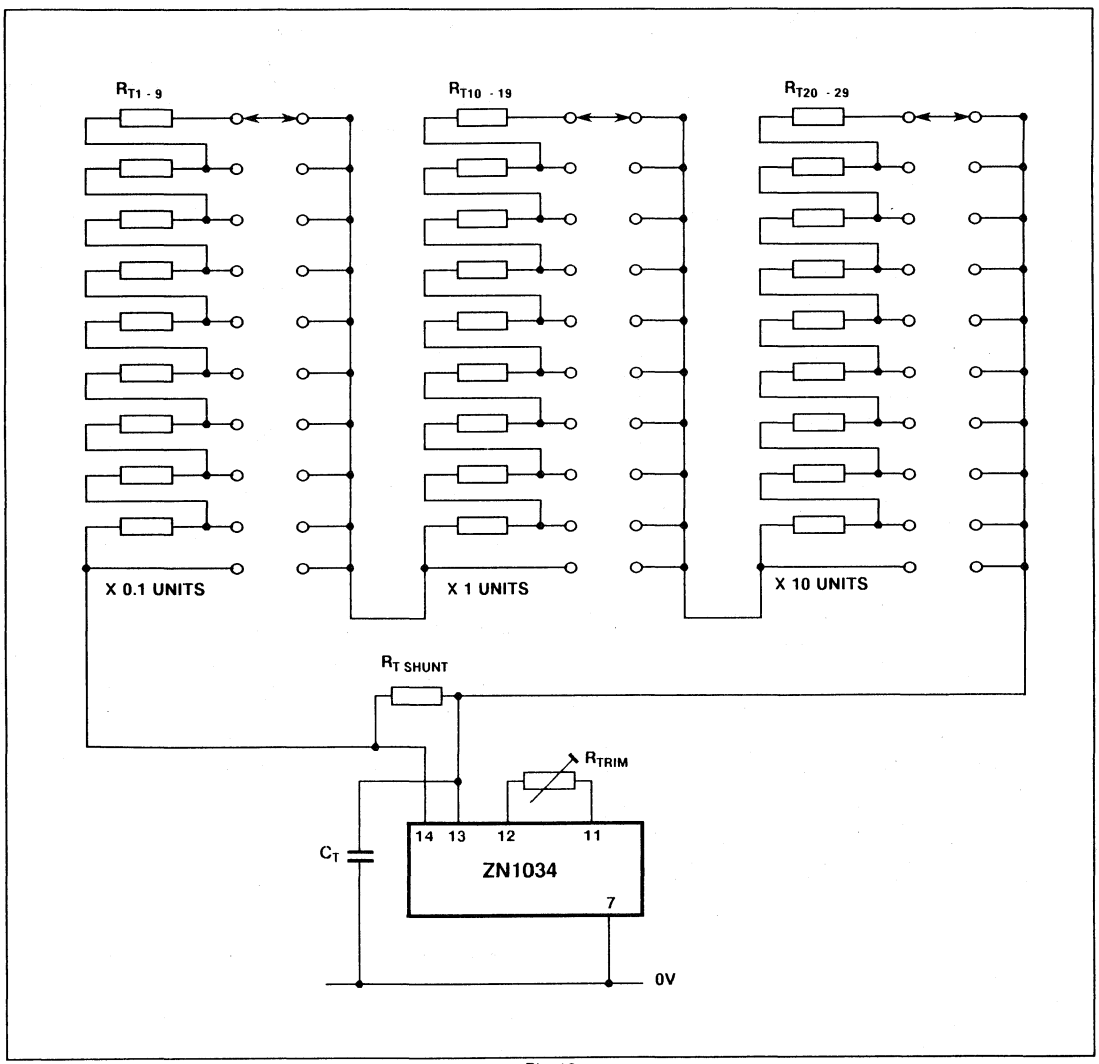


Fig.10

Fig.6 shows that for the maximum time of about 100 seconds R_T is required to be about 5MΩ and the value of C_T to be between 3.3nF and 10nF.

Fig.7 indicates that a 4.7nF capacitor will give 100 seconds with 5MΩ and the 4.7nF curve shows a minimum value of K_{50} of 4030 at 2 seconds and a value of 4280 at 100 seconds, an error of +7% on the linearity taking 2 seconds as standard.

Such a steady increase of time error can be corrected by shunting the switched resistors by the appropriate high value, $R_{T(SHUNT)}$. The value required in this particular case will be such as to reduce $R_{T(MAX)}$ by 6%.

$$\text{i.e. } R_{T(SHUNT)} = 5M\Omega\left[\frac{100-6}{6}\right]$$

$$= 82M\Omega \text{ (nearest preferred value)}$$

This will have no effect on the linearity error at the bottom end of the range.

Assuming the effect of the variation in multiplying factor over the production spread of devices and also the capacitor tolerance is trimmed out by R_{TRIM} we can specify the resistors as:

$$R_{T1} - R_{T9} = 5.1k\Omega \pm 0.5\%$$
$$R_{T10} - R_{T19} = 51k\Omega \pm 0.5\%$$
$$R_{T20} - R_{T29} = 510k\Omega \pm 0.5\%$$
$$\text{and } C_T = 4.7nF \pm 5\%$$

Typical errors derived from the graph shown in Fig.7 (multiplying factor against time), are shown in Table 1.

NOTES (See Table 1)

1. The timing resistance as specified above but allowing for the effect of an 82MΩ overall shunt resistor. (Only the significant values shown).
2. The multiplying factor used in the calculation of the time period should strictly be that pertaining to the calculated time which will differ from the set time by the error. Since this error is small, the error in using the set time to derive the multiplying factor from the graph is negligible.
3. Normalising the error by adjusting the trim resistor to give correct timing on the 10 second setting.
4. The timing resistors as specified above but with 82MΩ overall shunt resistance and a 4.7kΩ in place of a 5.1kΩ for the 0.1 second position. (Only significant values shown).

Using shunt resistor correction						Using shunt and series resistor			
Timing period setting secs.	Multiplying factor	Timing resistance (Note 1) kΩ	Calculated time (Note 2) seconds	Calculated error %	Normalised error (Note 3) %	Timing resistance (Note 4) kΩ	Calculated time (Note 2) seconds	Calculated error %	Normalised error (Note 3) %
0.1	4475	5.1	0.107	+7	+10	4.7	0.099	-1.2	+1.8
0.2	4230	10.1	0.203	+1.5	+4.5	9.8	0.195	-2.6	+0.4
0.3	4150		0.298	-0.6	+2.4	14.9	0.291	-3.1	-0.1
0.4	4100		0.393	-1.8	+1.2	20.0	0.39	-3.7	-0.7
0.5	4080		0.489	-2.2	+0.8	25.1	0.48	-3.7	-0.7
0.6	4070		0.585	-2.4	+0.6	30.2	0.58	-3.7	-0.7
0.7	4062		0.681	-2.7	+0.3	35.3	0.67	-3.7	-0.7
0.8	4055		0.778	-2.8	+0.2	40.4	0.77	-3.8	-0.8
0.9	4050		0.873	-3.0	0	45.5	0.87	-3.8	-0.8
1.0	4045		0.970	-3.0	0	51.0	0.97	-3.0	0
1.1	4040		1.07	-3.2	-0.2	55.7	1.06	-3.9	-0.9
1.2	4040		1.16	-3.2	-0.2	60.8	1.15	-3.8	-0.8
1.3	4040		1.26	-3.2	-0.2	65.9	1.25	-3.7	-0.7
1.4	4040		1.36	-3.2	-0.2	71.0	1.35	-3.7	-0.7
1.5	4040		1.45	-3.2	-0.2	76.1	1.44	-3.7	-0.7
1.9	4040		1.84	-3.2	-0.2	96.5	1.83	-3.6	-0.6
2.0	4040		1.94	-3.2	-0.2	102.0	1.94	-3.2	-0.2
2.1	4040		2.03	-3.2	-0.2	106.7	2.03	-2.5	-0.5
3.0	4040		2.90	-3.2	-0.2	153.0	2.91	-3.2	-0.2
10.0	4070	507	9.70	-3.0	0	507.0	9.70	-3.0	0
11.0	4075	557	10.67	-3.0	0				0
13.0	4080	658	12.61	-3.0	0				0
20.0	4110	1008	19.46	-2.7	+3.0				+0.3
30.0	4150	1502	29.30	-2.3	+0.7				+0.7
80.0	4260	3889	77.86	-2.7	+0.3				+0.3
90.0	4275	4349	87.4	-2.9	+0.1				+0.1
99.9	4280	4800	96.6	-3.3	-0.3		96.6		-0.3

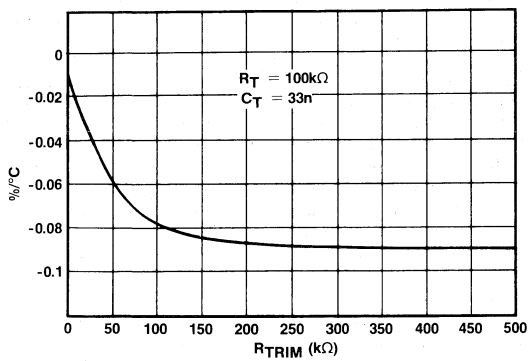
Table 1

The predicted maximum error is approximately ±5% of setting overall but with a shunt resistor across the switched resistors this can be reduced to ±0.5% for settings above 0.4 seconds. By altering one of the switched resistor values in addition to having a shunt resistor the overall predicted error becomes ±1.5% of setting.

N.B. Setting all three decade switches to zero should be avoided since this will disable the oscillator and stop the timer.

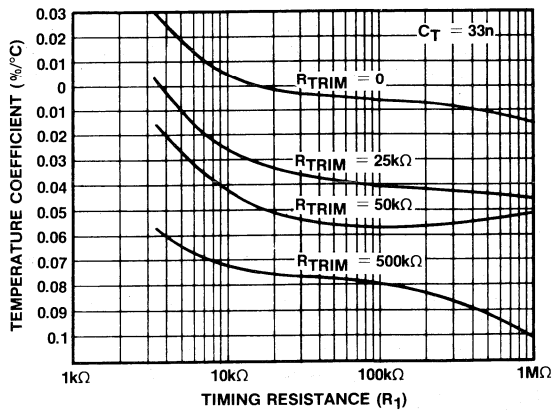
Effect of Temperature on Time Period

For optimum temperature coefficient of time period it is necessary to use as low a resistance as possible between pins 11 and 12 (R_{TRIM}) consistent with the maximum amount of adjustment of the time period required. This is illustrated by the graph Fig.11.



The effect of varying the value of the timing resistance on the time period temperature coefficient is shown in Fig.12.

Optimum temperature coefficient may be obtained with R_{TRIM} = 0, R_T = 20kΩ and C_T > 33nF.



INPUT AND OUTPUT CIRCUITS

External Clock

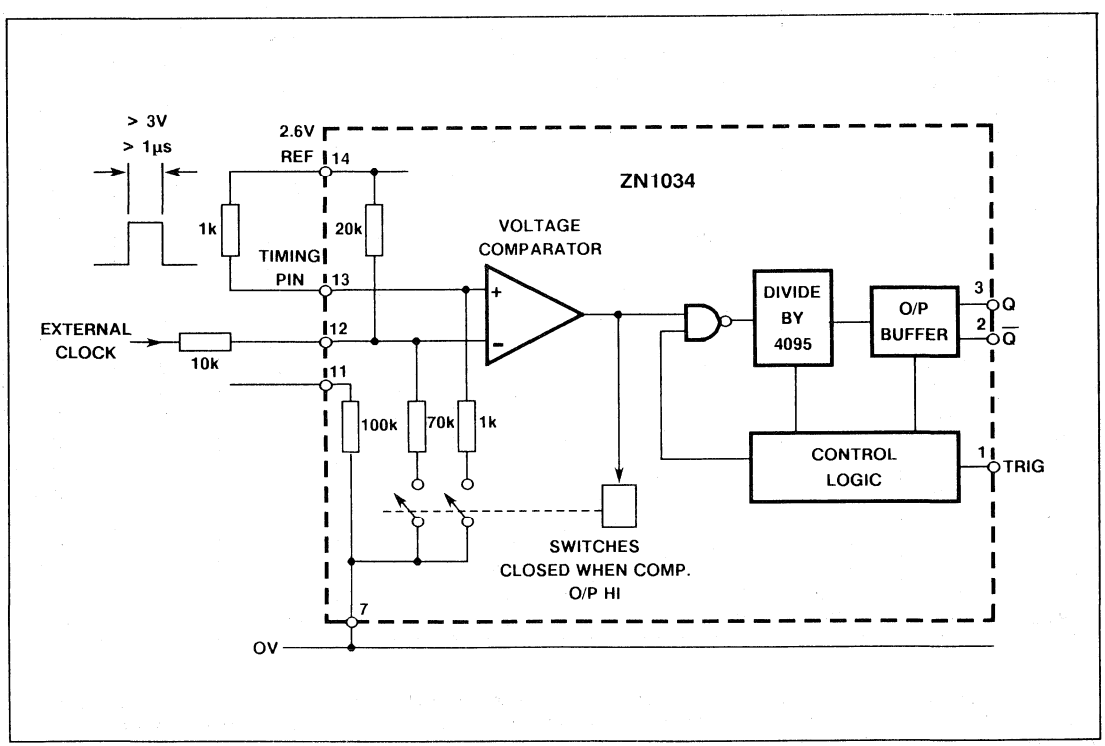


Fig. 13

The ZN1034 can be used with an external clock as shown in the circuit of Fig.13.

The internal clock is disabled by connecting a 1k resistor from the timing pin 13 to the +2.5V reference pin 14 thus preventing the non-inverting input to the amplifier dropping below the inverting input voltage. The amplifier output is therefore HI and the internal switches are closed.

An external clock pulse, provided it meets the limits defined in the characteristics, will override the disabling on pin 13 and, if the trigger input on pin 1 is LO, will cause a pulse to be passed to the divider circuit.

The output Q and $\overline{Q}$ will change from LO to HI and vice versa at the end of 4095 external clock pulses.

Timing Initiation and Reset (Fig.14)

Supply Initiated

When pin 1 is held LO and the supply is switched on, the control logic and counter are automatically reset as the supply rises to its ON voltage. This also initiates timing at the same instant by gating the oscillator output into the counter. After the set time (period 1), the outputs change state and remain thus until the supply is switched off or another period is initiated.

If, during such a timing cycle (period 2), the trigger input is taken HI, no matter how many times or for how long, the condition of the outputs and the length of the timing period will not be affected. If the supply drops below the reset level even for a few microseconds then the timing period will be terminated. It will be reset and restarted when the supply rises again above the reset level. Thus a supply drop-out has the effect of increasing the time period; Q output remains low for (period 2) plus (period 3).

Trigger Initiated

Allowing pin 1 to rise with the supply prevents timer initiation by the supply.

Pulling the trigger input LO now initiates a normal timing period (period 4). A further period may be initiated by dropping the trigger LO again (period 5). As for supply initiation, this period is not affected either in duration or in the condition of the outputs when the trigger input level is altered during timing. Similarly the period is terminated by the supply falling below the reset level but since the normal condition of the trigger is HI the timing will not restart on restoration of the supply. A supply drop-out during a trigger initiation timing period has the effect of reducing the set time.

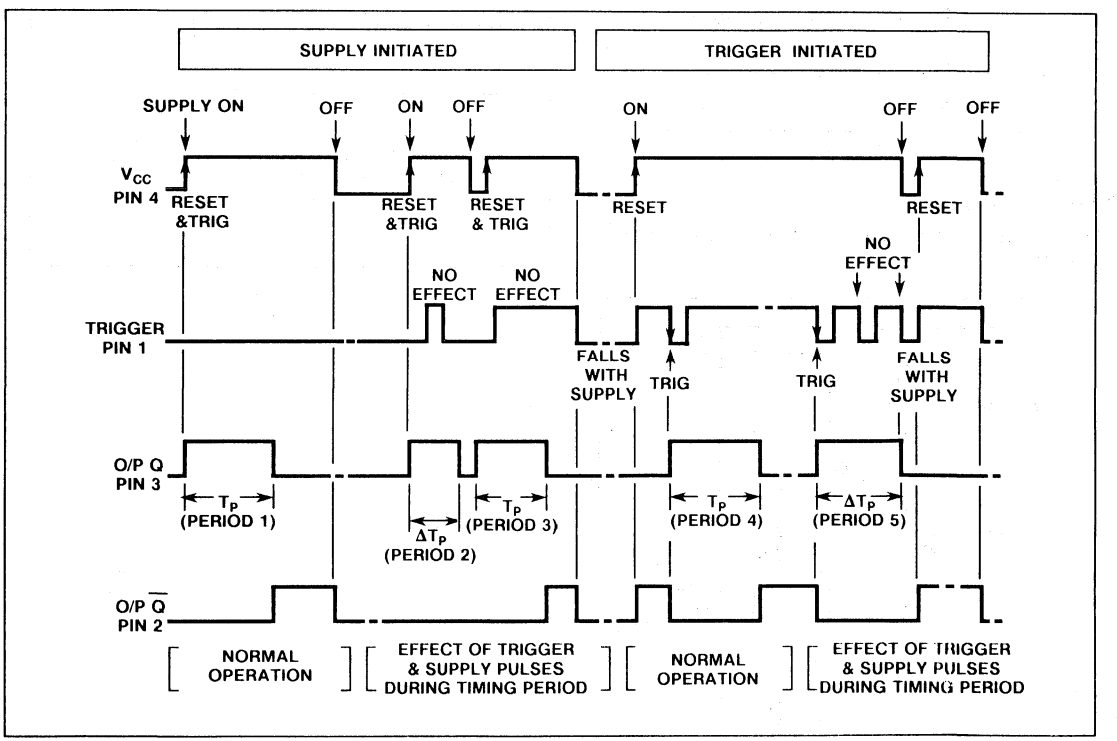


Fig. 14

Trigger Input Circuit (Fig.15)

The input is a Schmitt trigger circuit with a hysteresis of about 0.3V. With no input applied the input is pulled HI thus preventing initiation of the timer. When remote triggering is used with mechanical contacts it is advisable to provide a more positive pull-up of 10kΩ (shown dotted). A contact is then made between pins 1 and 7 to initiate timing.

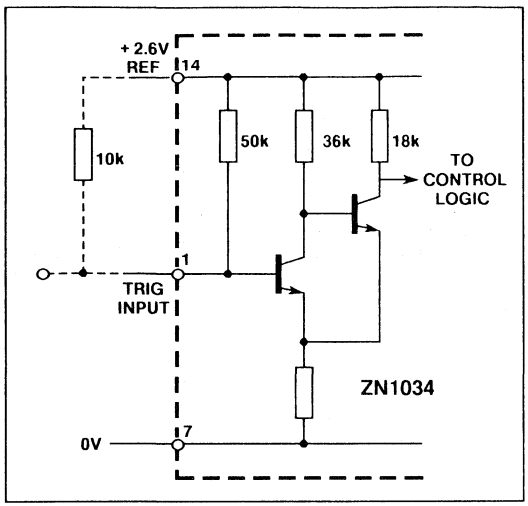


Fig. 15

Output Drive Circuits

The Q and $\overline{Q}$ output drive circuits both have the form illustrated in Fig.16.

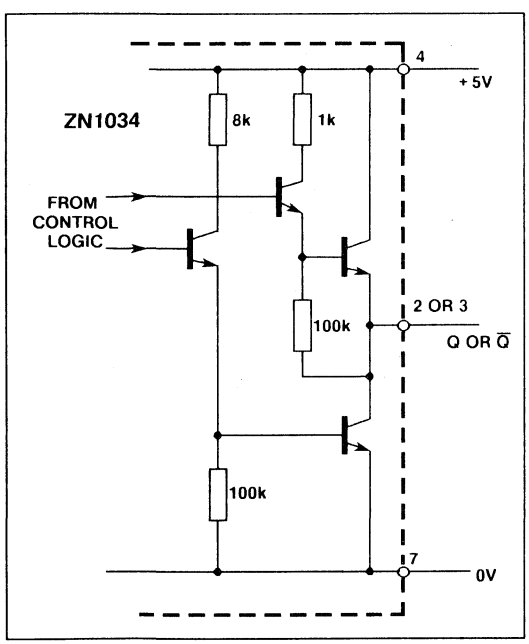
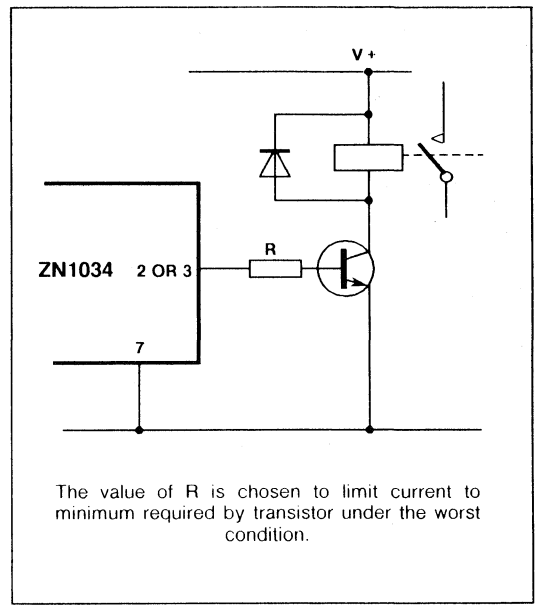


Fig. 16

An external resistor is required to limit the drive current to the requirements of the load circuit and to the current capability of the +5V supply taking into account the needs of the ZN1034 itself (minimum 5mA externally regulated or 7mA internally regulated).

Load Circuits

Transistor Driven Relay (Fig.17)



The value of R is chosen to limit current to minimum required by transistor under the worst condition.

Fig. 17

Thyristor Driven Relay (Fig.18)

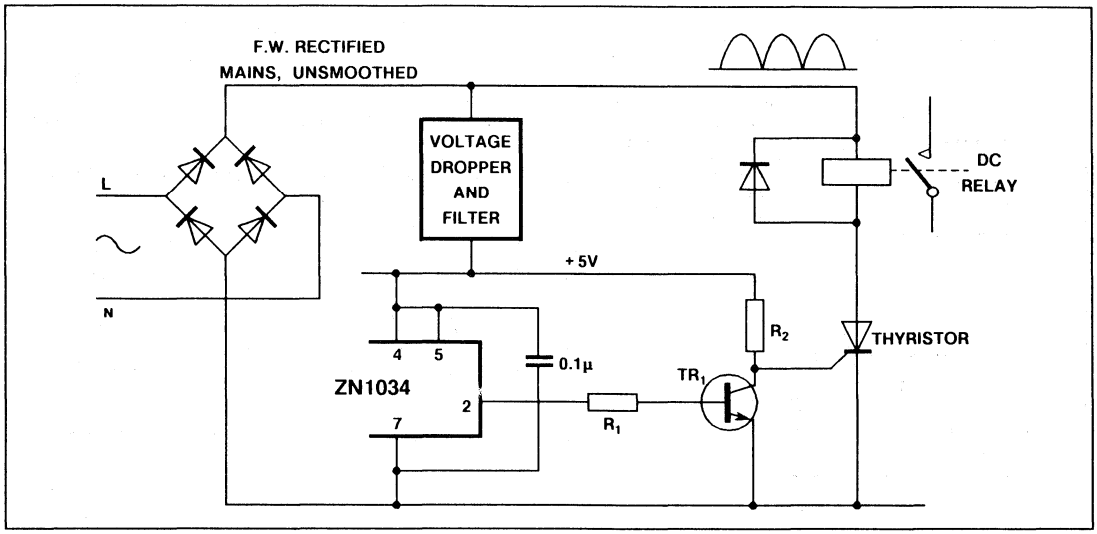


Fig.18

A thyristor gate may be driven via a limiting resistor directly from pin 2 for DELAY-TO-ON timers. Fig.18 illustrates a circuit for achieving DELAY-TO-OFF using a thyristor. R_2 can be as high as 10k for low gate current thyristors. The thyristor is chosen such that the reduction in gate-cathode impedance achieved with a saturated transistor is sufficient to increase the holding current to a value which ensures turn OFF and R_1 is chosen so that the transistor (T_{R1}) just reaches saturation.

For 240V AC mains it may be necessary to use a 110V DC relay with a dropping resistor of equal resistance since 220V DC relays are not easily obtainable.

Triac AC Load Circuit Positive Firing (Fig.19)

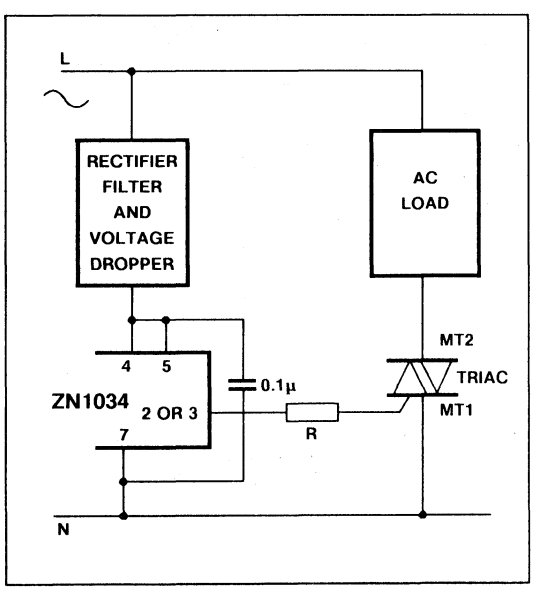


Fig.19

The value of R is chosen to limit the current to the minimum required by the triac for positive firing in both quadrants.

Triac AC Load Circuit Negative Firing (Fig.20)

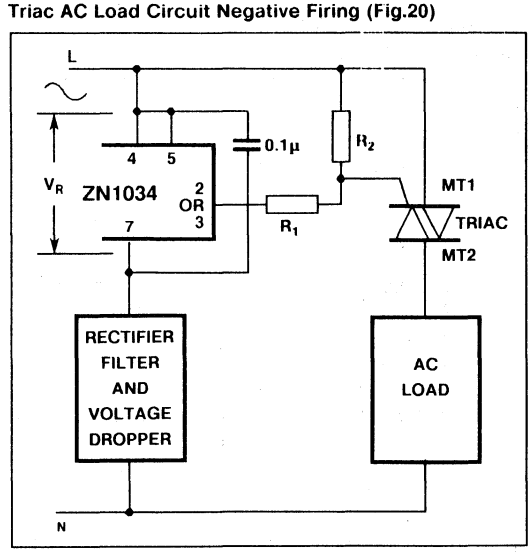
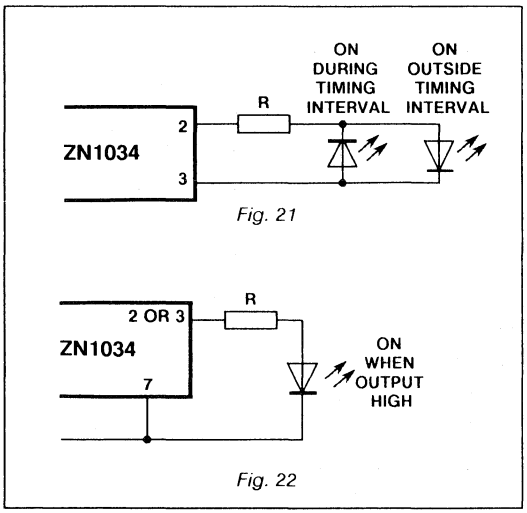


Fig.20

The value of R_2 is chosen to prevent any leakage currents biasing the triac gate ON during OFF periods. R_1 is chosen to limit the gate current to the maximum required by the triac for negative firing in both quadrants.

Triacs in general are easier to fire in the negative gate mode than the positive and in this configuration the ZN1034 output drive voltage is a maximum since the total output swing would be $V_{R\ Min} - V_{O(LO)\ Max}$ = 4.3V for a current of 25mA. Negative firing triac circuits therefore enable triacs of greater power to be driven directly from the ZN1034 outputs than would be the case for positive firing circuits.

Output State Indication (Figs.21 & 22)



The value of R is chosen to limit the current to the LED requirements. When mains supplies are used the extra power in the dropper resistor may make the use of neon indicators across the load preferable to LEDs.

POWER SUPPLIES AND REFERENCES

Externally Regulated Supplies (Fig.23)

If a 5V ± 6% supply rail is available then the internal shunt regulator is not necessary and by leaving pin 5 unconnected the minimum current drain of 2mA required is avoided. The current available from the supply should not fall below a level of:

I_{CC} = (5mA + the output current from pins 3 or 2)

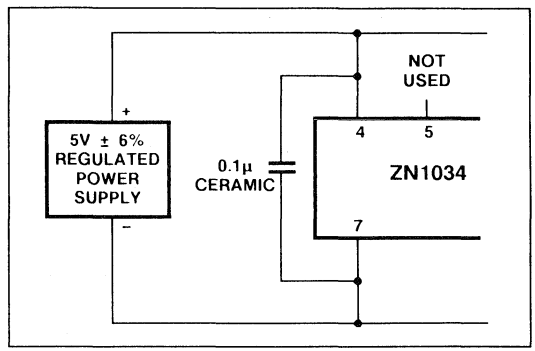


Fig. 23

N.B. The supply should be decoupled by 0.1μF capacitor connected as close as possible to pins 4 and 7.

Internally Regulated Supplies

DC Supplies Greater Than 5V (Fig.24)

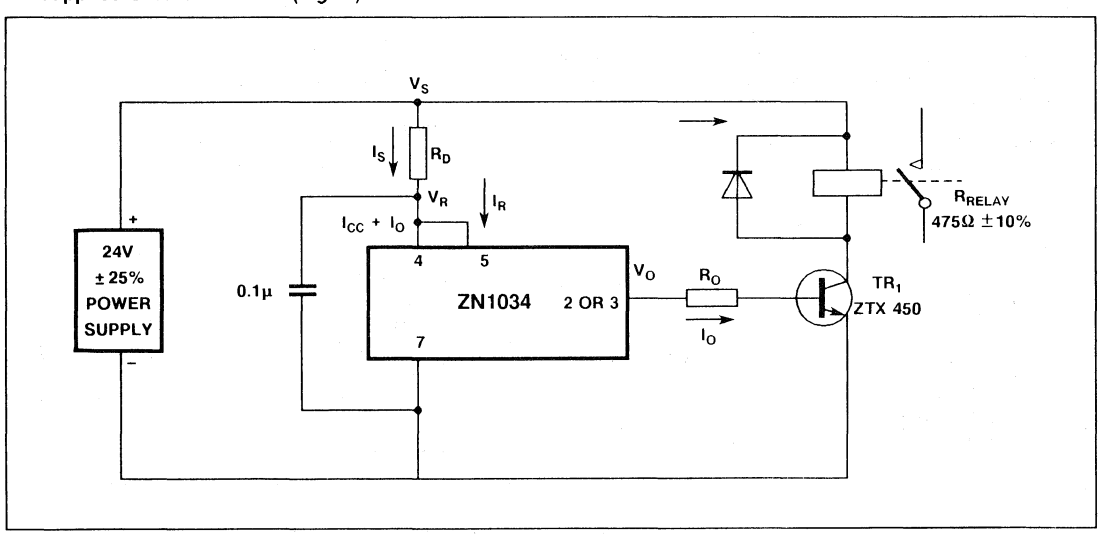


Fig.24

By connecting pin 5 to pin 4 an on-chip shunt regulator allows the use of unregulated DC supplies higher than 5V. To illustrate the use of the shunt regulator a supply circuit design for operation with a typical process equipment supply of +24V and ±25% is shown in Fig. 24..

N.B. The supply decoupling capacitor also acts as stabilisation for the internal regulator and the connection between pins 4 and 5 should therefore be as short as possible.

The values of R_O and R_D used in the circuit of Fig.24 are calculated as follows. For R_O we need $I_{O(Min)}$, the minimum current required into the base of TR_1 for worst case conditions.

$$I_{O(Min)} = I_{B(Max)}$$

$$= \frac{1}{h_{FE(Min)}} \times \frac{24\ (+25\%)}{475\ (-10\%)}$$

$$= \frac{1}{50} \times \frac{30}{427}$$

$$\mathbf{I_{O(Min)}} = \mathbf{1.4mA}$$

Deriving $V_{O(Min)}$ for the output circuit (Fig.16)

$$V_{O(Min)} = V_{R(Min)} - 2 \times (\text{Internal } V_{BE})$$

$$= 4.7 - 1.4$$

$$\mathbf{V_{O(Min)}} = \mathbf{3.3V}$$

Hence $$R_O = \frac{3.3 - V_{BE}}{1.4}\ k\Omega \quad (V_{BE} = 0.6V)$$

$$= 1.9k$$

Choose $\mathbf{R_O} = \mathbf{1.8k\Omega}$ (Nearest lower preferred value)

To calculate R_D we need $V_{O(Max)}$ and $I_{S(Min)}$

As above

$$V_{O(Max)} = V_{R(Max)} - 2 \times (\text{Internal } V_{BE})$$

$$= 5.3 - 1.4V$$

$$\mathbf{V_{O(Max)}} = \mathbf{3.9V}$$

and with the value of R_O chosen the actual current is

$$I_{O(Max)} = \frac{3.9 - V_{BE}}{1.8} = 1.8mA$$

From which the minimum allowable supply current can be obtained

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)}$$

$$= 5 + 1 + 1.8$$

$$\mathbf{I_{S(Min)}} = \mathbf{8.8mA}$$

Hence $$R_D = \frac{V_{S(Min)} - V_{R(Max)}}{I_{S(Min)}}$$

$$= \frac{18 - 5.3}{8.8}\ k\Omega$$

$$\mathbf{R_D} = \mathbf{1.5k\Omega}\ (\text{Nearest preferred value})$$

The power dissipated in the dropping resistor and the ZN1034 can be obtained also from

$$I_{S(Max)} = \frac{V_{S(Max)} - V_{R(Min)}}{1.5k\ (-5\%)}$$

$$= \frac{30 - 4.7}{1.425}\ mA$$

$$\mathbf{I_{SMax)}} = \mathbf{18mA}$$

Hence the ZN1034 dissipation = **90mW** max. and power dissipation by dropping resistor = **450mW** max.

The calculations assume ±2% tolerance resistors.

AC Mains Supplies (Fig.25)

A transformer may be used to drop the voltage from the mains and a rectified DC supply provided as discussed above.

However the on-chip shunt regulator makes the transformer unnecessary since the supply may be obtained directly from the mains or from any other source of AC or DC higher than 5V. With a load such as the directly driven triac (Figs.19 and 20) a half wave rectifier is used since either the line or neutral has a connection common to the load circuit and the IC supply thus preventing the use of a bridge rectifier.

The calculation of the smoothing and voltage dropping components is described below.

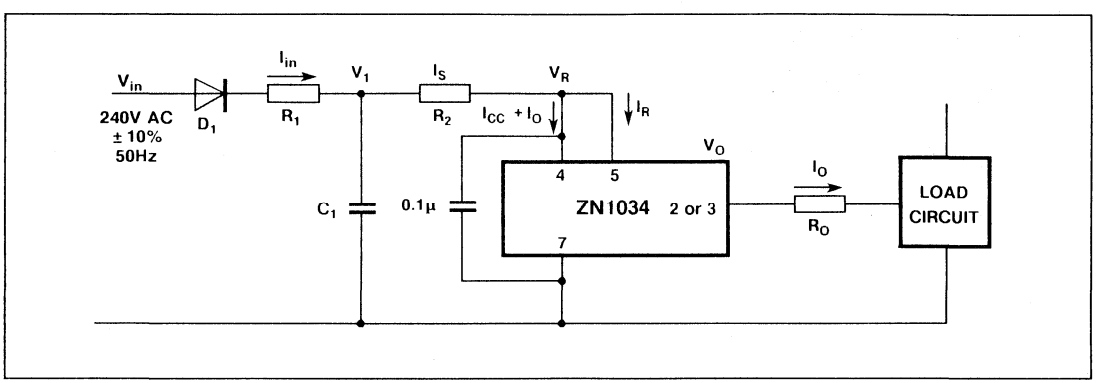


Fig. 25

The value of R_O and $I_{O(Max)}$ are calculated above and as an example a current $I_{O(Min)}$ of 10mA is assumed (the gate current for a 0.35A Triac, RS 202).

Therefore

$$V_{O(Min)} = 3.3V$$

$$R_O = \frac{3.3 - V_G}{10.10^{-3}} \ \Omega \ (V_G = 2V \text{ for RS 202})$$

$$\mathbf{R_O = 120\Omega} \quad \text{(Nearest lower preferred value)}$$

$$\mathbf{V_{O(Max)} = 3.9V}$$

Hence $$I_{O(Max)} = \frac{3.9 - V_G}{0.12} \ mA$$

$$\mathbf{I_{O(Max)} = 16mA}$$

And the minimum value of supply current for correct operation is therefore

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)}$$
$$= 5 + 2 + 16$$
$$\mathbf{I_{S(Min)} = 23mA}$$

If we assume that C1 is a 25V working capacitor and that 3V peak to peak ripple is allowable then the highest value for $V_{1(Min)}$ will be

$$V_{1(Min)} = 25\ (-20\%) - 3 \quad \text{(Allowing for } \pm 10\% \text{ variation in mains supply)}$$

$$\mathbf{V_{1(Min)} = 17V}$$

Therefore $$R_2 = \frac{17 - V_{R(Max)}}{23} \ k\Omega$$

$$\mathbf{R_2 = 510\Omega} \quad \text{(Nearest preferred value)}$$

The current I_{in} will flow for very nearly the full half cycle, 10ms in the case of 50Hz supplies, since V_1 is low compared to the peak mains voltage.

Now $$I_{in(avg)} = \frac{V_{in(pk)} - V_{1(avg)}}{\pi R_1}$$

and this current from the rectifier must be equal to the current into the timer circuit.

$$I_{in(avg)} = I_{S(avg)}$$

and the average value of this current is

$$I_{S(avg)} = \frac{V_{1(Min)} + V_{RIPPLE(avg)} + V_{R(Min)}}{R_2}$$
$$= \frac{17 + 1.5 + 4.7}{510}$$
$$= 27mA$$

Therefore $$R_1 = \frac{\sqrt{2} \times 240\ (-10\%) - (17 + 1.5)}{\pi \times 27} \ k\Omega$$

$$= \mathbf{3.3k\Omega} \text{ (Nearest preferred value)}$$

For the required ripple of 3V pk-pk we can obtain

$$C_1 = \frac{I_{S(avg)} \times 10ms}{3}$$

$$C_1 = \frac{27 \times 10^{-5}}{3}$$

$$\mathbf{C_1 = 100\mu F} \quad \text{(Nearest higher preferred value)}$$

In order to calculate the maximum power dissipation in the dropping resistor we need to know $I_{in(avg)}$ for the upper limit of mains voltage.

Maximum value of

$$I_{in(avg)} = \frac{V_{in(pk)(Max)} - V_{1(Max)}}{\pi R_1}$$

$$= \frac{2 \times 240\ (+10\%) - 20}{h \times 3.3 \times 10^3}$$

$$\mathbf{Max.\ I_{in(avg)} = 34mA}$$

and Max. dissipation in

$$R_1 = \frac{\pi^2}{4} \ I_{in}^2{}_{(avg)} \times R_1$$

$$\mathbf{P_{R1} = 9.4W}$$

When a DC load such as the thyristor relay driver of Fig.18 is required then a full wave bridge circuit can be used as shown in Fig.26.

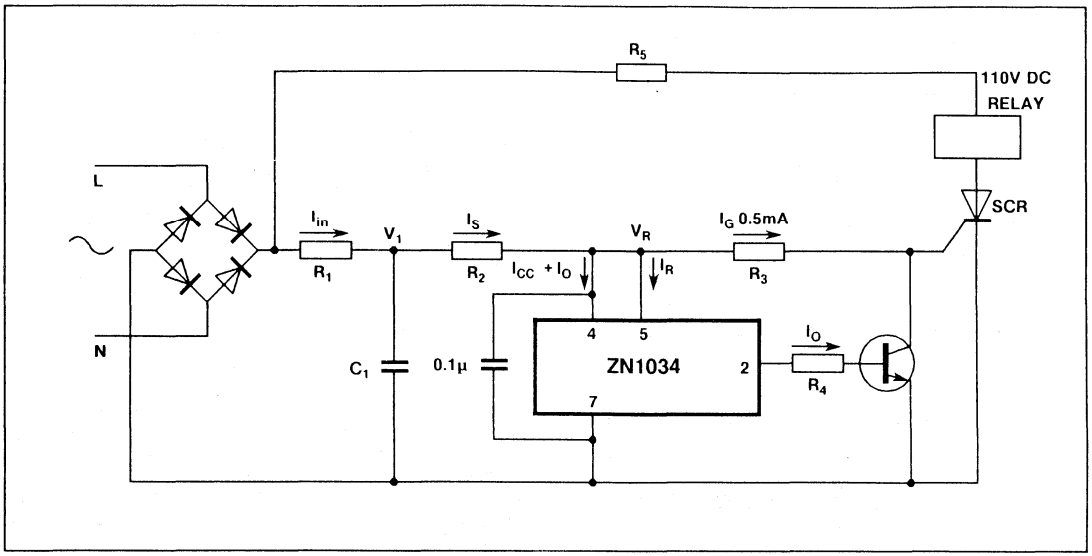


Fig. 26

The DELAY-TO-OFF timer circuit of Fig.18 has been taken as an example. A typical circuit might have the relay resistance equal to R_5 = 10k and for a 240V ± 10% mains supply the SCR could be a BRX49 which requires less than 0.5mA on gate current. To ensure gate turn-off a ZTX450 transistor with a base current of 0.5mA is sufficient with the above load.

Hence $I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)} + I_G$

$= 5 + 2 + 0.5 + 0.5$

$I_{SMin)} = \mathbf{8mA}$

Choosing C_1 to be 25V working and 3V peak to peak ripple as in the previous example. Then

$V_{1(Min)} = 25\ (-20\%) - 3$

$= \mathbf{17V}$

And $R_2 = \dfrac{17 - V_{R(Max)}}{8}\ k\Omega$

$= \mathbf{1.5k\Omega}$ (Nearest preferred value)

To find the required value of C_1 estimate the angle of conduction. Thus for a sine wave input conduction will change when the voltage on the smoothing capacitor is equal to the instantaneous value of the input voltage less the rectifier voltage drop.

So $V_1 + 1.2 = V_{in(pk)} \sin \theta$

and for small values:

$\theta = \sin \theta$

Hence $\theta = \dfrac{V_1 + 1.2}{V_{in(pk)}}$

(assuming 1.2V drop across the bridge rectifier)

for the rising sine wave

$$\theta_r = \frac{V_{1(Min)} + 1.2}{V_{in(pk)}}$$

and for the falling sine wave

$$\theta_f = \frac{V_{1(Max)} + 1.2}{V_{in(pk)}}$$

$$\theta_{tot} = \frac{V_{1(Min)} + V_{1(Max)} + 2.4}{V_{in(pk)}}$$

$$= \frac{\mathbf{17 + 20 + 2.4}}{305}$$ (Taking lowest mains input as worst case).

$= 0.13$ radian

The angle of non-conduction $\theta_{tot} \simeq 8°$ and the capacitance will discharge by 3V in this period which in terms of time is

$$t = \frac{8}{180°} \times 10\text{ms (for 50Hz mains)}$$

$= 0.44$ms

and since $C \simeq \dfrac{\Delta t}{\Delta V} \cdot I_{S(Max)}$,

where $I_{S(Max)} \simeq I_{S(Min)} + 20\%$

$$\simeq \frac{44 \times 10^{-5}}{3} \times 8 \times 10^{-3}\ (+20\%)$$

$\simeq 1.4\mu F$

So we can choose a 2.2µF of 25V working or higher for C_1.

The mains dropping resistor can be simply obtained with sufficient accuracy by assuming 100% conduction. Thus

$$R_1 = \frac{2}{\pi} \times \frac{V_{in(pk)} - V_{1(Max)}}{I_{S(Min)}}$$

$$= \frac{2 \times (305 - 20)}{\pi \times 8 \times 10^{-3}}$$

(Lowest mains voltage gives worst case).

$$\simeq \mathbf{22k\Omega}$$ (Next lowest preferred value

In order to calculate the power dissipated by the dropping resistor P_{R1} we need to know $I_{in(avg)}$ for the higher limit of the supply.

Maximum value of

$$I_{in(avg)} \simeq \left[\frac{2\,(V_{in(pk)(Max)} - V_{1(Max)})}{\pi R_1}\right]$$

$$= \frac{2}{\pi} \quad \frac{2 \times 240\,(+10\%) - 20}{22 \times 10^{-3}}$$

$$\mathbf{I_{in(avg)} = 10mA}$$

Hence

$$P_{R1} = \frac{\pi^2}{8} \times 10^{-4} \times 22 \times 10^3$$

$$\mathbf{P_{R1} = 2.7W}$$

The calculations have been performed using the 235V ± 10% 50Hz mains figures. Similar calculations may be made for 110V 60Hz or whatever supplies are available.

Reference supply

The 2.6V reference on pin 14 may be used for an external reference other than for the timing components.

INTERFERENCE SUPPRESSION

Two types of interference, mains borne and electromagnetically radiated interference, can affect the operation of the timing circuit. In environments where such noise is encountered steps should be taken to reduce its effect on the timing circuit and the following notes should enable the circuit designer to avoid interference problems. The points discussed are illustrated by referring to a mains delay-to-on, plug-in module timer design, illustrated in Figs.27, 28, 29 and 30.

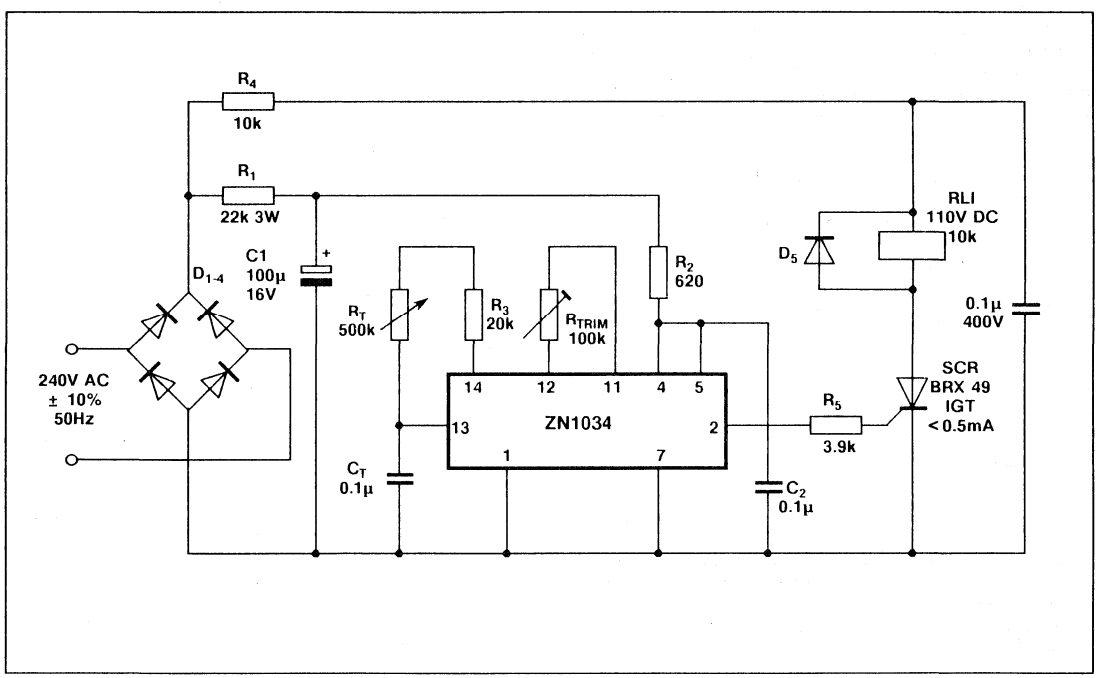


Fig. 27

Mains Borne Interference

If the supply is reduced below (typically) 3.6V at any time, even for less than a microsecond, the the ZN1034 counter section will be reset and restoration of the normal supply will initiate a new timing period or terminate the period depending on the initiation mode used. The effects of pulses on the supply are described above under 'Timing Initiation and Reset'.

Positive spikes are effective only when they produce a negative overshoot large enough to cause reset.

Negative spikes can be reduced by using a full diode bridge circuit, as in Fig.27 which rectifies the spikes as well as the AC supply, or a half bridge where an AC load is being driven and the timer ground cannot be separated from neutral. The dropping resistor R_1, with C_1, forms a low pass filter for mains smoothing and additional filtration is provided by R_2 and C_2. These filters will also attenuate noise spikes. The shunt regulator in conjunction with the dropping resistors R_1 and R_2 provides considerable spike attenuation as well as DC regulation. The circuit of Fig.27 for example, has an attenuation of supply spikes of 15000:1 due to the regulator alone. When a 5V supply designed for TTL, or similar requirements is available and the shunt regulator is not connected, protection against interference is not usually necessary since the supply itself should be capable of suppressing mains borne interference.

If a transformer is used to isolate the timer from the mains then the voltage drop can be divided between the transformer and the series resistor. The greater the series resistance then the greater the attenuation of noise by the shunt regulator and the smoothing capacitor. A transformer drop to 24V DC is a useful compromise allowing the use of 24V relays. The transformer itself will attenuate high frequency spikes.

Electromagnetically Induced Noise

The ZN1034 oscillator frequency is determined by the time taken to charge C_T via R_T from about 1.6 to 2.2V on pin 13. A single interference pulse of 0.1V on this pin could cause an error on a single time constant of 20% but since the timing period of a ZN1034 timer is made up of 4095 RC charging times then a large number of interference pulses in a timing period would be required to cause such a timing error. Where such inteference exists, and bearing in mind that for a constant rate of interference pulses the effect becomes greater for increasing length of time period, steps should be taken to screen pin 13 from electromagnetically induced noise. Since the oscillator is required to operate at

$$\frac{4095}{20 \times 10^{-3}} \text{ Hz},$$

i.e. 200kHz, pin 13 is sensitive to radiated high frequency interference. Mains Borne pulses can be equally troublesome if steps are not taken to isolate pin 13 from such interference. The method used in the design example of Fig.27 is effective against both EMI and Mains Borne noise. A ground plane is produced by leaving a large area of copper on the component side of a double sided PCB with clearance holes for the component connections. The ground pin (7) is connected to the ground plane and the ground side of components such as C_T and the decoupling capacitors are also connected directly to the ground plane. In this way the connections have a low impedance to pin 7 and the possibility of coupling interference pulses from the load or decoupling components into the oscillator circuit via common earth leads is reduced considerably. At the same time the printed circuit connections are screened from EMI.

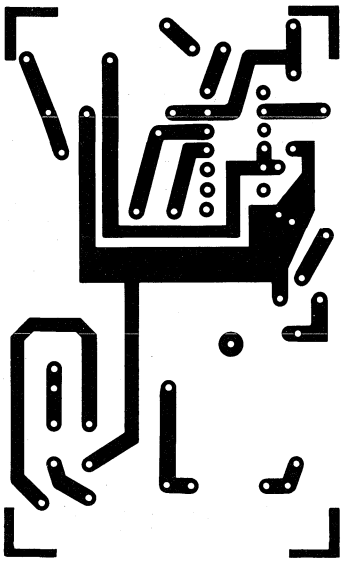


Fig.28 PCB for Fig.27 - track side

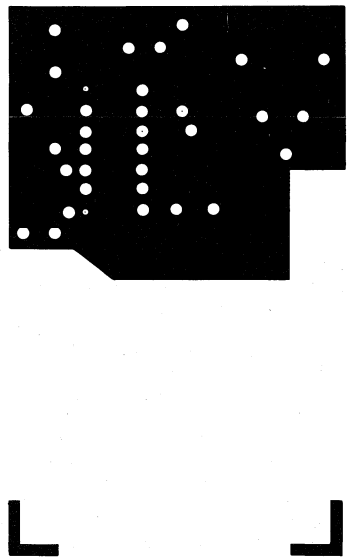


Fig.29 PCB for Fig.27 - ground plane

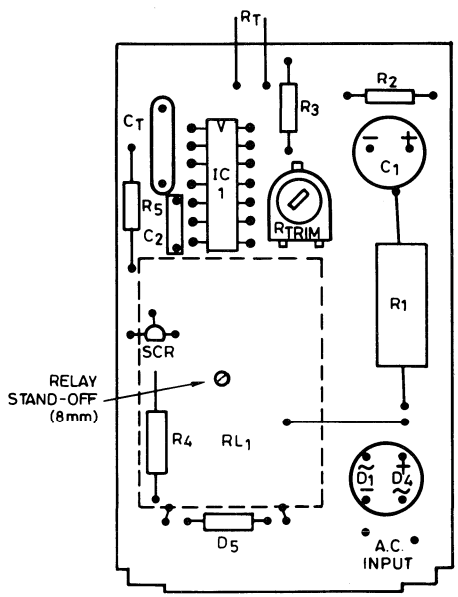


Fig.30 PCB component layout for Fig.27

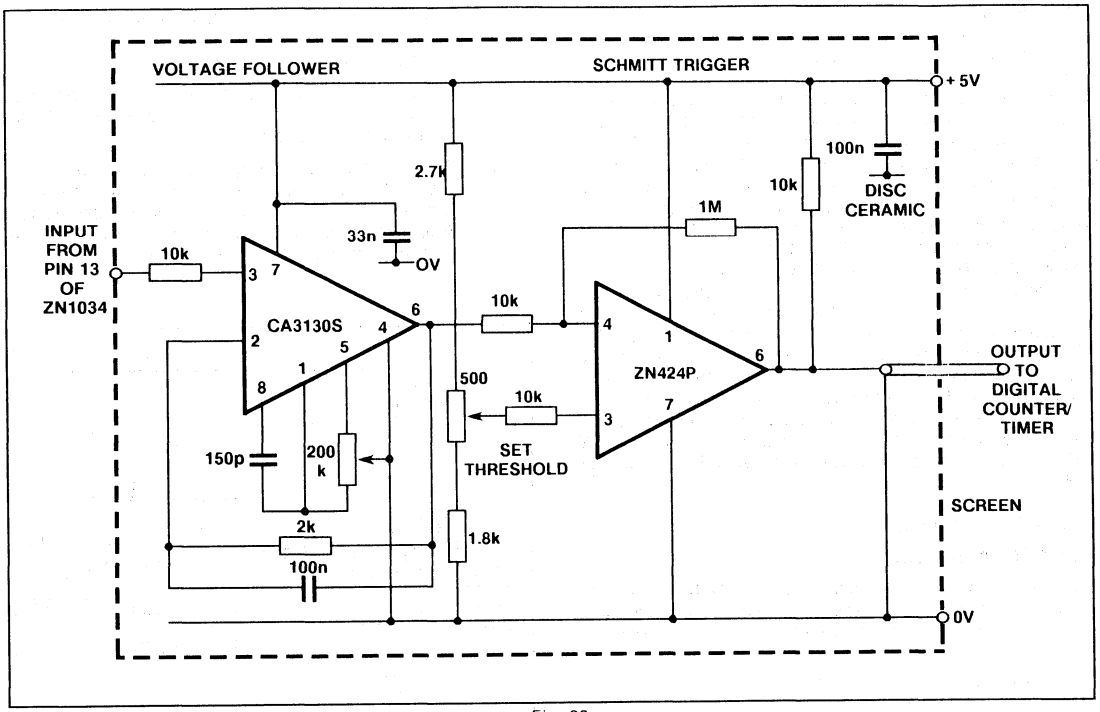

VOLTAGE FOLLOWER
SCHMITT TRIGGER
+5V
2.7k
100n
10k
DISC
CERAMIC
1M
INPUT
FROM
PIN 13
OF
ZN1034
10k
33n
0V
CA3130S
10k
OUTPUT
TO
DIGITAL
COUNTER/
TIMER
ZN424P
500
10k
SET
THRESHOLD
150p
200
k
SCREEN
2k
1.8k
100n
0V

Fig. 32

An external screen such as a metal case can be effective against radiated interference but it does not have the advantage of a ground plane with regard to the reduction of common earth lead interference.

Any leads connected to pin 13 are susceptible to interference pick-up and should be screened. A remote variable timing resistor can be connected to the PCB either by twin screened lead with the screen to ground or single screened with the screen connected to pin 14. It will be noticed that the fixed part of the timing resistance is connected very close to pin 13 to help decouple the connecting leads to the variable resistor.

When the ZN1034 oscillator frequency is near to that of the mains supply, or to low harmonics, care should be taken in the layout of the circuitry and in the position of components such as mains transformers to obviate this effect. Stray coupling of mains frequencies can have the effect of locking the oscillator to that frequency and producing a band over which variation in timing components will not cause a corresponding variation in timing period. The periods most susceptible to such interference are 82 and 41 seconds for 50Hz mains or 68 and 34 seconds for 60Hz mains.

TIMER CALIBRATION

Direct Measurement

Timer circuits may be calibrated directly by measuring the time period between changes of state on the output pins 2 or 3. This method should be used where accuracies of better than 0.2% are required.

Oscillator Period Measurement

The measurement of oscillator period is a much quicker method of calibration but it involves measurements at a high impedance point in the circuit where the loading due to the measuring instrument could effect the result. The following notes should assist in calibration by oscillator period measurement.

(a) A passive high impedance probe may be used to connect an oscillator or a digital frequency meter to pin 13 and if the probe resistance is greater than 100 R_T and the capacitance less than $C_t/100$ then an accuracy better than 2% should be obtainable. For lower accuracy these requirements may be relaxed proportionally. The period of the oscillator sawtooth waveform is measured and multiplied by 4095 to obtain the time period.

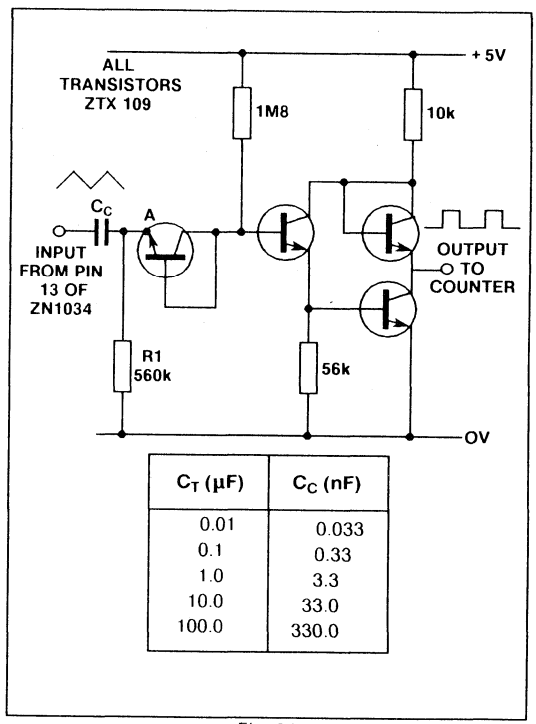
(b) A capacitively coupled probe illustrated in Fig. 31 enables calibration accuracies of better than 0.2% to be obtained.

The maximum value of coupling capacitance for this accuracy is tabulated against timing capacitance above.

(c) It may be advantageous to build-in the probe input capacitor and resistor to the timer and have point 'A' as the input to the external buffer.

An active voltage follower probe such as that illustrated in Fig. 32 may be used instead of the passive probe in (a) above.

(d) Connecting extra circuitry to pin 13 increases the possibility of incorrect operation due to interference and the precautions suggested under 'Interference Suppression' above should be borne in mind when devising oscillator period calibration systems.



C_T (µF)	C_C (nF)
0.01	0.033
0.1	0.33
1.0	3.3
10.0	33.0
100.0	330.0

Fig. 31

ZN1036E/D

PROGRAMMABLE COUNTER TIMER INTEGRATED CIRCUIT

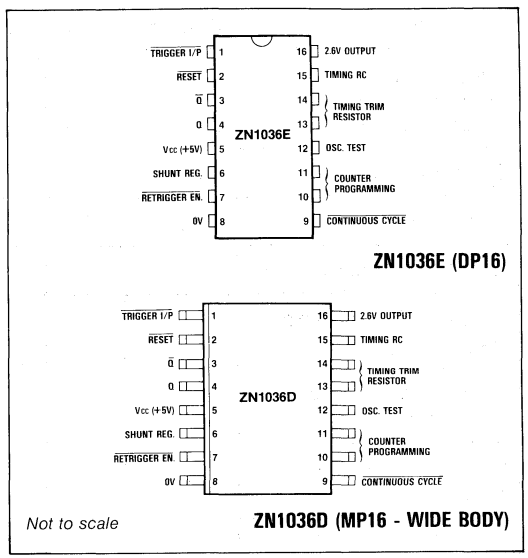
The ZN1036 combines linear and digital functions on the same chip such that simple precision timers can be constructed using the minimum of low cost external components. The frequency of an on-chip oscillator is determined by an external capacitor and resistor. Fine adjustment can then be achieved by the variation of an external trimming resistor. A buffered oscillator output can be used to monitor the trimming operation without affecting the oscillator frequency.

Pulses from the oscillator are fed into a programmable counter and the output changes state after a preset number of pulses. The counter is programmable in 4 stages - 4095, 2047, 1023 and 511 counts.

In this way precise time periods can be defined by timing capacitors and resistors of much smaller value than would be required by single RC time constant timers.

The count can be initiated either (a) with trigger input LO and supply going HI (supply initiation), or (b) with supply HI and trigger input going LO (trigger initiation). The timer can also be retriggered at any point (thus initiating a new timing period) or reset, terminating the time period.

The IC can operate from normal +5V logic supplies or from any higher voltage using a dropping resistor and internal shunt regulator connected to the supply pin.



Pin connections (top view)

FEATURES

- External Control of Operational Mode
- Accurate and Repeatable Performance
- Complementary High Current Output Drivers
- Buffered Oscillator Output for Easy Oscillator Calibration
- Time Period Trimming
- Supply or Trigger Input Timing Initiation
- Continuous Cycle Facility
- On-Chip Regulator or TTL Supply Option
- Minimum of External Components Required
- Available in Plastic DIL (DP) — ZN1036E and Miniature Plastic DIL (MP) — ZN1036D

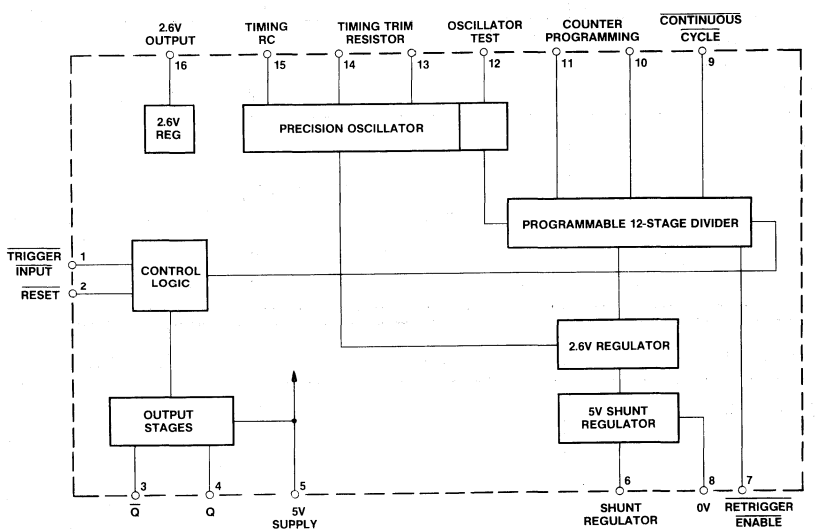


Fig.1

ABSOLUTE MAXIMUM RATINGS

Dissipation	250mW derate above 30°C at 5mW/°C
Output source current	25mA
Output sink current	25mA
Operating temperature range	0 to +70°C
Storage temperature range	−55 to +125°C

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Timing section						See Note 5
Timing resistor	R_T	2k7		5M6	Ω	
Timing capacitor	C_T	0.1			nF	See Fig 2
Trim resistor	R_{trim}	0		560	kΩ	
Repetitive timing error			0.01		%	
Timing initiation and reset						
(a) Supply voltage initiation						
Voltage to initiate timing	V_{CC}	4.7			V	supply applied to pin 5 with Pin 1 connected to Pin 8
Rate of change of V_{CC}				0.25	V/μs	
(b) Trigger input initiation						
Voltage to initiate timing	$V_{T(LO)}$			1	V	
Voltage to prevent initiation of timing	$V_{T(HI)}$	2.2			V	
Minimum pulse to trigger			2		μs	
(c) Supply voltage reset						
Voltage to reset	V_{CC}		3.6		V	See note 2
External clock input						
Frequency				250	kHz	Clock input to pin 14 via a 10k resistor
Drive current	I_{clk}		0.1		mA	
Pulse width	t_{clk}	2			μs	
Pulse amplitude	V_{clk}	2.5		5.5	V	

Parameter	Symbol	Conditions	
Time multiplying factor	M	Pin 10	Pin 11
4095		H	H
2047		H	L
1023		L	H
511		L	L

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply						Note 4
(a) Externally regulated						connected to Pin 5
Supply voltage Supply current	V_{CC} I_{CC}	4.5	 3.8	5.5 4.5	V mA	V_{CC} = 5V outputs unloaded
(b) Internally regulated (5V shunt regulator)						connect pin 5 to Pin 6. Note 4
Operating current range	I_R	5		55	mA	see Note 3
Regulated voltage	V_R	4.5		5.5	V	I_R = 10mA
Slope resistance			1.25		Ω	I_R = 7 – 55mA
Regulated voltage change with temperature			35		mV	I_R = 7 – 55mA t = 0 to +70°C
(c) Reference voltage (2.5V series regulator)						
Regulated voltage	V_{REF}	2.4	2.5	2.6	V	V_{CC} = 5V, Pin 16 unloaded
Load current	I_{REF}		1		mA	V_{CC} = 5V
Slope resistance			2.5		Ω	
Output drive Q to $\overline{Q}$						V_{CC} = 5V
Output voltage	$V_{O(HI)}$ $V_{O(LO)}$	2.5 0.3	3.0 0.4	3.2 0.6	V V	$I_{O(HI)}$ = 25mA $I_{O(LO)}$ = – 25mA
Output current	$I_{O(HI)}$ $I_{O(LO)}$			– 25 + 25	mA mA	Source Sink
Rise time	t_r		300		ns	I_O = 5mA, V_{CC} = 5V
Fall time	t_f		100		ns	I_O = 5mA, V_{CC} = 5V
Propagation delay V_T Low to V_O High	t_p		2.3	2.5	μs	
Oscillator test output swing		3	4	5	V	10k Pull up to 5V
Temperature coefficient	T_C		0.008		%/°C	R_{TRIM} = 56k

Note 1 Time = MCR

C = capacitance in μF
R = resistance in MΩ
M = multiplying factor

For $t_{osc} \geqslant 10\mu s$

At $t_{osc} < 10\mu s$ this relationship no longer holds as the reset time becomes a significant fraction of t_{osc}

Ncte 2 In order to reset the timer the supply voltage should be reduced to 2V although reset may be typically acheived at 3.6V. Reset will not occur with the supply greater than 4V

Note 3 Since the +5V regulator cannot be used on its own without the rest of the circuit, the minimum operating current includes the 4.5mA maximum supply current taken by the timer.

Note 4 A 0.1μF capacitor should be connected between V_{CC} (Pin 5) and G_{ND} (Pin8) at all times.

Note 5 Minimum recommended oscillator period = 4μs

SECTION 1 THE TIMING FUNCTION

1.1 Fixed time period

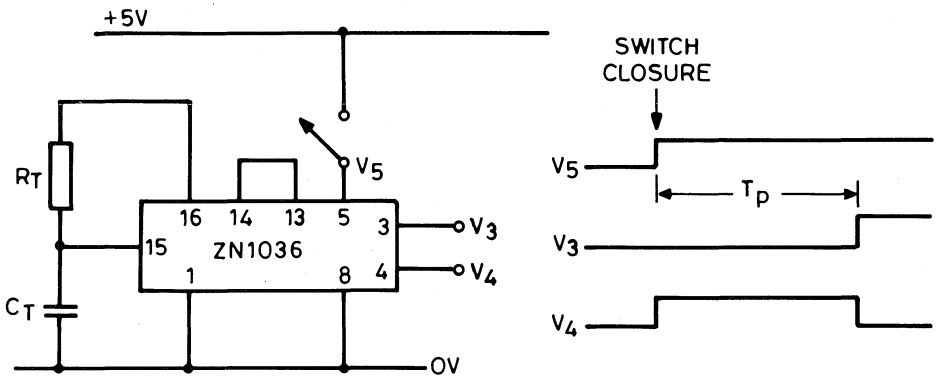


Fig. 2

External components R_T and C_T determine the length of period T_p. The timing components set the period of an internal oscillator to C_T R_T ± 10% and an internal divider causes a change in the output state after a preset number of oscillator cycles (determined by counter programming Pins).

When the time period is initiated Pin 4 goes Hi for a time period T_p. On completion of the time period, Pin 4 goes Lo and Pin 3 which was previously Lo goes Hi and remains Hi until the timing sequence is re-initiated.

1.2 Trimming the time period

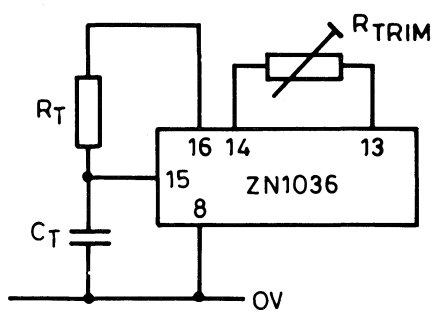


Fig. 3

1.3 Design of variable period timers

Time periods from 2.044ms to infinity may theoretically be obtained using the ZN1036 integrated timer circuit. The following section should enable the designer to get the best possible circuit configuration achievable within the design limits. The necessary information is presented below, Fig 4, in the form of a timing components against oscillator period graph. The graph has been plotted using a 56kΩ trim resistor between Pins 13 and 14.

The maximum range of oscillator period possible for a particular value - or timing capacitor can easily be obtained from the graph. To obtain the time period the oscillator period (from Fig. 4) is multiplied by the multiplying factor M (determined by programming Pins 10 and 11)

The periods obtained with the timing components selected from Fig. 4 may be trimmed to the exact time required using a variable resistor up to the value of 560kΩ between Pins 13 and 14.

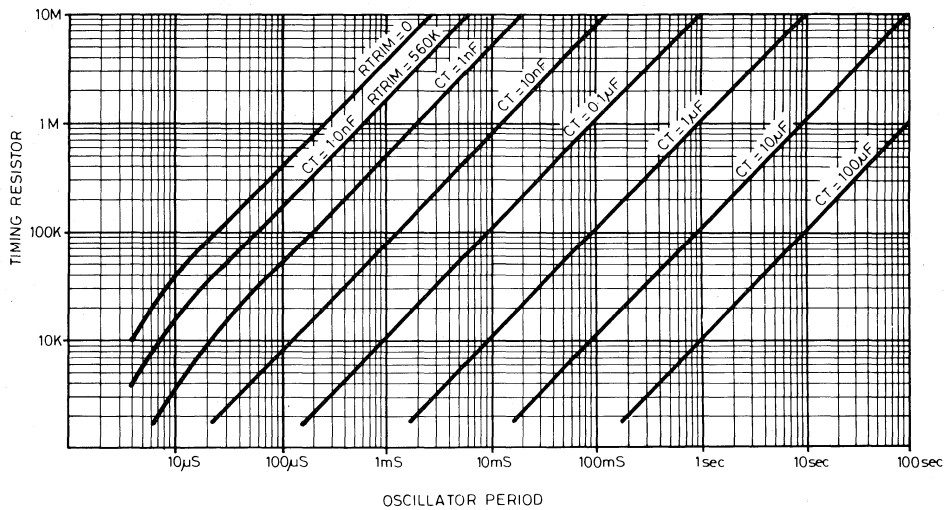


Fig. 4 Oscillator period

SECTION 2 INPUT AND OUTPUT CIRCUITS

Note 2.1 External clock

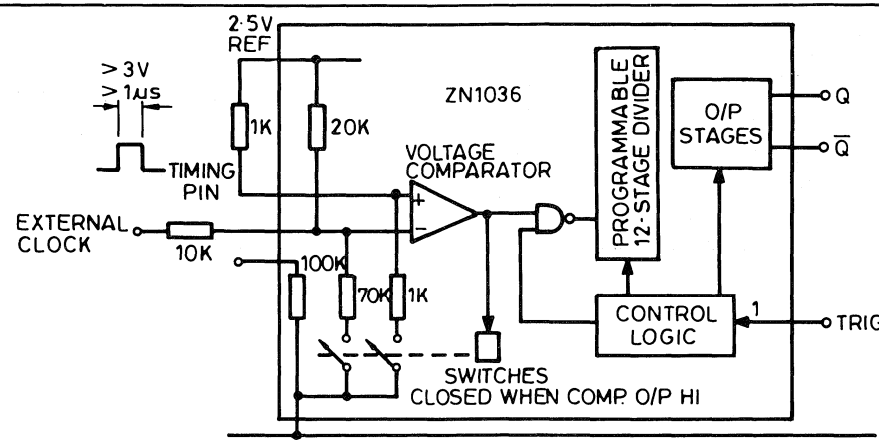


Fig. 5

The ZN1036 can be used with an external clock as shown in the circuit of Fig. 5.

The internal clock is disabled by connecting a 1k resistor from the timing pin 15 to the +2.5V reference pin 16 thus preventing the non-inverting i/p to the amplifier dropping below the inverting input voltage. The amplifier output is therefore HI and the internal switches are closed.

An external clock pulse, provided it meets the limits defined in the characteristics, will override the disabling on pin 15 and, if the trigger i/p on pin 1 is LO, will cause a pulse to be passed to the divider circuit.

The output Q and $\overline{Q}$ will change from LO to HI and vice versa at the end of a present number of external clock pulses.

Note 2.2 Timing initiation and reset

2.2.1 Supply initiated

When pin 1 is held 'LO' and the supply is switched on, the control logic and counters are automatically reset as the supply rises to its on voltage. This also initiates timing at the same instant by gating the oscillator output into the counter. After the set time the outputs change state and remain thus until the supply is switched off or another period is initiated.

If, during such a timing cycle the trigger input is taken HI, no matter how many times or for how long, the condition of the outputs and the length of the timing period will not be affected. If the supply drops below the reset level even for a few microseconds then the timing period will be terminated. It will be reset and restarted when the supply rises again above the reset level. Thus a supply drop-out has the effect of increasing the time period. The timer can also be reset at any time by taking Pin2 Lo.

2.2.2 Trigger initiated

Allowing pin 1 to rise with the supply prevents timer initiation by the supply.

Pulling the trigger input 'LO' now initiates a normal timing period. A further period may be initiated by dropping the trigger LO again. This period is not affected when the trigger input level is altered during timing - as long as the 'retrigger enable' (Pin 7) remains Hi. When the retrigger enable goes Lo during timing any further trigger pulse will cause the initiation of a further time period at that point. The period is terminated again by the supply falling below the reset level or a Lo pulse to reset Pin 2. Since the normal condition of the trigger is Hi the timing will not restart on restoration of supply. A supply drop-out during a trigger initiated timing period has the effect of shortening the set time.

2.2.3 A simple repetitive timer

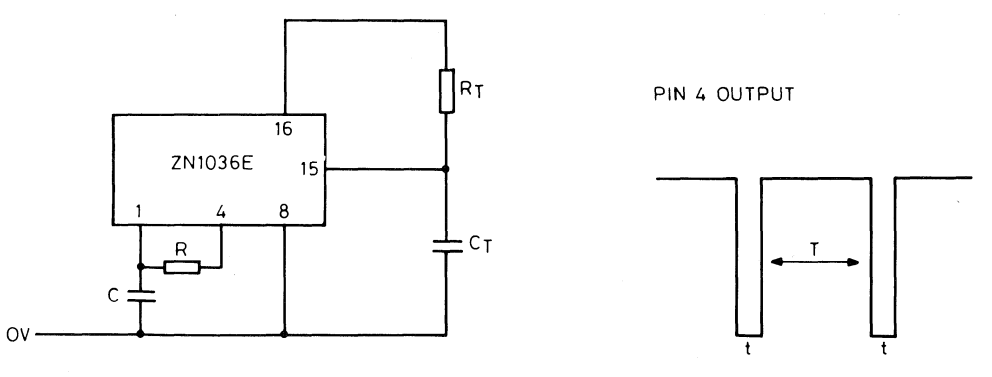


Fig. 6

A capacitor and resistor in the feedback loop can be used and the pulse length t determined by the values of C and R. T is determined by timing components R_T and C_T. R may be any value up to 10k whilst C is limited to 10μF.

2.2.4 A simple closed loop timer

The ZN1036 enables the designer to construct multistage timers with ease as one can be triggered by a single wire link from the output of another.

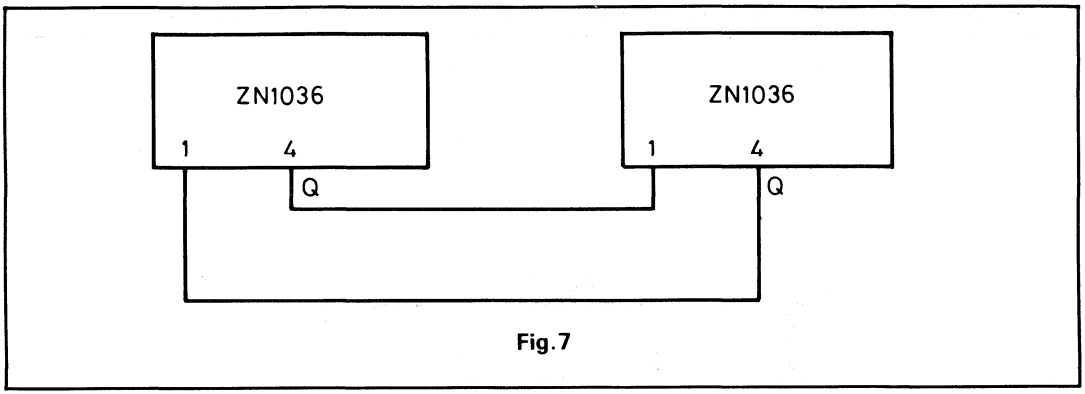


Fig.7

This may in theory be extended to any number of counters but for more than 3 there will be other modes of oscillation. For a ring of three, component tolerances will usually ensure that one mode is dominant with only one Q output Hi at a time. Higher numbers may not operate in the desired mode unless one set time is greater than the sum of all the others.

Fig. 8 shows a four stage ring timer.

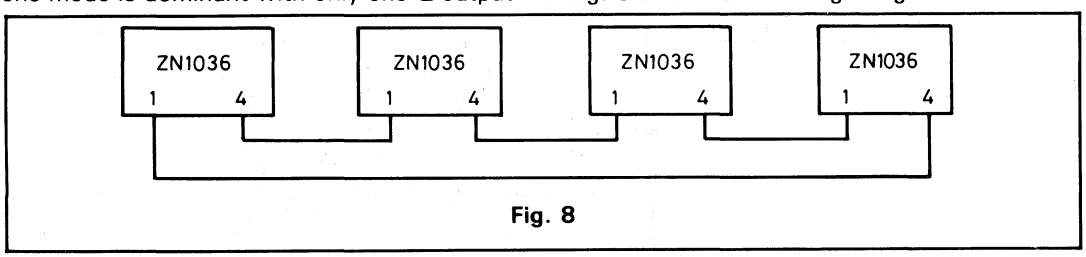


Fig. 8

2.2.5 ZN1036 Waveforms

The function of this device is demonstrated below as a Waveform diagram (Fig. 9)

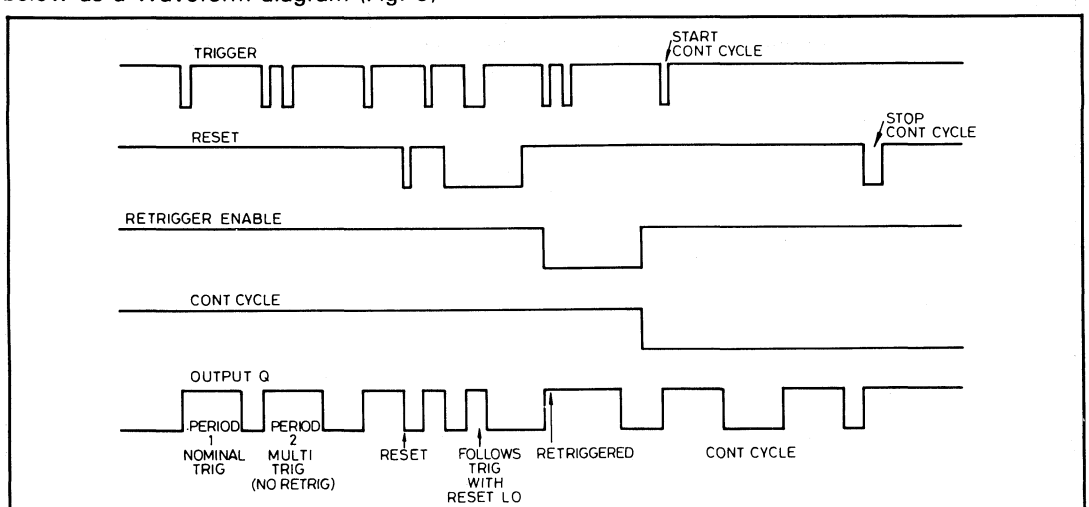


Fig. 9

2.3 Trigger input circuit

The input circuit comprises of a buffer input followed by a schmitt trigger circuit. The buffer pull up resistor can be as low as 30kΩ. So to pull the input down below the IV threshold a pull down resistor of less than 5.6kΩ is recommended for worst case design.

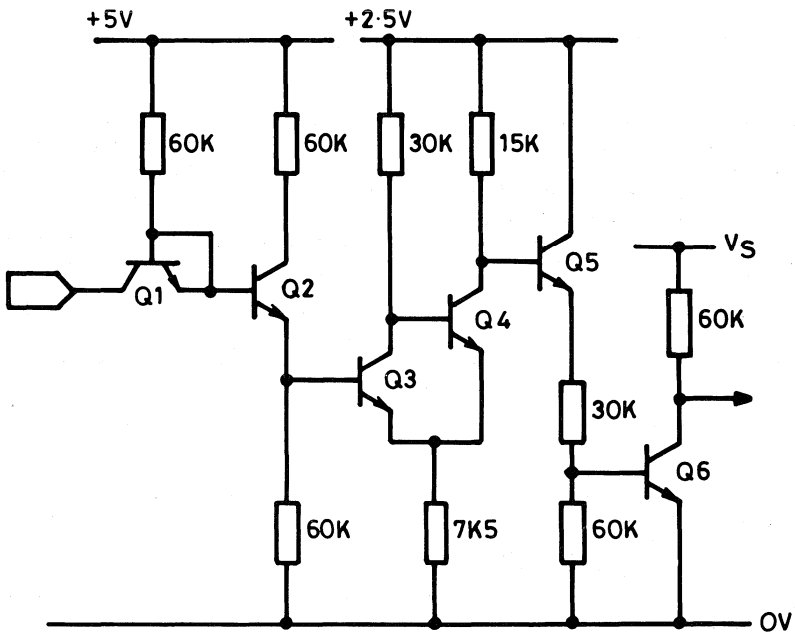


Fig. 10

2.4 Output drive circuits

The Q and $\overline{Q}$ output drive circuits have the form illustrated in Fig. 11

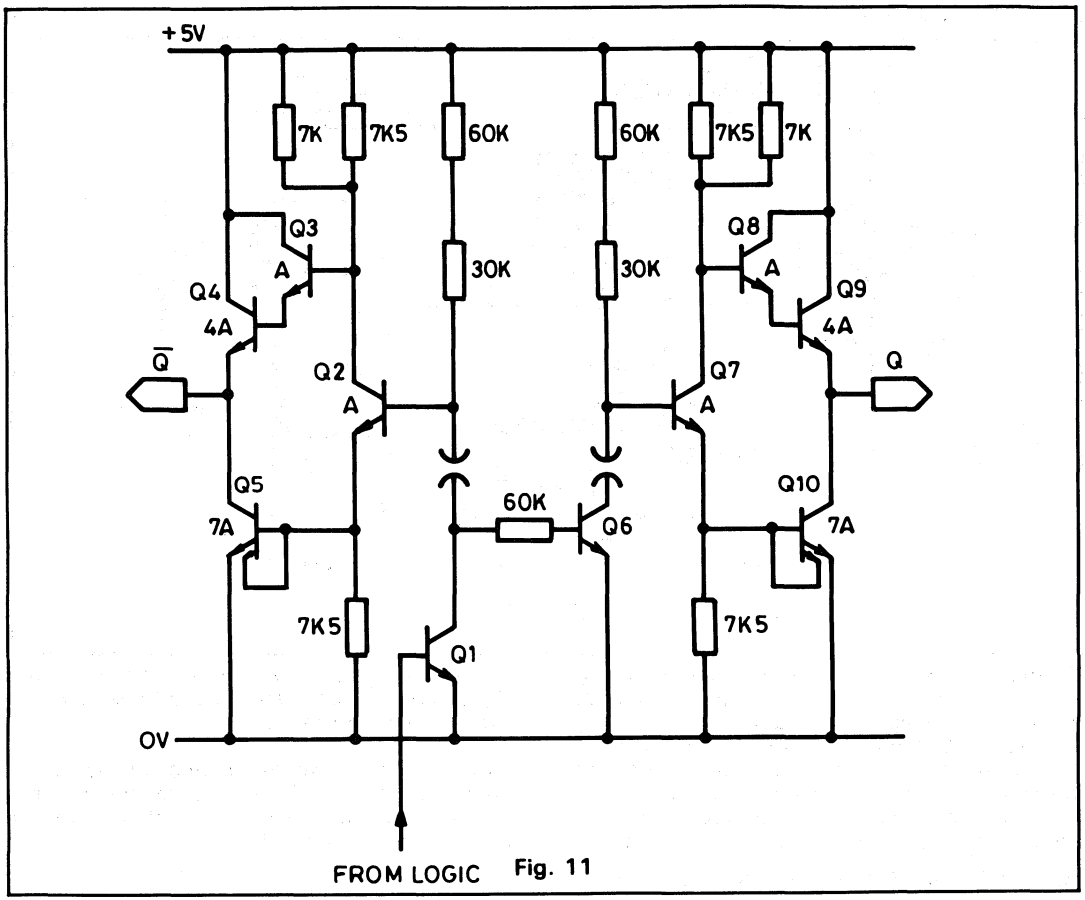


Fig. 11

2.5 Load circuits

2.5.1 Transistor driven relay

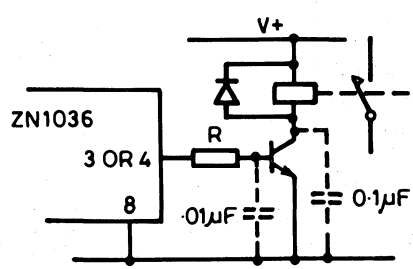


Fig. 12

The value of R is chosen to limit current to minimum required by the transistor under the worst condition.

If interference is experinenced suppression capacitors as shown may be needed.

2.5.2 Thyristor driven relay

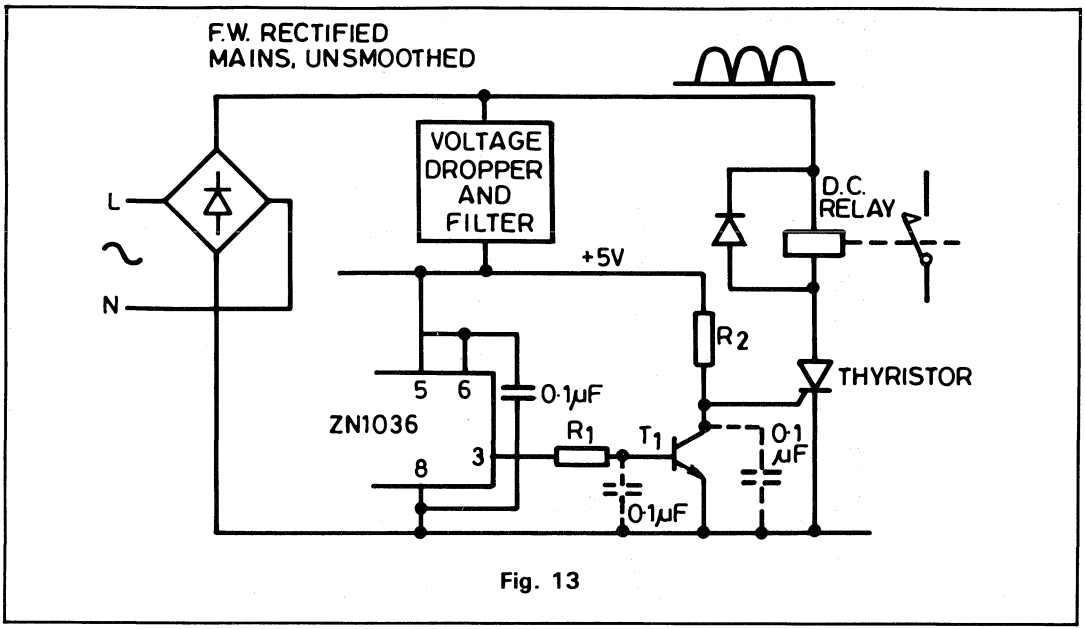


Fig. 13

A thyristor gate may be driven via a limiting resistor directly from pin 3 for DELAY-TO-ON timers. Fig. 13 illustrates a circuit for achieving DELAY-TO-OFF using a thyristor. R_2 can be as high as 10k for low gate current thyristors. The thyristor is chosen such that the reduction in gate-cathode impedance achieved with a saturated transistor is sufficient to increase the holding current to a value which ensures turn OFF and R_1 is chosen so that the transistor (T_1) just reaches saturation.

For 240 volts a.c. mains it may be necessary to use a 110 volt d.c. relay with a dropping resistor of equal resistance since 220 volts d.c. relays are not easily obtainable.

2.5.3 Triac a.c. load circuit positive firing

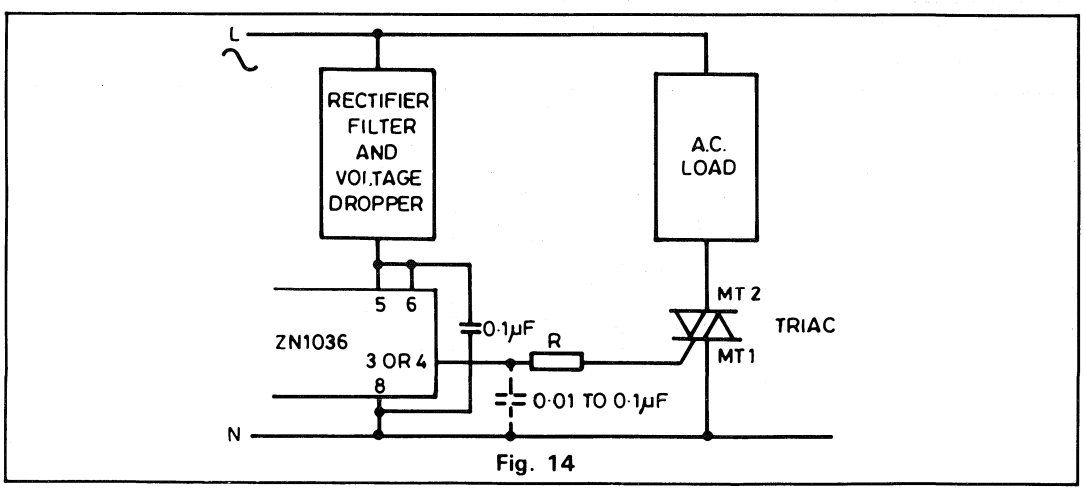


Fig. 14

The value of R is chosen to limit the current to the minimum required by the triac for positive firing in both quadrants.

2.5.4 Triac a.c. load circuit negative firing

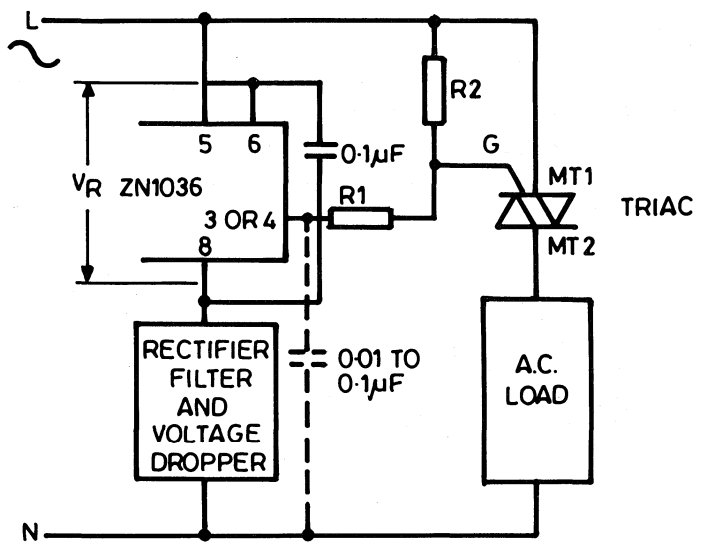


Fig. 15

The value of R_2 is chosen to prevent any leakage currents biasing the triac gate ON during OFF periods. R_1 is chosen to limit the gate current to the maximum required by the triac for negative firing in both quadrants.

Triacs in general are easier to fire in the negative gate mode than the positive and in this configuration the 1036 output drive voltage is a maximum since the total output swing would be $V_{R\,Min} - V_{O(LO)\,Max} \simeq 4.3$ volts for a current of 25mA. Negative firing triac circuits therefore enable triacs of greater power to be driven directly from the ZN1036 outputs than would be the case for positive firing circuits.

2.5.5 Output state indication

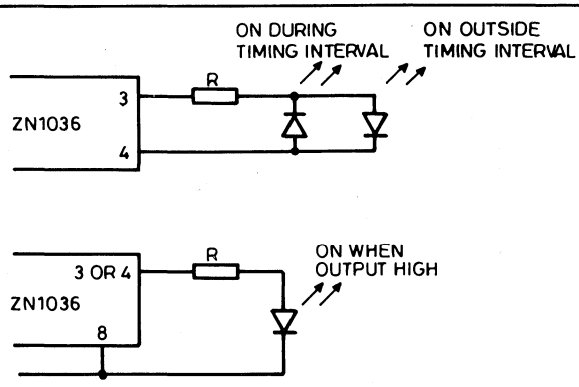


Fig. 16

The value of R is chosen to limit the current to the LED requirements. When mains supplies are used the extra power in the dropper resistor may make the use of neon indicators across the load preferable to LEDs.

SECTION 3 POWER SUPPLIES AND REFERENCES

3.1 Externally regulated supplies

If a 5V ±10% supply rail is available then the internal shunt regulator is not necessary and by leaving pin 6 unconnected the minimum current drain of 2mA required is avoided. The current available from the supply should not fall below a level of:

$$I_{CC} = (5mA + \text{the output current from pins 3 or 4})$$

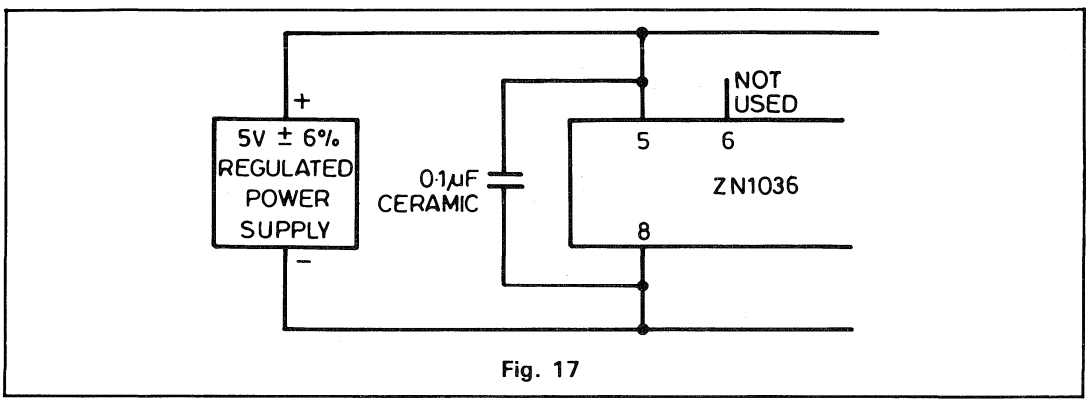


Fig. 17

N.B. The supply should be decoupled by 0.1μF capacitor connected as close as possible to pins 5 and 8.

3.2 Internally regulated supplies

3.2.1 d.c. supplies greater than 5 volts

By connecting pin 6 to pin 5 an on-chip shunt regulator allows the use of unregulated d.c. supplies higher than 5 volts. To illustrate the use of the shunt regulator a supply circuit design for operation with a typical process equipment supply of +24V and ±25% is shown below.

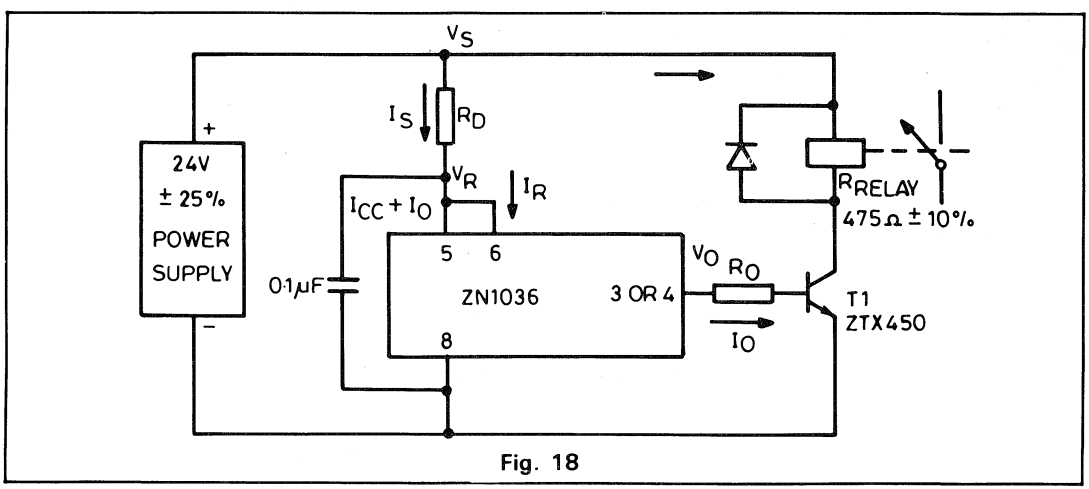


Fig. 18

N.B. The supply decoupling capacitor also acts as stabilisation for the internal regulator and the connection between pins 6 and 5 should therefore be as short as possible.

The values of R_O and R_D used in the circuit of Fig. 18 are calculated as follows. For R_O we need $I_{O(Min)}$, the minimum current required into the base of T_1 for worst case conditions.

$$I_{O(Min)} = I_{B(Max)}$$

$$= \frac{1}{h_{FE(Min)}} \times \frac{24(+25\%)}{475(-10\%)}$$

$$= \frac{1}{50} \cdot \frac{30}{427}$$

$$\mathbf{I_{O(Min)}} = \mathbf{1.4mA}$$

Deriving $V_{O(Min)}$ for the output circuit (Fig. 11)

$$V_{O(Min)} = V_{R(Min)} - 2 \times (\text{Internal } V_{BE})$$

$$= 4.7 - 1.4$$

$$\mathbf{V_{O(Min)}} = \mathbf{3.3\ volts}$$

Hence

$$R_O = \frac{3.3 - V_{BE\,T_1}}{1.4}\ k\Omega \quad (V_{BE\,T_1} = 0.6V)$$

$$= 1.9k$$

Choose $\mathbf{R_O}$ = **1.8k** (Nearest lower preferred value)

To calculate R_D we need $V_{O(Max)}$ and $I_{S(Min)}$

As above

$$V_{O(Max)} = V_{R(Max)} - 2 \times (\text{Internal } V_{BE})$$

$$= 5.3 - 1.4V$$

$$\mathbf{V_{O(Max)}} = \mathbf{3.9\ volts}$$

and with the value of R_O chosen the actual current is

$$I_{O(Max)} = \frac{3.9 - V_{BE\,T_1}}{1.8} = 1.8mA$$

From which the minimum allowable supply current can be obtained

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)}$$

$$= 5 + 1 + 1.8$$

$$\mathbf{I_{S(Min)}} = \mathbf{8.8mA}$$

Hence

$$R_D = \frac{V_{S(Min)} - V_{R(Max)}}{I_{S(Min)}}$$

$$= \frac{18 - 5.3}{8.8}\ k$$

$$\mathbf{R_D} = \mathbf{1.5k}\ \text{(Nearest preferred value)}$$

The power dissipated in the dropping resistor and the ZN1036 can be obtained also from

$$I_{S(Max)} = \frac{V_{S(Max)} - V_{R(Min)}}{1.5k(-5\%)}$$

$$= \frac{30 - 4.7}{1.425} \text{ mA}$$

$$\mathbf{I_{S(Max)} = 18mA}$$

Hence the ZN1036 dissipation = 90mW max. and power dissipation by dropping resistor = 450mW max.

The calculations assume ±2% tolerance resistors.

3.2.2 a.c. mains supplies

A transformer may be used to drop the voltage from the mains and a rectified d.c. supply provided as discussed in 3.2.1

However the on-chip shunt regulator makes the transformer unnecessary since the supply may be obtained directly from the mains or from any other source of a.c. or d.c. higher than 5 volts. With a load such as the directly driven triac (sections 2.5.3 and 2.5.4) a half wave rectifier is used since either the line or neutral has a connection common to the load circuit and the I.C. supply thus preventing the use of a bridge rectifier.

The calculation of the smoothing and voltage dropping components is described below.

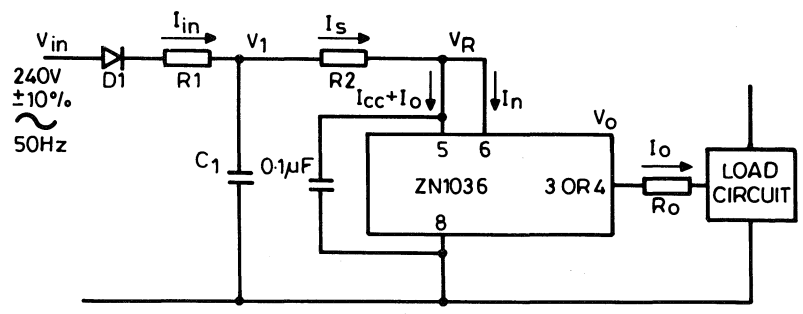


Fig. 19

The value of R_O and $I_{O(Max)}$ are calculated as in 3.2.1 and as an example a current $I_{O(Min)}$ of 10mA is assumed (the gate current for a 0.35A Triac, RS 202).

Therefore

$$\mathbf{V_{O(Min)} = 3.3V}$$

$$R_O = \frac{3.3 - V_G}{10.10^{-3}} \Omega \quad (V_G T_1 = 2V \text{ for RS 202})$$

$$\mathbf{R_O = 120\Omega} \text{ (Nearest lower preferred value)}$$

$$\mathbf{V_{O(Max)} = 3.9V}$$

Hence

$$I_{O(Max)} = \frac{3.9 - V_G}{0.12} \text{ mA}$$

$$\mathbf{I_{O(Max)} = 16mA}$$

And the minimum value of supply current for correct operation is therefore

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)}$$
$$= 5 + 2 + 16$$
$$\mathbf{I_{S(Min)} = 23mA}$$

If we assume that C1 is a 25 volt working capacitor and that 3 volts peak to peak ripple is allowable then the highest value for $V_{1(Min)}$ will be

$$V_{1(Min)} = 25(-20\%) - 3 \text{ (Allowing for } \pm 10\% \text{ variation in mains supply)}$$
$$\mathbf{V_{1(Min)} = 17V}$$

Therefore
$$R_2 = \frac{17 - V_{R(Max)}}{23} \text{ k}\Omega$$
$$\mathbf{R_2 = 510\Omega} \text{ (Nearest preferred value)}$$

The current i_{in} will flow for very nearly the full half cycle, 10ms in the case of 50Hz supplies, since V_1 is low compared to the peak mains voltage.

Now
$$i_{in(avg)} = \frac{V_{in(pk)} - V_{1(avg)}}{\pi R_1}$$

and this current from the rectifier must be equal to the current into the timer circuit.

$$i_{in(avg)} = I_{S(avg)}$$

and the average value of this current is

$$I_{S(avg)} = \frac{V_{1(Min)} + V_{RIPPLE(avg)} - V_{R(Min)}}{R_2}$$
$$= \frac{17 + 1.5 - 4.7}{510}$$
$$= 27\text{mA}$$

Therefore
$$R_1 = \frac{\sqrt{2} \times 240\,(-10\%) - (17 + 1.5)}{\pi \times 27} \text{ k}\Omega$$
$$= \mathbf{3k3} \text{ (Nearest preferred value)}$$

For the required ripple of 3V pk.pk. we can obtain

$$C_1 = \frac{I_{S(avg)} \times 10\text{ms}}{3}$$
$$C_1 = \frac{27 \times 10^{-5}}{3}$$
$$\mathbf{C_1} = \mathbf{100\mu F} \text{ (Nearest higher preferred value)}$$

In order to calculate the maximum power dissipation in the dropping resistor we need to know $i_{in(avg)}$ for the upper limit of mains voltage.

Maximum value of $$i_{in(avg)} = \frac{V_{in(pk)(Max)} - V_{1(Max)}}{\pi R_1}$$

$$= \frac{2 \times 240\ (+10\%) - 20}{h \times 3.3 \times 10^3}$$

$$\textbf{Max. } i_{in(avg)} = \textbf{34mA}$$

and Max dissipation in $$R_1 = \frac{\pi^2}{4} \times i_{in}{}^2{}_{(avg)} \times R_1$$

$$P_{R1} = \textbf{9.4 watts}$$

When a d.c. load such as the thyristor relay driver of section 2.4.2 is required then a full wave bridge circuit can be used as shown below.

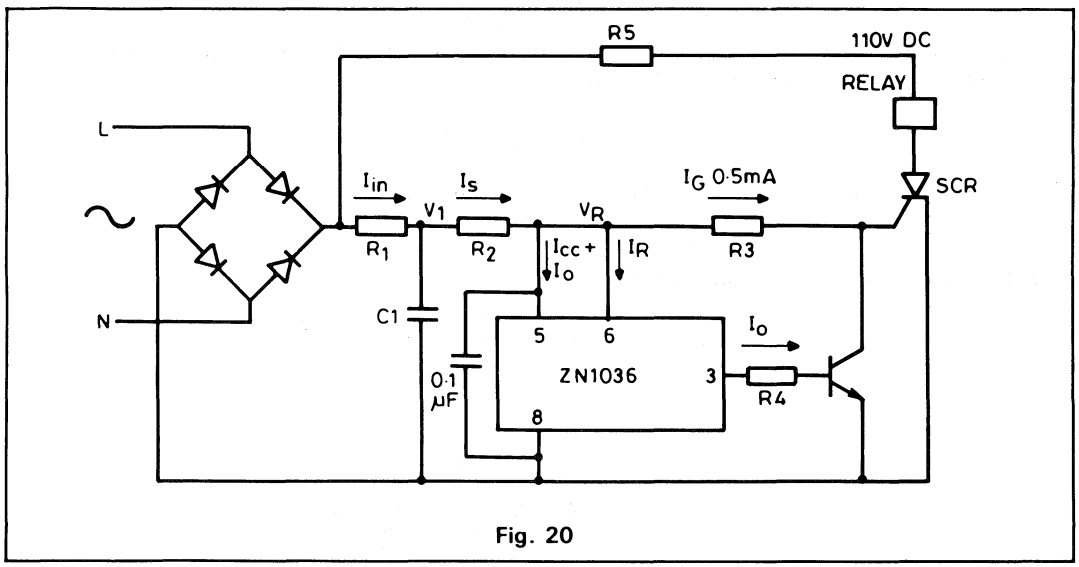


Fig. 20

The DELAY-TO-OFF timer circuit of Fig. 13 has been taken as an example. A typical circuit might have the relay resistance equal to $R_5 = 10k$ and for a 240V $\pm$ 10% mains supply the SCR could be a BRX49 which requires less than 0.5mA on gate current. To ensure gate turn-off a ZTX450 transistor with a base current of 0.5mA is sufficient with the above load.

Hence $$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)} + I_G$$

$$= 5 + 2 + 0.5 + 0.5$$

$$I_{S(Min)} = \textbf{8mA}$$

Choosing C_1 to be 25 volts working and 3 volts peak to peak ripple as in the previous example. Then

$$V_{1(Min)} = 25\ (-20\%) - 3$$

$$= \textbf{17 volts}$$

And $$R_2 = \frac{17 - V_{R(Max)}}{8}\ K\Omega$$

$$= \textbf{1.5k}\ \text{(Nearest preferred value)}$$

To find the value of C_1 required estimate the angle of conduction. Thus for a sine wave input conduction with change when the voltage on the smoothing capacitor is equal to the instantaneous value of the input voltage less the rectifier voltage drop.

So $V_1 + 1.2 = V_{in(pk)} \text{ Sin } \theta$

and for small values $\theta = \text{Sin } \theta$

Hence $\theta = \dfrac{V_1 + 1.2}{V_{in(pk)}}$

(assuming 1.2 volt drop across the briage rectifier).

for the rising sine wave $\theta_r = \dfrac{V_{1(Min)} + 1.2}{V_{in(pk)}}$

and for the falling sine wave $\theta_f = \dfrac{V_{1(Max)} + 1.2}{V_{in(pk)}}$

$$\theta_{tot} = \frac{V_{1(Min)} + V_{1(Max)} + 2.4}{V_{in(pk)}}$$

$$= \frac{\mathbf{17 + 20 + 2.4}}{305} \text{ (Taking lowest mains input as worst case).}$$

$$= 0.13 \text{ radian}$$

The angle of non conduction $\theta_{tot} \simeq 8°$ and the capacitance will discharge by 3 volts in this period which in terms of time is

$$t = \frac{8}{180°} \times 10\text{ms (for 50Hz mains)}$$

$$= 0.44\text{ms}$$

and since $C \simeq \dfrac{\Delta t}{\Delta V} \cdot I_{S(Max)}$ $\qquad (I_{S(Max)} \simeq I_{S(Min)} + 20\%)$

$$\simeq \frac{44 \times 10^{-5}}{3} \times 8 \times 10^{-3} \ (+20\%)$$

$$\simeq 1.4\mu F$$

So we can choose a $2.2\mu F$ of 25 volt working or higher for C_1.

The mains dropping resistor can be simply obtained with sufficient accuracy by assuming 100% conduction. Thus

$$R_1 = \frac{2}{\pi} \times \frac{V_{in(pk)} - V_{1(Max)}}{I_{S(Min)}}$$

$$= \frac{2 \times 305\ 1\ 20}{\pi \times 8 \times 10^{-3}}$$

(Lowest mains voltage gives worst case).

$$\simeq 22\text{k (Next lowest preferred value)}$$

In order to calculate the power dissipated by the dropping resistor P_{R1} we need to know $i_{in(avg)}$ for the higher limit of the supply.

Maximum value of

$$i_{in(avg)} \simeq \frac{2\,(V_{in\,(pk)\,(Max)} - V_{1(Max)})}{\pi\, R_1}$$

$$= \frac{2}{\pi}\left(\frac{2 \times 240\,(+10\%) - 20}{22 \times 10^{-3}}\right)$$

$$i_{in(avg)} = \mathbf{10mA}$$

Hence

$$P_{R1} = \frac{\pi^2}{8} \times 10^{-4} \times 22 \times 10^3$$

$$P_{R1} = \mathbf{2.7\ watts}$$

The calculations have been performed using the 235V ± 10% 50Hz mains figures. Similar calculations may be done for 110V 60Hz or whatever supplies are available.

Note 3.3 Reference supply

The 2.6V reference on pin 16 may be used for an external reference other than for the timing components.

SECTION 4 INTERFERENCE SUPPRESSION

Two types of interference, mains borne and electromagnetically radiated interference, can affect the operation of the timing circuit. In environments where such noise is encountered steps should be taken to reduce its effect on the timing circuit and the following notes should enable the circuit designer to avoid interference problems. The points discussed are illustrated by referring to a mains delay-to-on, and timer design illustrated in Figs. 21 and 22.

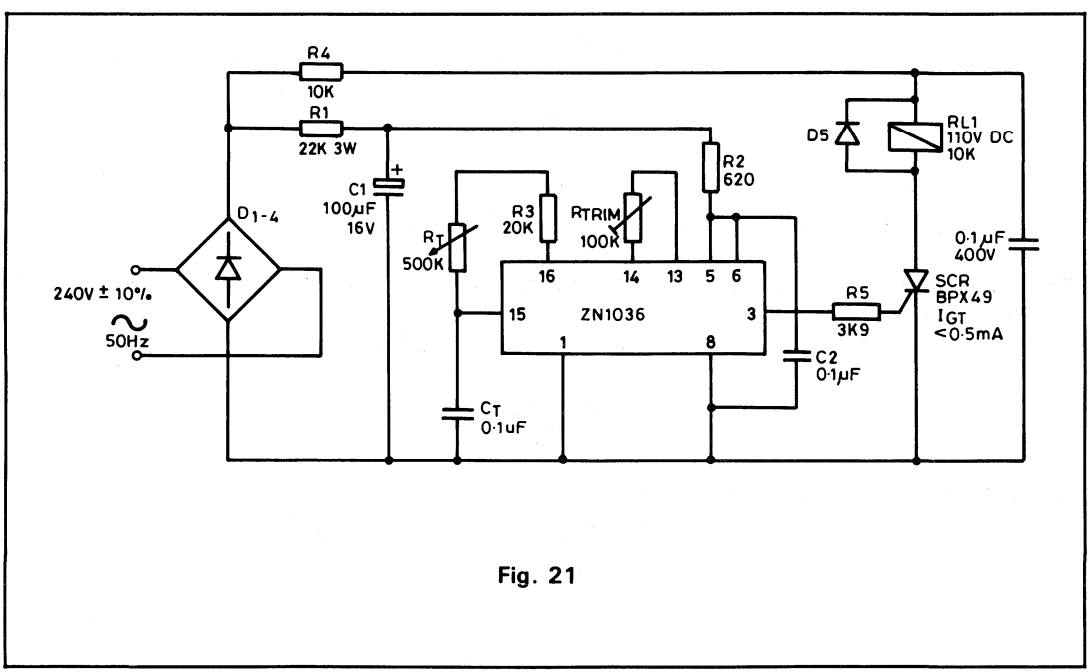


Fig. 21

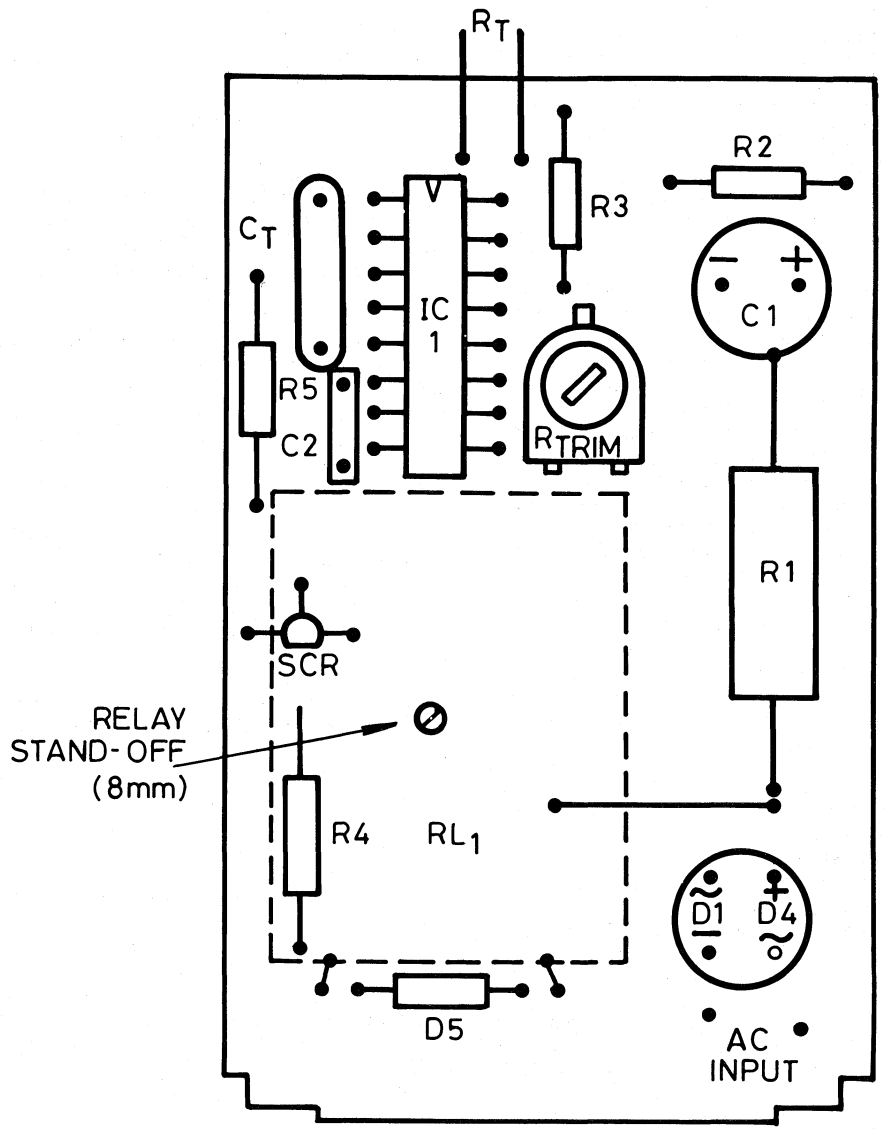

RT
R2
R3
CT
IC
1
C1
R5
C2
RTRIM
R1
SCR
RELAY
STAND-OFF
(8mm)
R4
RL1
D1
D4
D5
AC
INPUT

Fig. 22

Note 4.1 Mains borne interference

If the supply is reduced below (typically) 3.5V at any time, even for less than a microsecond then the logic and counter section of the ZN1036 will be reset and restoration of the normal supply may result in the initiation of a new timing period regardless of the initiation state. The effects of pulses on the supply are described in operating note 2.1.

Positive spikes are effective only when they produce a negative overshoot large enough to cause reset.

Negative spikes can be reduced by using a full diode bridge circuit, as in Fig. 21 which rectifies the spikes as well as the a.c. supply, or a half bridge where an a.c. load is being driven and the timer ground cannot be separated from neutral. The dropping resistor R_1, with C_1, forms a low pass filter for mains smoothing and additional filtration is provided by R_2 and C_2. These filters will also attenuate noise spikes. The shunt regulator in conjunction with the dropping resistors R_1 and R_2 provides considerable spike attenuation as well as d.c. regulation. The circuit of Fig. 21 for example, has an attenuation of supply spikes of 15000:1 due to the regulator alone. When a 5 volt supply designed for TTL, or similar requirements is available and the shunt regulator is not connected, protection against interference is not usually necessary since the supply itself should be capable of suppressing mains borne interference.

If a transformer is used to isolate the timer from the mains then the voltage drop can be devided between the transformer and the series resistor. The greater the series resistance then the greater the attenuation of noise by the shunt regulator and the smoothing capacitor. A transformer drop to 24V d.c. is a useful compromise allowing the use of 24V relays. The transformer itself will attenuate high frequency spikes.

Note 4.2 Electromagnetically induced noise

The ZN1036 oscillator frequency is determined by the time taken to change C_T via R_T from about 1.6 to 2.2 volts on pin 15. A single interference pulse of 0.1V on this pin could cause an error on a single time constant of 20% but since the timing period of a ZN1036 timer is made up of 511, 1023, 2047, or 4095 RC charging times then a large number of interference pulses in a timing period would be required to cause such a timing error. Where such interference exists, and bearing in mind that for a constant rate of interference pulses the effect becomes greater for increasing length of time period, steps should be taken to screen pin 15 from eletro-magnetically induced noise. Since the oscillator is required to operate for example in one of its modes at

$$\frac{4095}{20 \times 10^{-3}}\ \text{Hz},$$

i.e. 200kHz, pin 15 is sensitive to radiated high frequency interference. Mains borne pulses can be equally troublesome if steps are not taken to isolate pin 15 from such interference. The method used in the design example of Fig. 22 is effective against both EMI and Mains Borne noise. A ground plane is produced by leaving a large area of copper on the component side of a double sided PCB with clearance holes for the component connections. The ground pin (8) is connected to the earth plane and the earthy side of components such as C_T and the decoupling capacitors are also connected directly to the ground plane. In this way the connections have a low impedance to pin 8 and the possibility of coupling interference pulses from the load or decoupling components into the oscillator circuit via common earth leads is reduced considerably. At the same time the printed circuit connections are screened from EMI.

An external screen such as a metal case can be effective against radiated interference but it does not have the advantage of an earth plane with regard to the reduction of common earth lead interference.

Any leads connected to pin 15 are susceptable to interference pick-up and should be screened. A remote variable timing resistor can be connected to the PCB either by twin screened lead with the screen to ground or single screened with the screen connected to pin 16. It will be noticed that the fixed part of the timing resistance is connected very close to pin 15 to help decouple the connecting leads to the variable resistor.

When the ZN1036 oscillator frequency is near to that of the mains supply, or to low harmonics, care should be taken in the layout of the circuitry and in the position of components such as mains transformers to obviate this effect. Stray coupling of mains frequencies can have the effect of locking the oscillator to that frequency and producing a band over which variation in timing components will not cause a corresponding variation in timing period.

SECTION 5 TIMER CALIBRATION

5.1 Direct measurement

Timer circuits may be calibrated directly by measuring the time period between changes of state on the output pins 3 or 4. Accuracies of better than 0.2% can be achieved using this method.

5.2 Oscillator period measurement

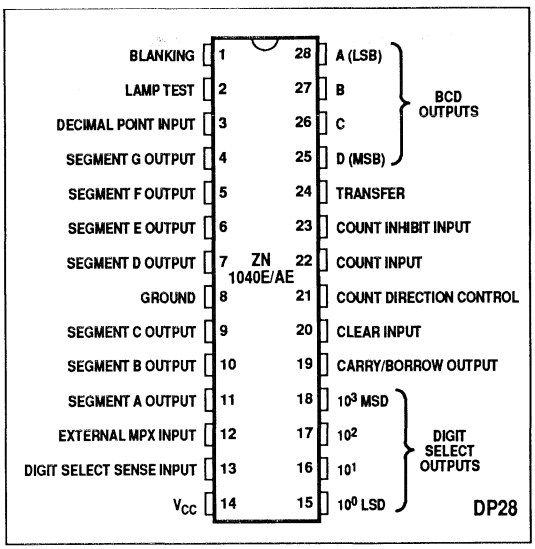
The measurement of oscillator period is a much quicker method of calibration and this is made possible on the ZN1036 by the inclusion of a low impedance output. This output is Pin 12 and an external pull up resistor of 5-10k is required. This enables the designer to calibrate the oscillator easily without affecting its operation and without the necessity for a high impedance probe.

ZN1040E/AE
UNIVERSAL COUNT/DISPLAY CIRCUIT

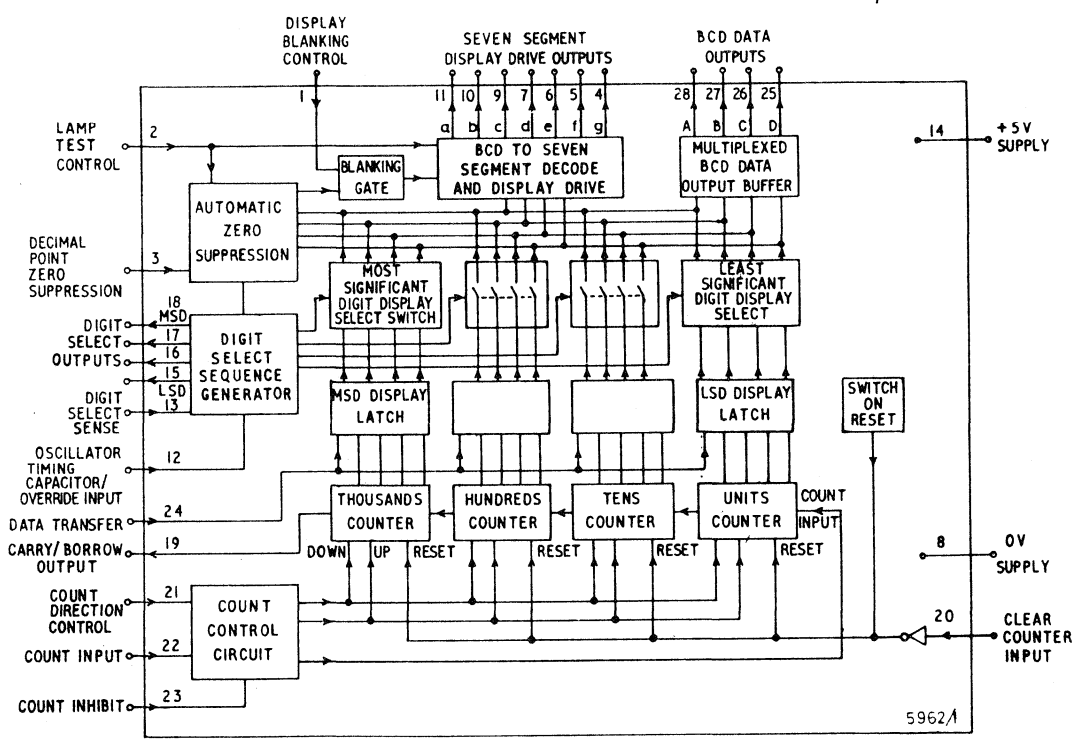
The ZN1040 is designed to satisfy the need for a universal count/display circuit suitable for the widest possible range of applications. This bipolar device allows fast count rates and high output currents to drive seven - segment LED displays, whilst BCD outputs allow interfacing to decoders for other types of display.

FEATURES

- 4 Decade synchronous up/down counter with Memory
- Carry/borrow output for direct synchronous Cascading
- BCD and seven-segment outputs
- Segment outputs can drive LED displays directly
- Schmitt trigger on count input for slow input Waveform
- Count inhibit gating
- Two versions: ZN1040E; high-speed; ZN1040AE, Low-cost
- Fully TTL compatible



Pin connections - top view



Function Diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage, Vcc	+5.5 V
Segment output currents	100 mA (ZN1040E) 80 mA (ZN1040AE)
Other output currents	25 mA
Operating temperature range	- 20°C to + 70°C(ZN1040E) 0°C to + 70°C (ZN1040A
Storage temperature range	- 55°C to + 125°C

ELECTRICAL CHARACTERISTICS: V_{CC} = 5V T_{AMb} = 25°C (unless otherwise specified)

Characteristics	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Count input positive going Threshold	V_T+	—	1.5	—	V	
Count input negative going Threshold	V_T-	—	1	—	V	
High level input voltage(1)	V_{IH}	2.0	—	—	V	
Low level input voltage(1)	V_{IL}	—	—	0.8	V	
High level input current	I_{IH}	—	—	20	µA	
Low level input current	I_{IL}	—	—	- 600	µA	
High level output voltage(2)	V_{OH}	2.4	3.3	—	V	I_{LOAD} = - 0.4mA
Low level output voltage(2)	V_{OL}	—	0. 25	0.5	V	I_{LOAD} = 16mA
Segment low level output Voltage (ZN1040E)		—	0.3	0.6	V	I_{LOAD} = 50mA
Segment low level output Voltage (ZN1040AE)		—	0.3	0.6	V	I_{LOAD} = 40mA
Maximum count rate (ZN1040E)		5	8	—	MHz	
Maximum count rate (ZN1040AE)		3	—	—	MHz	
Transfer pulse width		50	—	—	ns	
Clear pulse width		100	—	—	ns	
Supply voltage	V_{CC}	4.75	—	5.25	V	
Supply current(3)	I_S	—	90	—	mA	

NOTES (1) All inputs except count input
(2) All outputs except segment outputs
(3) All inputs and outputs open circuit

OPERATING NOTES

SECTION 1 : COUNTER

1.1 Counter Operation

The counter section of the ZN1040 is a synchronous four decade BCD counter. Each decade consists of four flip-flops which are clocked simultaneously on the positive going edge of the count input pulse. Suitable steering logic ensures that the 16 flip-flops count in a four decade BCD sequence. The BCD outputs of the counter are connected to data latches in which the count may be stored for subsequent decoding and display.

The counter and count control circuitry are shown in figure 1 whilst the count input and inhibit input circuits are shown in more detail in figure 2.

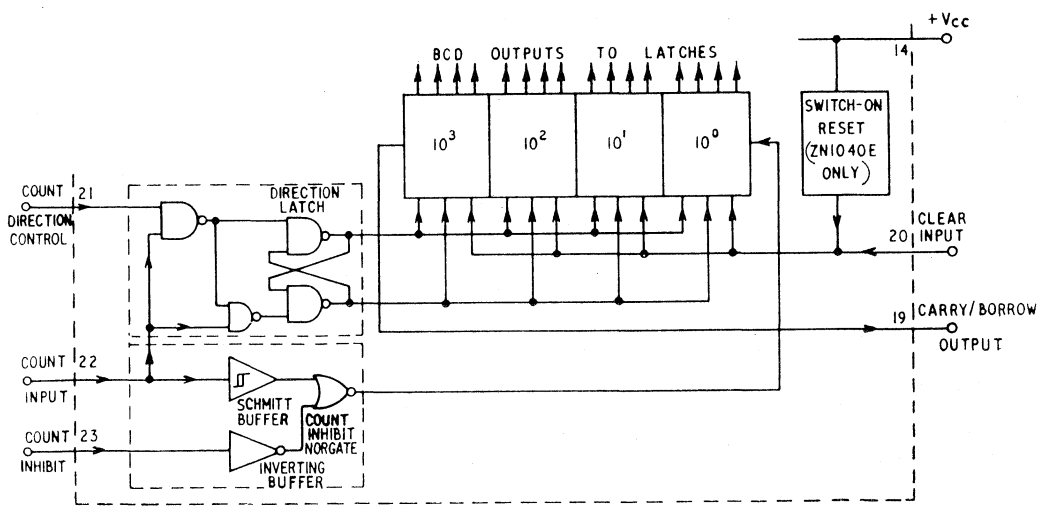


Fig. 1. Count System Functional Diagram

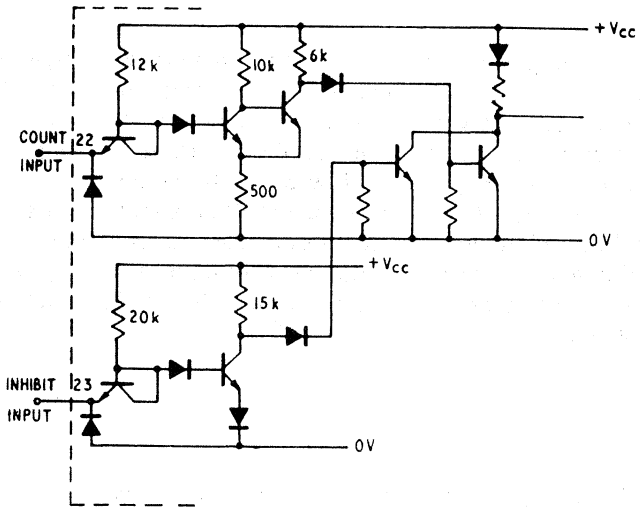


Fig. 2. Count Input and Inhibit Circuit

Counting occurs on the positive going edge of the count input pulse.

The counter input consists of a Schmitt trigger which allows the counter to operate reliably from input waveforms with very slow edges. It also allows a very simple anti-bounce circuit to be used when the count input is taken from a mechanical contact as shown in figure 3.

Bounce occurs mainly on contact closure. R_2 is made very much smaller than R_1 so that when the contact closes C_1 discharges rapidly to below the lower threshold of the Schmitt trigger. However, if the contact subsequently opens due to bounce, the time constant $(R_1 + R_2)\ C_1$ is of sufficient length so that C_1 does not charge to the upper threshold of the Schmitt trigger. When the contact genuinely opens then C_1 will charge and the counter will be clocked. The values of R_1, R_2 and C_1 will depend on the contact characteristics and the maximum count rate.

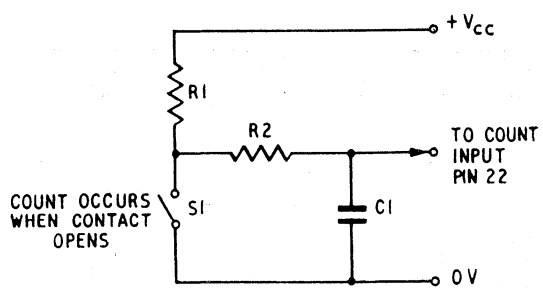


Fig. 3. Anti-Bounce Circuit

1.2 Inhibit Input

The inhibit input is used to gate the count input pulses. When the inhibit input is high then the second input of the inhibit NOR gate is low and count pulses are allowed through. However, when the inhibit input is taken low, the second input of the inhibit NOR gate is taken high. This holds the output low so that the count pulses are blocked. Correct timing of the inhibit control is important. If the inhibit control is taken low when the count input is low then an extra positive going edge will be fed through the inhibit NOR gate and an extra count will result as shown in figure 4a. The inhibit input should thus be operated when the count input is already high as shown in figure 4b. If the count input waveform has a duty cycle which is not 50% then it is advisable to arrange that it is normally high, as in figure 4b, since this makes operation of the inhibit control simpler.

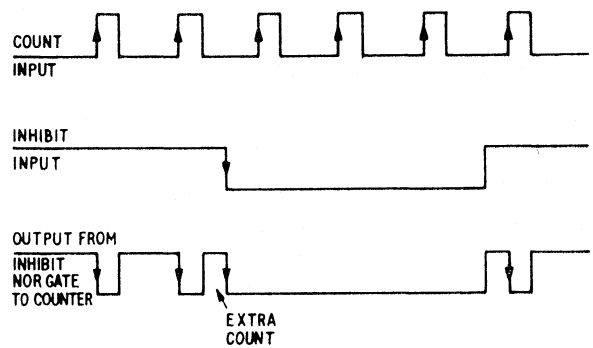


Fig. 4a. Incorrect Inhibit Operation

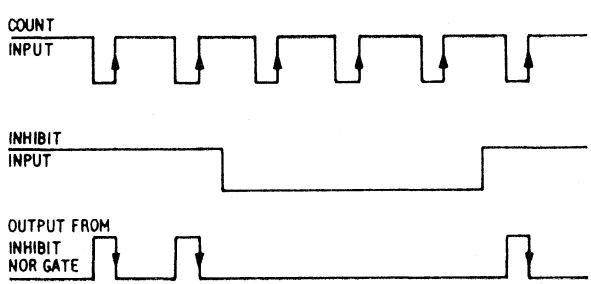


Fig. 4b. Correct Inhibit Operation

1.3 Direction Control

Count direction is controlled by a 'D' latch (see section 1.1) which can be set, for counting up, by taking the mode input high and reset, for counting down, by taking the mode input low. The clock input of this latch is connected to the count input and the state of the latch may therefore be changed only when the count input is high. If the count direction is to be reversed at a particular count then the state of the direction latch must be changed immediately that count is reached, whilst the count input is still high. Waiting until the count input has gone low again will result in the count direction not being reversed until the count input has gone high again, by which time an additional count will have been made in the original direction. Incorrect and correct operation of the direction control is illustrated in figures 5a and 5b.

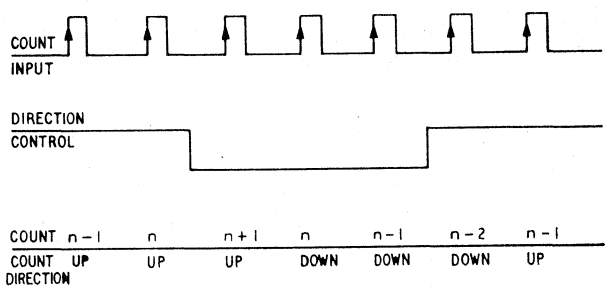


Fig. 5a. Incorrect Operation of Direction Control

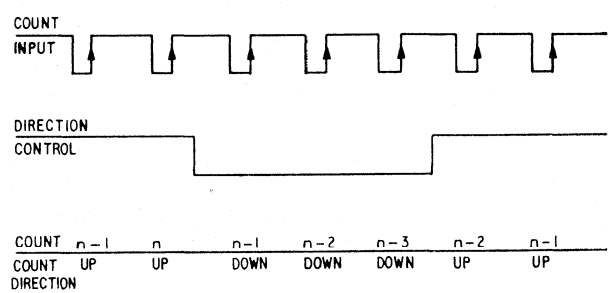


Fig. 5b. Correct Operation of Direction Control

1.4 Counter Reset

The counter may be reset to zero at any time by taking the clear input low. The counter will remain reset until the clear input is taken high again. In addition the ZN1040E incorporates a 'power-on' reset facility which resets the counter to zero when the power is first applied to the IC. This function is not available in the ZN1040AE.

Whichever version of the IC is used, care must be taken to set the direction latch to the correct state immediately after switch-on, otherwise the initial count may be made in the wrong direction. This may occur if the count input is low at switch-on since the direction latch may then set in either state. It is therefore advisable to ensure that the count input is normally high so that the direction latch will be set to the correct state at switch-on by the count direction control.

1.5 Carry/Borrow Output

The carry/borrow output (pin 19) may be used as an overflow indicator or to facilitate direct cascading of ZN1040's. When the count direction is UP then the carry output will go high on the next low-going edge of the count input after a count of 9999 is reached. The carry output will go low again on the next high-going edge at the count input, when the count changes to 0000.

When the ZN1040 is in the count DOWN mode then the carry output will go high on the next low-going edge at the count input after the counter reaches 0000. The carry output will go low again on the next high-going edge at the count input, when the count changes to 9999. In either case the carry output is subject to a propagation delay, t_C of typically 75 ns, relative to the count input edges.

Carry output timing for both up and down counting is shown in figures 6a and 6b.

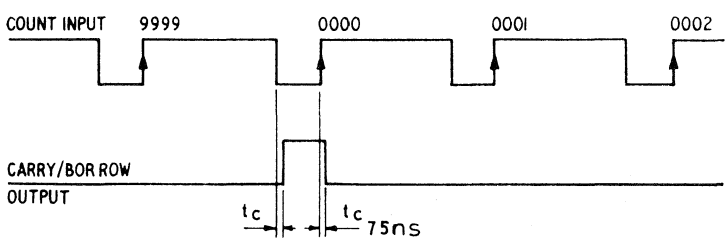


Fig. 6a. Carry Output Timing for Up Count

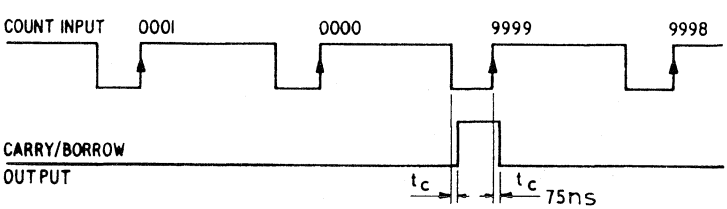


Fig. 6b. Carry Output Timing for Down Count

SECTION 2. COUNT MEMORY

2.1 Display Latch

Each of the decade counters in the ZN1040 produces a binary coded decimal (BCD) number synchronous with the count input. The counter outputs are connected to the inputs of data latches which can store the counter outputs for subsequent display. Whilst the transfer input (pin 24) is high the latches are transparent, and their outputs will follow the data present at the inputs. When the transfer input is taken low the input data present at that instant will be held in the latches and will be unaffected by subsequent changes in the counter outputs.

SECTION 3. DISPLAY MULTIPLEXING

3.1 Multiplex System

In order to economise on pin connections to the ZN1040 and to simplify connection to displays the outputs of the ZN1040 are multiplexed, i.e. the four BCD output digits from the data latches are connected, one at a time, to a common data bus. The multiplexed BCD data is connected to four output pins directly and also via a BCD seven-segment decoder driver so that multiplexed seven-segment outputs are also available. Four digit select outputs indicate which digit is present on the BCD or 7-segment outputs at a particular time.

3.2 Internal Multiplex Oscillator

Clock pulses for the multiplex sequence are generated by the oscillator circuit shown in figure 7. An internal capacitor of nominally 5 pF is charged via a nominal 700k resistor to the upper threshold voltage of the Schmitt trigger. The Schmitt output then goes high, turning on the transistor, and the capacitor discharges through a nominal 10k resistor to the lower threshold of the Schmitt trigger, at which point the output of the Schmitt goes low, the transistor turns off, and the cycle repeats. The nominal frequency of the multiplex oscillator is 500 kHz but this can be altered by adding an external capacitor between pin 12 and ground. A graph of MPX frequency v. external capacitance is shown in figure 8. To ensure stable oscillator operation it is recommended that an external capacitor with a value of at least 100 pF should always be used. When displays are used with the ZN1040 it will frequently be necessary to keep the MPX frequency below 1 kHz to avoid 'ghosting' due to the storage time of the digit-drive transistors. On the other hand the MPX frequency should not be lower than a few hundred Hz otherwise display flicker may become noticeable.

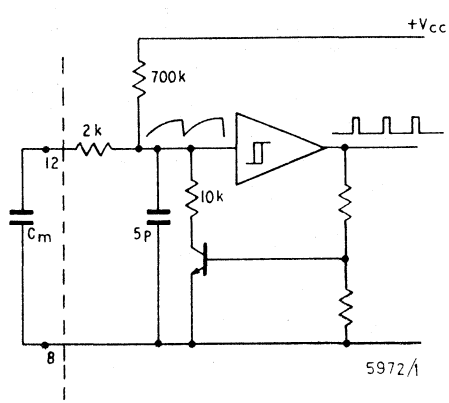


Fig. 7. Multiplex Oscillator Circuit

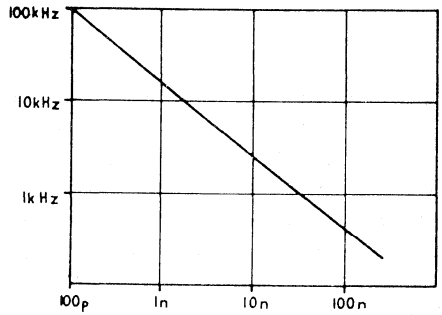


Fig. 8. Nominal MPX Oscillator Frequency v. External Capacitance

3.3 External MPX Oscillator

Since the Schmitt trigger input of the MPX oscillator is only coupled to three fairly high impedances (10k and 700k resistors, and a 5 pF capacitor) it is a simple matter to override the oscillator action by driving pin 12 from a low impedance external source such as a normal TTL output. Taking pin 12 high will hold the MPX oscillator output high, whilst taking pin 12 low will hold the output low. In this way the multiplexed BCD outputs of the ZN1040 can be synchronised to an external clock. This can be useful if, for example, the BCD output data is to be compared, digit by digit, with some preset limit. In this case the MPX frequency must at least be four times the input frequency to ensure that each digit has been compared before the next input pulse arrives.

The MPX input can be overdriven at frequencies up to 1 MHz which means that the BCD outputs can be compared at count frequencies up to 250 kHz.

3.4 Multiplex Sequence Generation

The output of the MPX oscillator is connected to the clock input of a sequence generator which is essentially a four-stage ring counter. This produces a sequence of four output pulses which are used to gate the BCD outputs, in sequence, on to the four output lines as shown in figure 9.

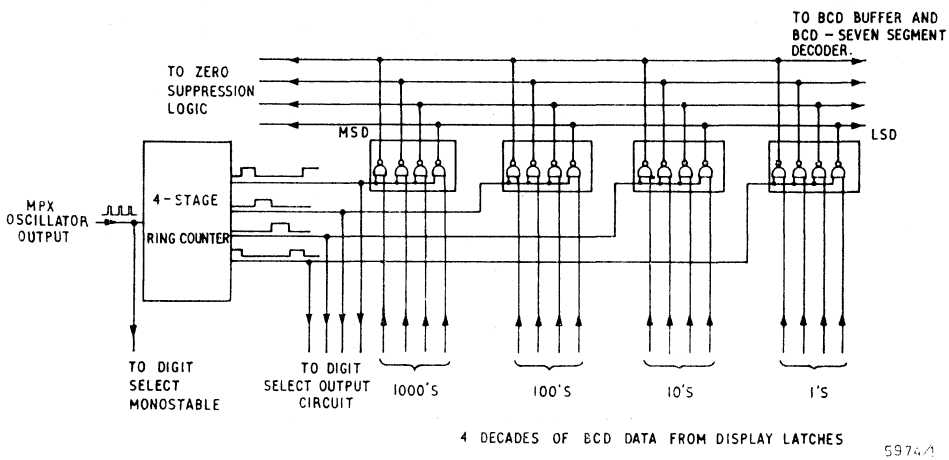


Fig. 9. Operation of Digit Multiplexing Circuit

3.5 Digit Select Output Circuit

The four digit select outputs are derived from the outputs of the MPX sequence ring counter using the circuit shown in figure 10.

To minimise digit drive overlap they are first passed through NAND gates, and a monostable triggered by the MPX oscillator takes a 200 ns 'bite' from the high-going edge of each pulse to provide interdigit blanking.

Further gating allows the selection of either high-going or low-going digit select pulses, thus allowing either common-anode or common-cathode displays to be driven using simple circuits. When the digit select sense input (pin 13) is high then the digit select pulses are high-going, when this input (pin 13) is low the digit select pulses are low-going. A timing diagram for high-going digit select pulses is given in figure 11. For low-going pulses the digit select waveforms are simply inverted. One digit select equivalent output circuit is shown in figure 12.

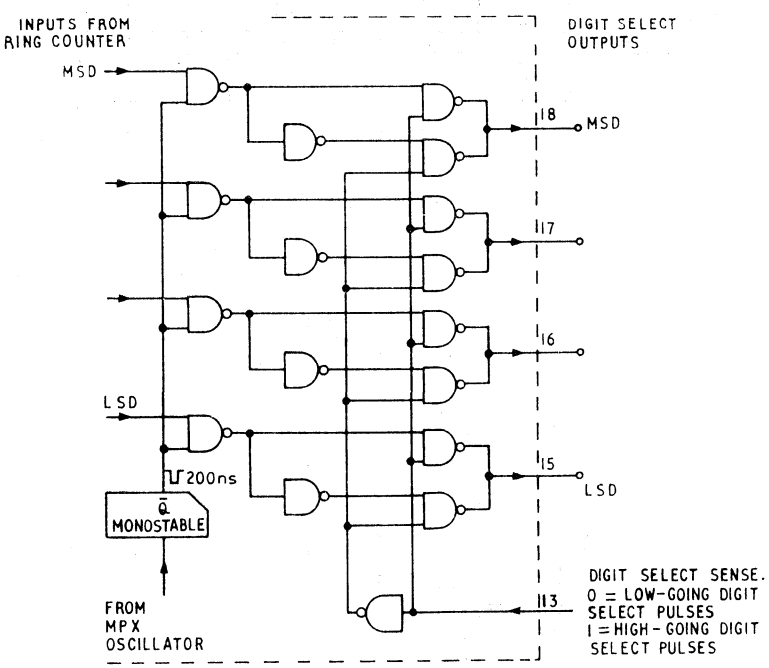


Fig. 10. Digit Select Logic

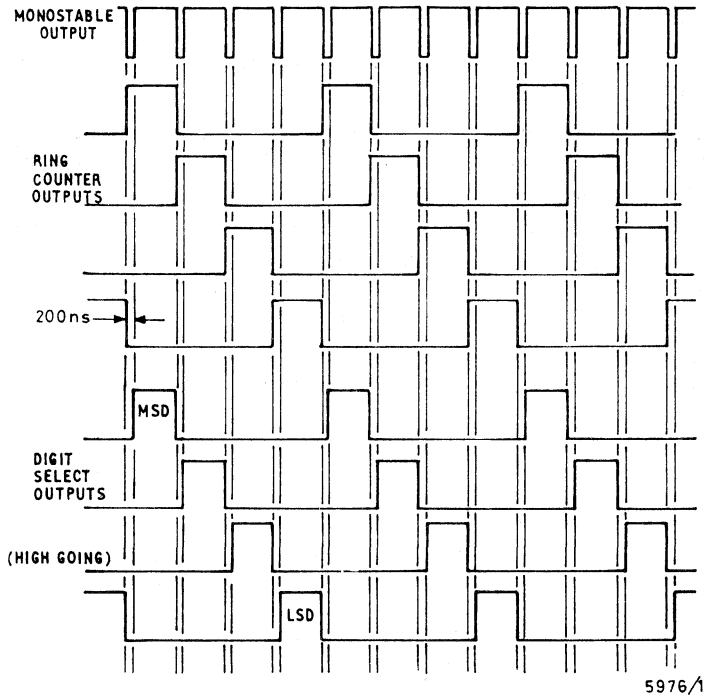


Fig. 11. Digit Select Timing

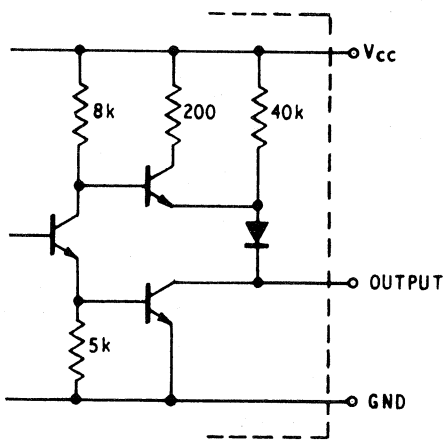


Fig. 12. Digit Select Output Circuit

3.6 Seven-segment Outputs

The seven segment outputs (pins 4-7, 9-11) are active low and can sink at least 50 mA in the case of the ZN1040E and 40 mA in the case of the ZN1040AE. The segment cathodes of common-anode displays may thus be driven directly. Display driving is discussed in detail in section 5. The output circuit for one segment is shown in figure 13.

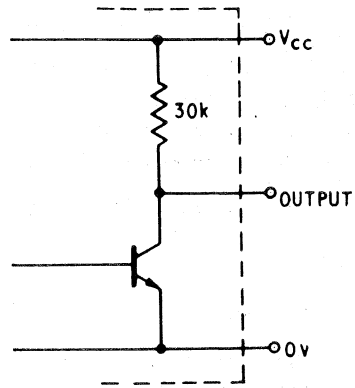


Fig. 13. Segment Output Circuit

3.7 BCD Outputs

The BCD output for each digit appears on the BCD output lines synchronous with the appropriate digit select pulse. However, since the MPX sequence gating is driven directly from the ring counter outputs, there is no inter-digit gap between one set of BCD data and the next. During the transition between digits the BCD data must therefore be considered invalid. If the BCD data is to be utilised (e.g. stored in an external latch or compared) then the simplest way to overcome this problem is to make use of the leading edge of the digit select pulse to indicate when the data is valid. This is illustrated in figure 14.

Similar comments also apply to the seven-segment outputs, but since these are normally used only for display driving, the problem does not usually arise.

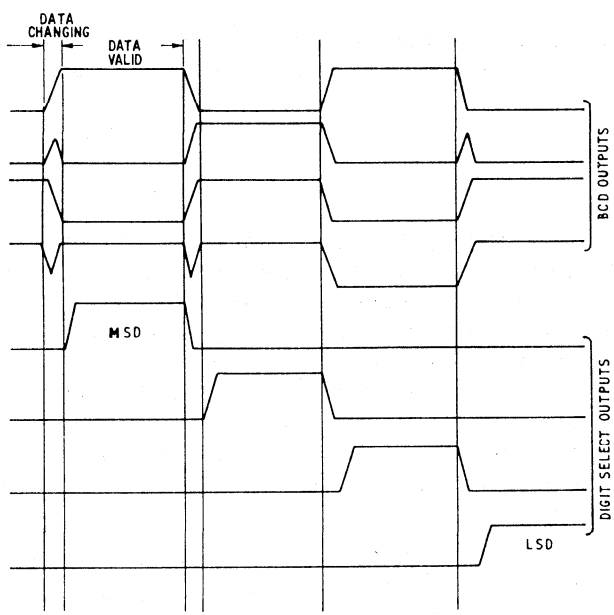


Fig. 14. BCD Output Timing

SECTION 4. ZERO SUPPRESSION, BLANKING, DECIMAL POINT AND LAMP TEST

The ZN1040 provides automatic blanking of leading zeroes in the display, thus improving readability. A decimal point input is also provided which allows leading zeroes to be displayed where these occur after the decimal point. A blanking input is provided to inhibit the display together with a lamp test input to check the operation of all display segments.

These sections of the ZN1040 circuit are shown in figure 15.

4.1 Blanking

Operation of the blanking input is extremely simple. When this input is high the seven-segment decoder functions normally and when this input is taken low the output of AND gate N6 goes low and the seven segment output transistors are all turned off, blanking the display.

4.2 Zero Blanking

Zero blanking operates on the principle of leaving the display blanked until non-zero data is detected at the outputs of the digit select gates. The trailing edge of the LSD output of the ring counter triggers a monostable which sets flip-flop N4/N5. The output of N4 holds one input of N6 low and the display is therefore blanked. It remains blanked until a non-zero digit appears on the BCD data bus, thus taking one or more of the inputs of NOR gate N3 high. The output of N3 then goes low resetting flip-flop N4/N5 so that the leading non-zero digit and all subsequent digits are displayed.

Should all four digits be zero then the flip-flop will be reset when the LSD output of the ring counter goes high and the output of N1 goes low. This ensures that the right hand digit (LSD) is always displayed, even if zero.

4.3 D.P. Input

If not used, the decimal point input is normally held high. If a decimal point is used in the display then the D.P. input can be utilised to prevent the possibility of a blanked digit appearing after the decimal point. This is achieved by feeding a low-going pulse into the D.P. input synchronously with the digit select pulse for the digit where the decimal point is to appear. This resets flip-flops N4/N5 so that the display is unblanked for this digit and all subsequent digits even if there are leading zeroes after the decimal point. Depending on whether the display has left or right-hand decimal points the display will be of the form .0 —— or 0. ——. If there is to be a decimal point before the MSD then left-hand point displays must obviously be used. If no leading zero blanking is required then the D.P. input is simply grounded, when all digits will be displayed.

A timing diagram for the D.P. input is shown in figure 11. Applications circuits using the decimal point are given in section 5. It should be pointed out that the ZN1040 does not produce an output to drive the decimal point of a display, this must be done using a simple external circuit several of which are shown in section 5.

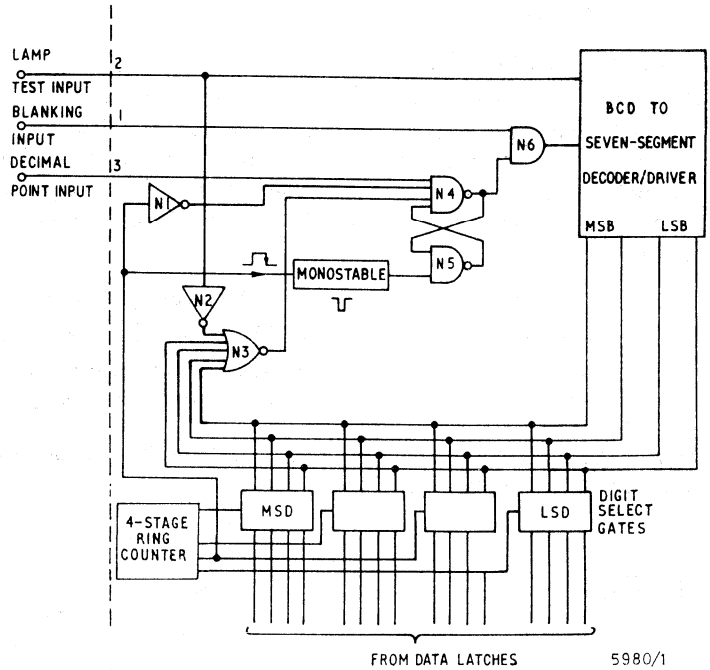


Fig. 15. Zero Suppression, Lamp Test and Blanking

4.4 Lamp Test

Operation of the lamp test function is quite simple. Taking the lamp test input low applies the BCD code 1000 (8) to the inputs of the BCD seven-segment decoder/driver. Simultaneously flip-flop N4/N5 is reset via N2 and N3, the output of N6 goes high, the display is unblanked and displays 8888. The blanking input must be high for lamp test to operate as a low blanking input will override the lamp test input and blank the display.

SECTION 5. USING THE ZN1040

5.1 Driving Common Anode LED Displays

Common anode LED displays can be driven with a minimum of external components, using the circuit of figure 16. The segment cathodes are driven directly (via current limit resistors) whilst the low going digit outputs turn on PNP digit drive transistors. As the display is multiplexed, and each digit is thus active for only a quarter of the time, the segment resistors should be chosen to give a peak current of approximately four times the required average current by using the equation:

$$R = \frac{V_{CC} - V_f}{4I_S}$$

V_{CC} = supply voltage (volts)
V_f = LED forward voltage drop
I_S = average segment current (A)
R = segment resistance (Ω)

The base resistors of the PNP digit drive transistors should be chosen such that the transistors receive sufficient base current to turn them fully on.

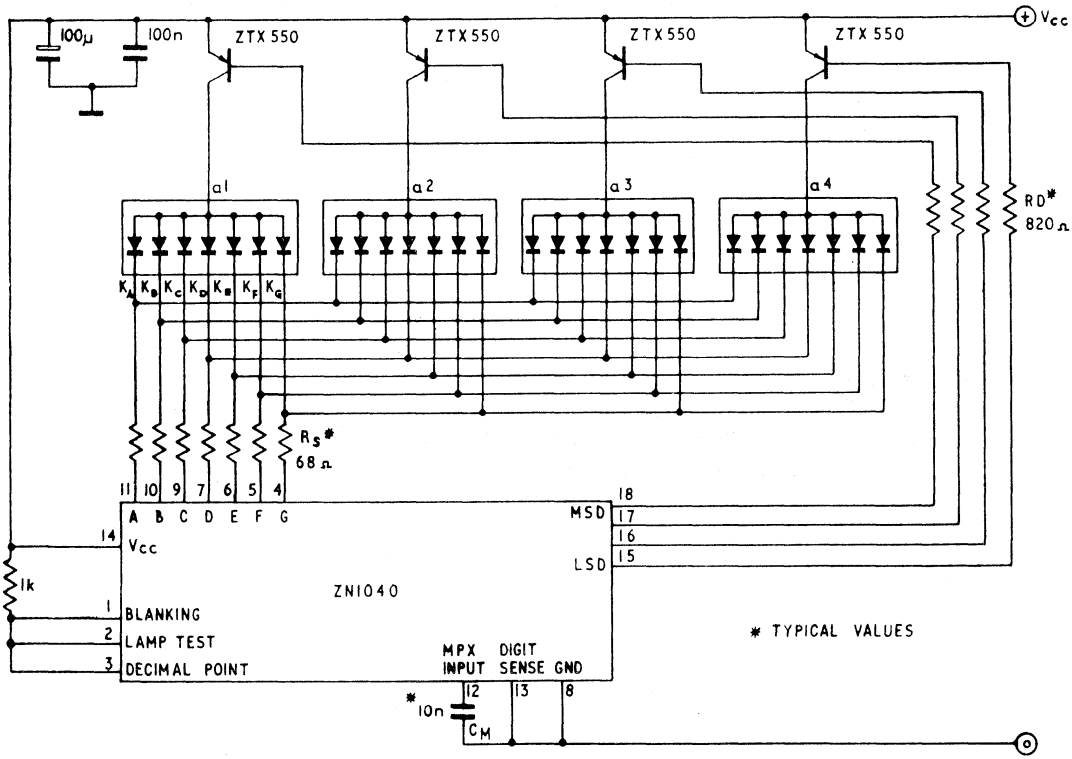


Fig. 16. Interfacing to Common-Anode LED Displays

5.2 Driving Common Cathode LED Displays

A circuit for driving common cathode LED displays is given in figure 17. Since the segment outputs are only active low it is necessary to use PNP segment drive transistors. High going digit select outputs are used to turn on NPN digit drive transistors. As with the common anode display, the segment resistors should be chosen to give the required segment current, and the transistor base resistors should be chosen to turn the transistors hard on. In both cases it is advisable to use displays which are optimised for multiplexed operation. Note that, since the digit outputs have to supply a significant base current to the digit drive transistors, the high level output voltage is less than the minimum specified to drive a TTL input. The digit select outputs therefore cannot be used as normal logic outputs with this circuit configuration.

Good decoupling of the supply to the ZN1040 is essential to avoid erratic counting and other problems. This is especially true when displays are being driven because of the large current pulses taken by these devices. It is therefore recommended that an electrolytic capacitor of between 100 μF and 1000 μF and a 100 nF ceramic capacitor be connected between $+V_{CC}$ and ground, as close as possible to the appropriate pins of the ZN1040.

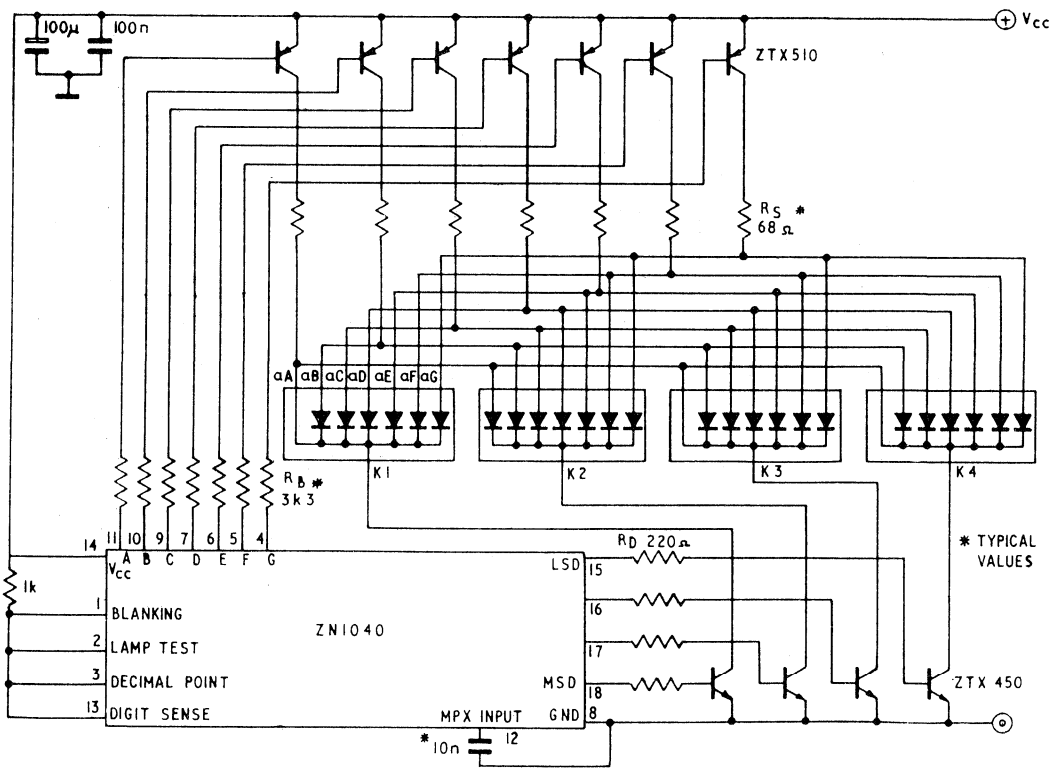


Fig. 17. Interfacing to Common-Cathode LED Displays

5.3 Using the Decimal Point Input

(a) Common Anode Display

Figure 18 shows a circuit which allows a decimal point to be displayed before any one of the display digits. When all the decimal point inputs are low then the 'wire-ANDed' outputs of N5 to N8 are all high and no decimal point is displayed. If for example D.P. input 2 is taken high then, when digit select output 2 goes low, both inputs of N6 will be high. The output of N6 will therefore go low synchronous with the digit 2 select pulse which will apply a low going pulse to the D.P. input of the ZN1040 to unblank the display and also to the decimal point cathode of the display to light decimal point 2.

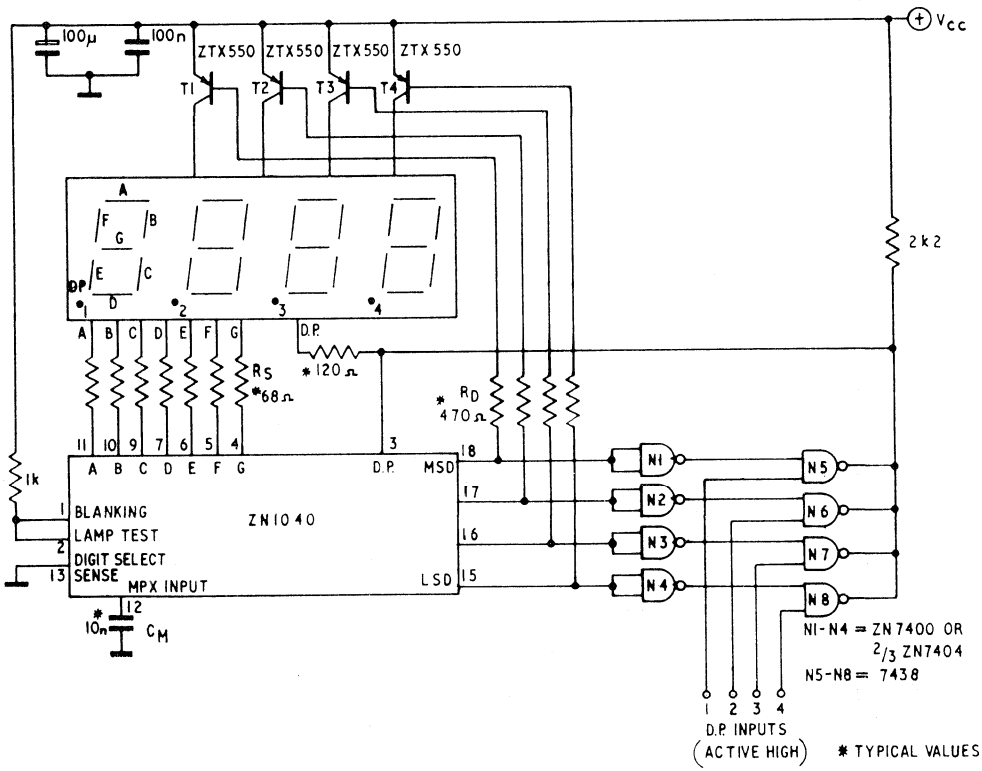


Fig. 18. Driving a Multiplexed Common-Anode Display with Decimal Point

(b) Common Cathode Display

The principle of this circuit is identical to that of figure 18 with minor circuit differences to take account of the different type of display. The digit select outputs are high-going, therefore no inverters are required at the inputs of the NAND gates. However, since the digit select outputs are used as logic outputs (see 5.2), buffers N1-N4 are interposed between them and the digit drive transistors. The wired AND output of N5-N8 turns on T8 when it goes low synchronous with the chosen digit select pulse thus driving the decimal point anode.

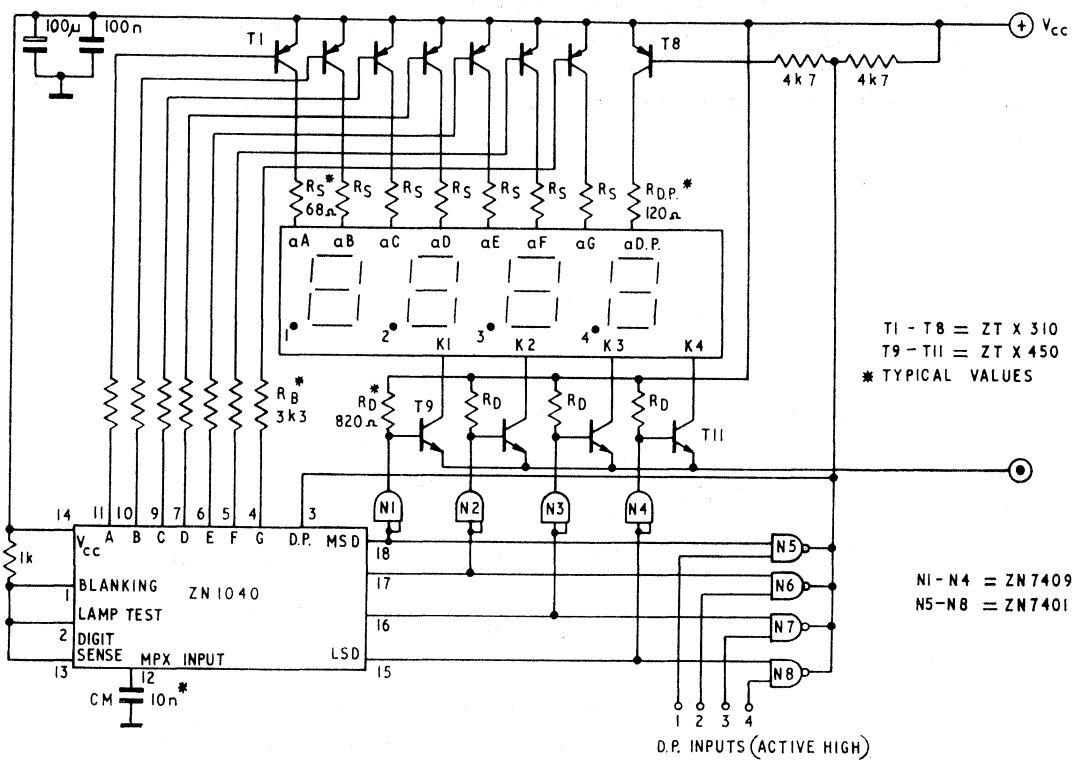


Fig. 19. Driving a Multiplexed Common-Cathode Display with Decimal Point

5.4 Cascading the ZN1040

If a count greater than 4 digits is required then two ZN1040's may be cascaded using the carry/borrow output; or additional TTL decade counters may be added. To cascade two ZN1040's the carry/borrow output of the less significant counter is connected to the inhibit input of the more significant counter and the count inputs are linked as shown in figure 20. The M.S.C. is thus inhibited until after the 9999th clock pulse when the inhibit input will be taken high by the carry output of the L.S.C. On the leading edge of the 1000th clock pulse the M.S.C. count will increase by 1 whilst the L.S.C. count will go to zero. After the carry propagation delay the carry output of the L.S.C. will go low and the M.S.C. will again be inhibited. A timing diagram for this sequence of events is shown in figure 21.

The leading zero blanking facility of the ZN1040 cannot be used directly in this application since the blanking circuits would operate independently for each device, leading to gaps in the display when the count was 999 or less, e.g. – – – 0 – 456.

This problem can be overcome by grounding the D.P. inputs of both counters thus inhibiting the zero blanking, or alternatively the D.P. input of the L.S.C. may be grounded giving zero blanking only on the first three digits of the M.S.C. If full zero blanking is required then the circuit given in Section 5.5 should be used.

When ZN1040's are cascaded then separate display interfacing will be used for each set of four digits.

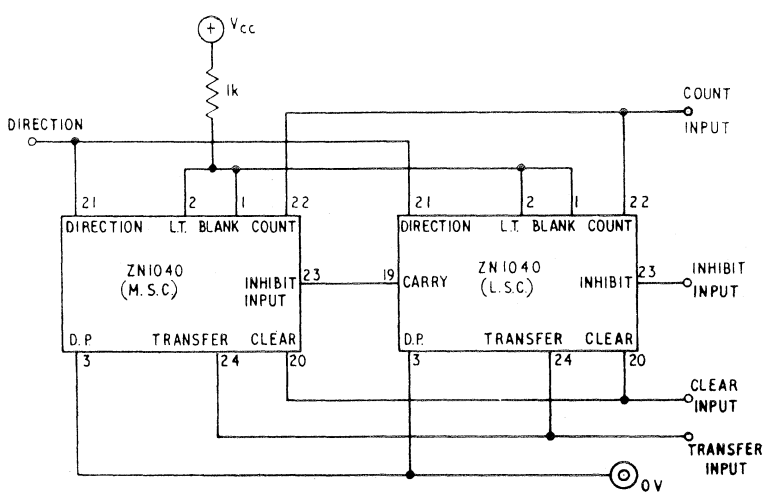


Fig. 20. Cascading ZN1040's without Leading Zero Blanking

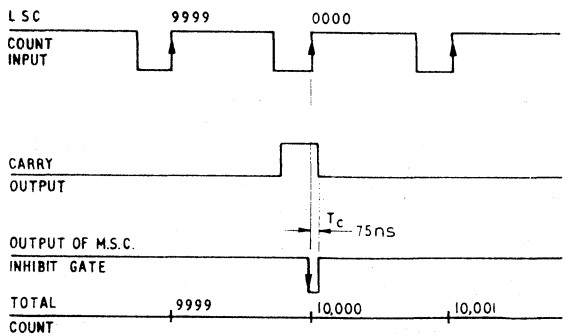


Fig. 21. Timing Diagram for Cascaded ZN1040's

5.5 Cascading ZN1040's with Leading Zero Blanking

The circuit of figure 22 allows cascading of two ZN1040's with full leading zero blanking. It operates by monitoring the BCD outputs of the more significant counter. When these are all zero this counter is blanked and the less significant counter is allowed to operate with leading zero suppression. When any of the BCD outputs is non-zero then the M.S.C. is unblanked and operates with leading zero suppression whilst the zero blanking of the L.S.C. is inhibited. The BCD outputs of the M.S.C. are monitored by a four input open collector NOR gate comprising N2 and N3. Whilst the multiplexed BCD data is zero the outputs of N2 and N3 are high, the output of N1 is low, so that M.S.C. is blanked. The output of N4 holds the D.P. input of the L.S.C. high and therefore the leading zero blanking operates normally.

If, at any time during the multiplex sequence, the BCD data is non-zero, then the output of N2 or N3 will go low discharging C1 rapidly. The D.P. input of the L.S.C. will thus be pulled low, inhibiting the zero blanking, whilst the output of N1 is high, unblanking the M.S.C. If only one of the BCD digits is non-zero, then C1 will be discharged only once during each multiplex sequence and will charge in the interval. The time constant (R2 + R3) C1 must therefore be made considerably longer than one multiplex sequence to ensure that the input to N1 remains low in this event.

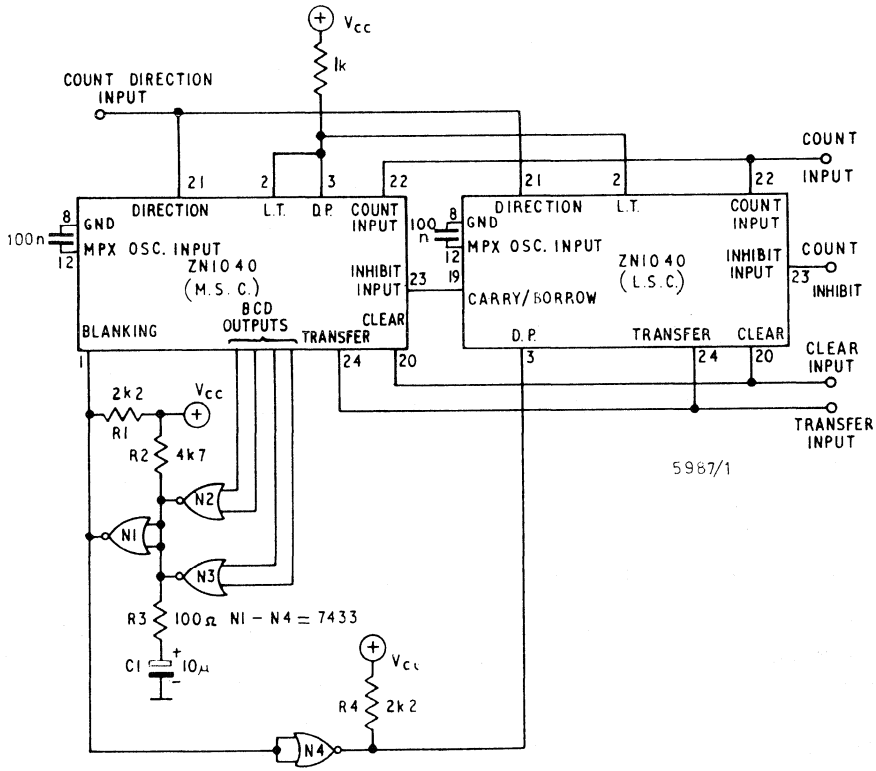


Fig. 22. Cascading ZN1040's with Leading Zero Blanking

ZN1044E

PROGRAMMABLE COUNTER TIMER INTEGRATED CIRCUIT

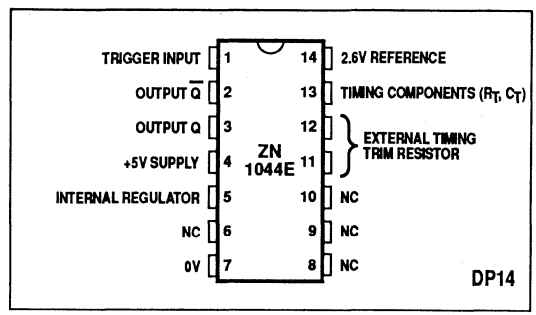
The ZN1044 combines linear and digital functions on the same chip such that simple precision timers can be constructed using the minimum of low cost external components. The frequency of an on-chip oscillator is determined by an external capacitor and resistor. Fine adjustment can then be achieved by the variation of an external trimming resistor.

Pulses from the oscillator are fed into a 12 bit counter and the output changes state after 4095 pulses.

In this way precise time periods can be defined by timing capacitors and resistors of much smaller value than would be required by single RC time constant timers.

The count can be initiated either (a) with trigger input LO and supply going HI (supply initiation), or (b) with supply HI and trigger input going LO (trigger initiation).

The IC can operate from normal +5V logic supplies or from any higher voltage using a dropping resistor and internal shunt regulator connected to the supply pin.



Pin connections - top view

FEATURES

- Accurate and Repeatable Performance
- Complementary High Current Output Drivers
- Time Period Trimming
- Supply or Trigger Input Timing Initiation
- On-chip Regulator or TTL Supply Option
- Minimum of External Components Required
- Available in Plastic DIL (DP) Package

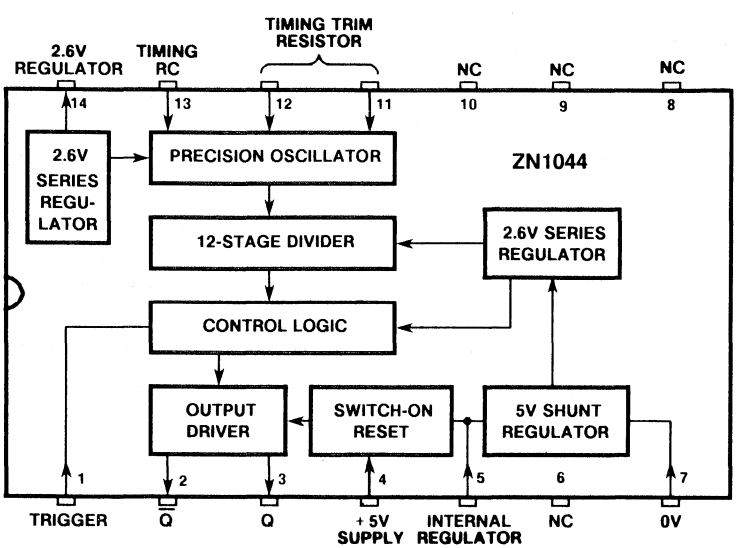


Fig.1 System diagram

ABSOLUTE MAXIMUM RATINGS

Dissipation	250mW derate above 30°C at 5mW/°C
Output source current	25mA
Output sink current	25mA
Operating temperature range	0 to +70°C
Storage temperature range	−55 to +125°C

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Timing section						See Note 5
Timing resistor	R_T	2k7		5M6	Ω	
Timing capacitor	C_T	0.1			nF	See Fig 2
Trim resistor	R_{trim}	0		560	kΩ	
Repetitive timing error			0.01		%	
Timing initiation and reset						
(a) Supply voltage initiation						
Voltage to initiate timing	V_{CC}	4.7			V	Supply applied to pin 4 with pin 1 connected to pin 7.
Rate of change of V_{CC}				0.25	V/μs	
(b) Trigger input initiation						
Voltage to initiate timing	$V_{T(LO)}$			1	V	
Voltage to prevent initiation of timing	$V_{T(HI)}$	2.2			V	
Minimum pulse to trigger			2		μs	
(c) Supply voltage reset						
Voltage to reset	V_{CC}		3.6		V	See note 2
External clock input						
Frequency				250	kHz	Clock input to pin 12 via a 10k resistor
Drive current	I_{clk}		0.1		mA	
Pulse width	t_{clk}	2			μs	
Pulse amplitude	V_{clk}	2.5		5.5	V	

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply						Note 4
(a) Externally regulated						connected to pin 4
Supply voltage	V_{CC}	4.5		5.5	V	V_{CC} = 5V
Supply current	I_{CC}		3.8	4.5	mA	outputs unloaded
(b) Internally regulated (5V shunt regulator)						Connect pin 4 to pin 5. See note 4.
Operating current range	I_R	5		55	mA	see Note 3
Regulated voltage	V_R	4.5		5.5	V	I_R = 10mA
Slope resistance			1.25		Ω	I_R = 7 – 55mA
Regulated voltage change with temperature			35		mV	I_R = 7 – 55mA t = 0 to +70°C
(c) Reference voltage (2.5V series regulator)						
Regulated voltage	V_{REF}	2.4	2.5	2.6	V	VCC = 5V, Pin 14 unloaded
Load current	I_{REF}		1		mA	V_{CC} = 5V
Slope resistance			2.5		Ω	
Output drive Q to $\overline{Q}$						V_{CC} = 5V
Output voltage	$V_{O(HI)}$	2.5	3.0	3.2	V	$I_{O(HI)}$ = 25mA
	$V_{O(LO)}$	0.3	0.4	0.6	V	$I_{O(LO)}$ = – 25mA
Output current	$I_{O(HI)}$			– 25	mA	Source
	$I_{O(LO)}$			+ 25	mA	Sink
Rise time	t_r		300		ns	I_O = 5mA, V_{CC} = 5V
Fall time	t_f		100		ns	I_O = 5mA, V_{CC} = 5V
Propagation delay V_T Low to V_O High	t_p		2.3	2.5	μs	
Temperature coefficient	T_C		0.008		%/°C	R_{TRIM} = 56k

Note 1 Time = MCR

C = capacitance in μF
R = resistance in MΩ
M = multiplying factor = 4095

For $t_{osc} \geqslant 10\mu s$

At $t_{osc} < 10\mu s$ this relationship no longer holds as the reset time becomes a significant fraction of t_{osc}

Note 2 In order to reset the timer the supply voltage should be reduced to 2V although reset may be typically acheived at 3.6V. Reset will not occur with the supply greater than 4V

Note 3 Since the +5V regulator cannot be used on its own without the rest of the circuit, the minimum operating current includes the 4.5mA maximum supply current taken by the timer.
Note 4 A 0.1μF capacitor should be connected between V_{CC} (Pin 4) and GND (Pin 7) at all times.
Note 5 Minimum recommended oscillator period = 4μs.

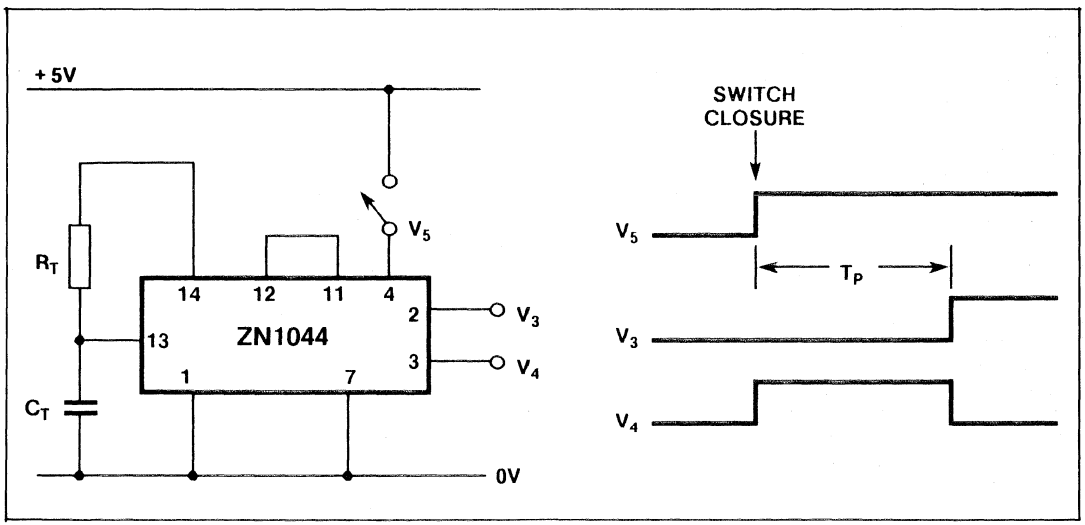


Fig.2

External components R_T and C_T determine the length of period T_P. The timing components set the period of an internal oscillator to $C_T R_T \pm 10\%$ and an internal divider causes a change in the output state after 4095 oscillator cycles.

When the time period is initiated Pin 3 goes Hi for a time period T_P. On completion of the time period, Pin 3 goes Lo and Pin 2 which was previously Lo goes Hi and remains Hi until the timing sequence is re-initiated.

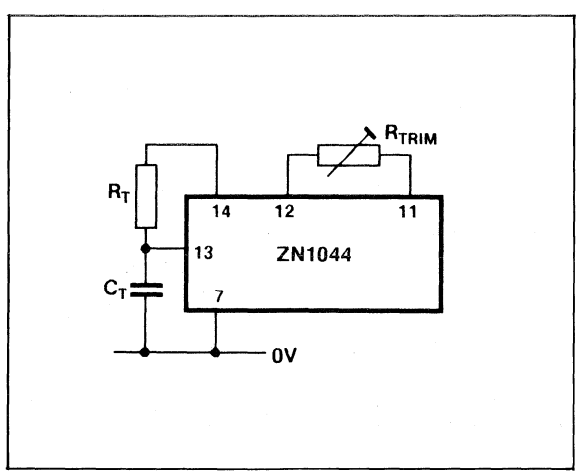


Fig.3

1.3 Design of variable period timers

Time periods from 16ms to infinity may theoretically be obtained using the ZN1044 integrated timer circuit. The following section should enable the designer to get the best possible circuit configuration achievable within the design limits. The necessary information is presente d below, Fig. 4., in the form of a timing components against oscillator period graph. The graph has been plotted using a 56kΩ trim resistor between Pins 11 and 12.The maximum range of oscillator period possible for a particular value - or timing capacitor can be easily obtained from the graph. To obtain the time period the oscillator period (Fig. 4) is mulitplied by the multiplying factor M which is 4095.

The periods obtained with the timing components selected from Fig. 4 may be trimmed to the exact time required using a variable resistor up to the value of 560kΩ between Pins 11 and 12.

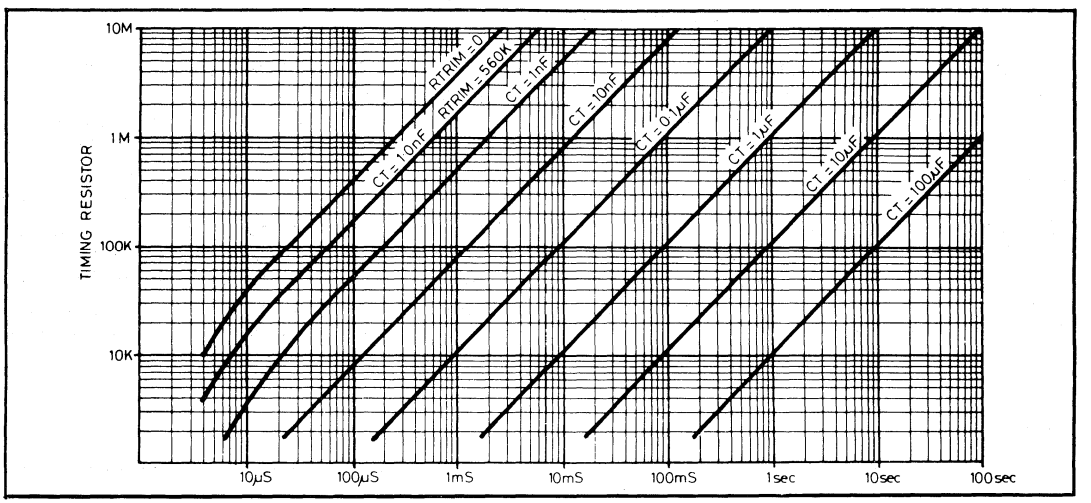


Fig.4 Oscillator period

SECTION 2 INPUT AND OUTPUT CIRCUITS

Note 2.1 External clock

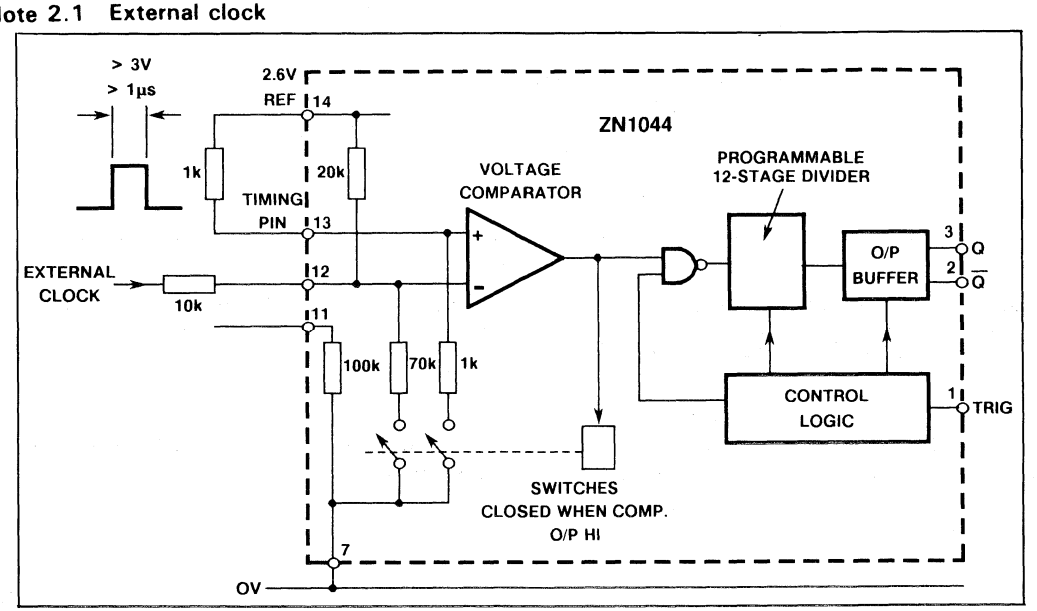


Fig.5

The ZN1044 can be used with an external clock as shown in the circuit of Fig. 5
The internal clock is disabled by connecting a 1k resistor from the timing Pin 13 to the + 2.5V reference, Pin 14 thus preventing the non-inverting i/p to the amplifier dropping below the inverting input voltage. The amplifier output is therefore Hi and the internal switches are closed.
An external clock pulse, provided it meets the limits defined in the characteristics, will override the disabling on Pin 13 and, if the trigger i/p on Pin 1 is Lo, will cause a pulse to be passed to the divider circuit.
The output Q and $\overline{Q}$ will change from Loto Hi and vice versa at the end of 4095 external clock pulses.

2.2 Timing initiation and reset

2.2.1 .Supply initiated

When Pin 1 is held Lo and the supply is switched on, the control logic and counters are automatically reset as the supply rises to its on voltage. This also initiates timing at the same instant by gating the oscillator output into the counter. After the set time the outputs change state and remain thus until the supply is switched off or another period is initiated. If, during such a timing cycle the trigger input is taken Hi, no matter how many times or for how long, the condition of the outputs and the length of the timing period will not be affected. If the supply drops below the rest level even for a few microseconds then the timing period will be terminated. It will be reset and restarted when the supply rises again above the reset level. Thus a supply drop-out has the effect of increasing the time period.

2.2.2.Trigger initiated

Allowing Pin 1 to rise with the supply prevents timer initiation by the supply.
Pulling the trigger input Lo now initiates a normal timing period. A further period may be initiated by dropping the trigger Lo again. This period is not affected when the trigger input level is altered during timing. The period is terminated again by the supply falling below the reset level. Since the normal condition of the trigger is Hi the timing will not restart on restoration of supply. A supply drop-out during a trigger initiated timing period has the effect of shortening the set time.

2.2.3 A simple repetitive timer

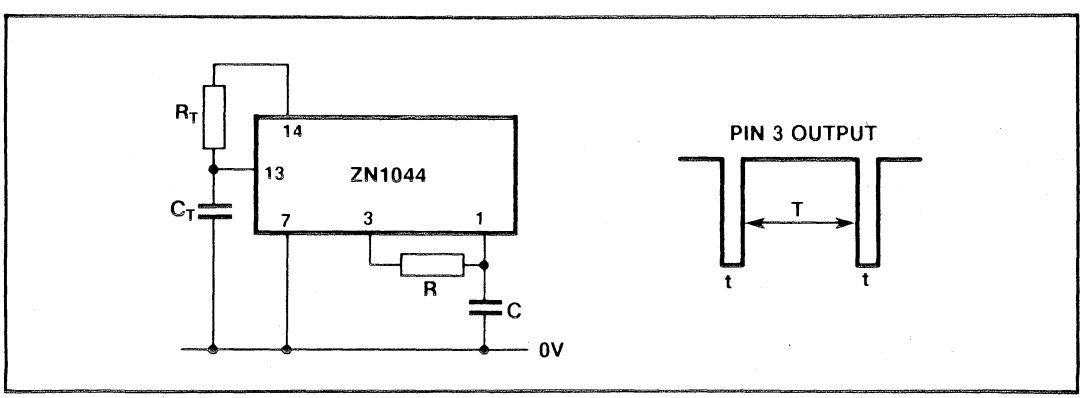


Fig.6

A capacitor and resistor in the feedback loop can be used and the pulse length t determined by the values of C and R. T is determined by timing components R_T and C_T. R may be any value up to 10k whilst C is limited to 10μF.

2.2.4 A simple closed loop timer

The ZN 1044 enables the designer to construct multistage timers with ease as one can be triggered by a single wire link from the output of another.

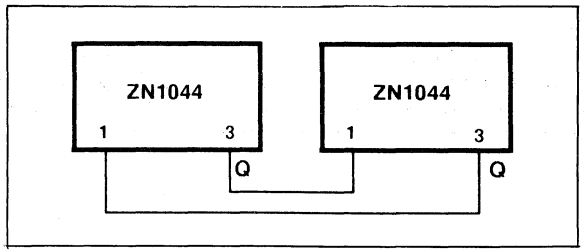


Fig.7

This may in theory be extended to any number of counters but for more than 3 there will be other modes of oscillation. For a ring of three, component tolerances will usually ensure that one mode is dominant with only one Q output Hi at a time. Higher numbers may not operate in the desired mode unless one set time is greater than the sum of all the others.

Fig. 8 shows a four stage ring timer.

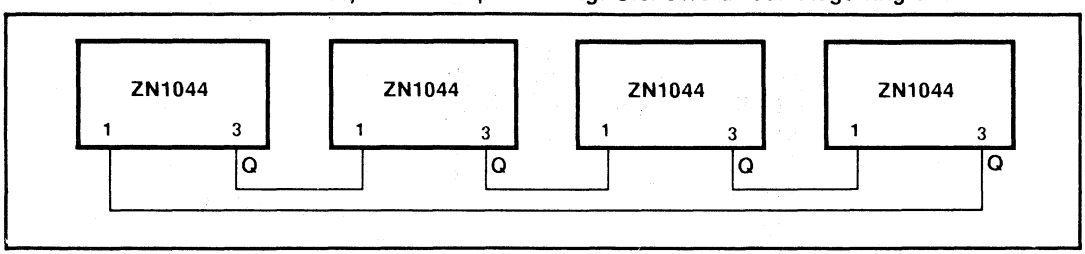


Fig.8

2.2.5. ZN1044 waveforms

The function of this device is demonstrated below as a Waveform diagram (Fig. 9)

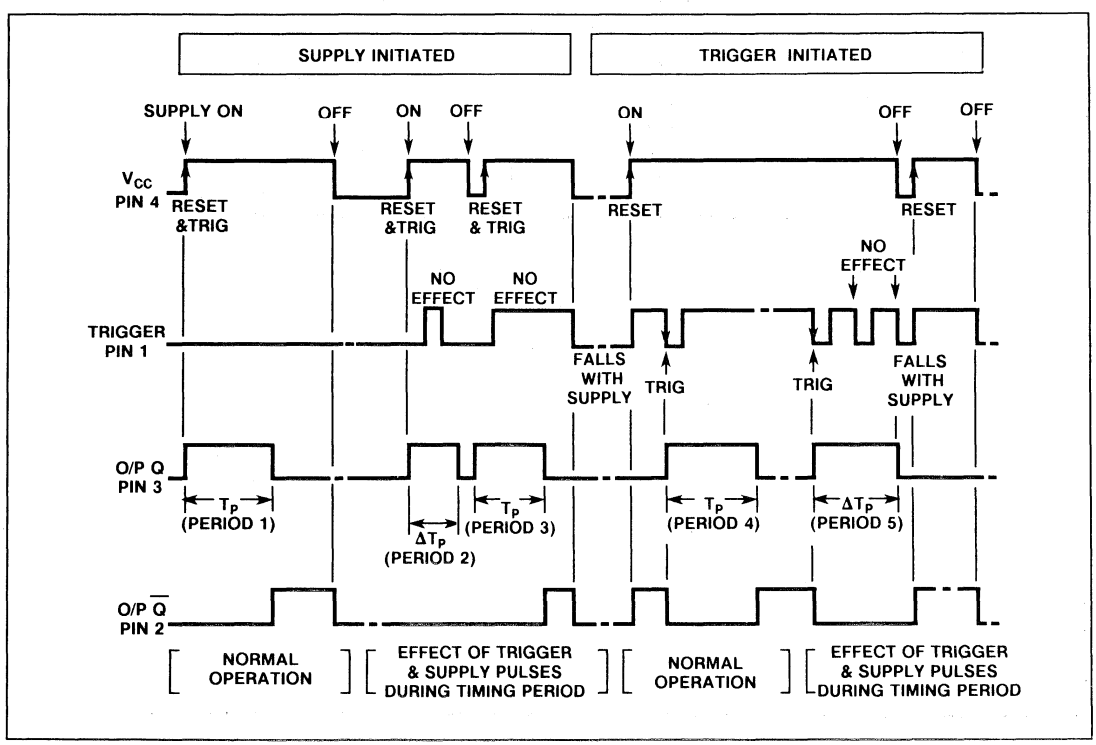


Fig.9

2.3 Trigger input circuit

The input circuit comprises of a buffer input followed by a schmitt trigger circuit. The buffer pull up resistor can be as low as 30kΩ. So to pull the input down below the IV threshold a pull down resistor of less than 5.6kΩ is recommended for worst case design.

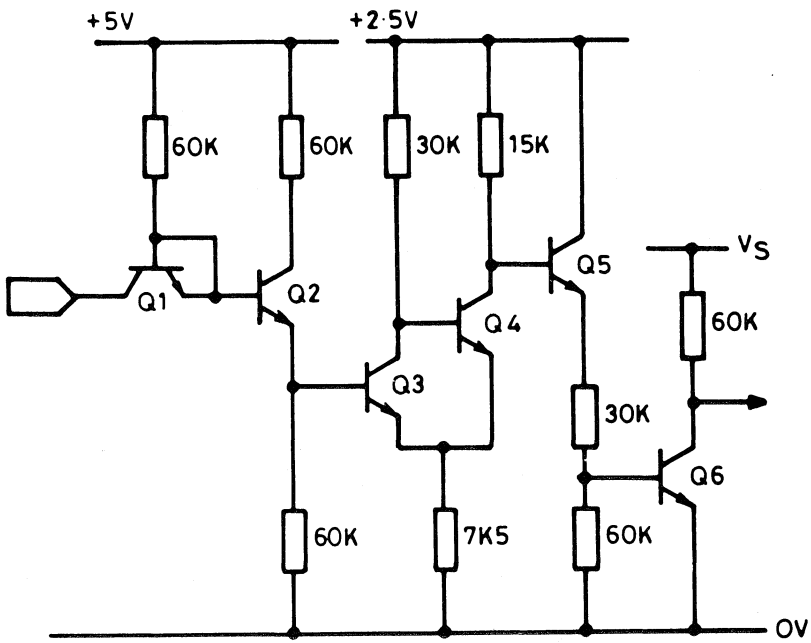


Fig.10

2.4 Output drive circuits

The Q and $\overline{Q}$ output drive circuits have the form illustrated in Fig. 11

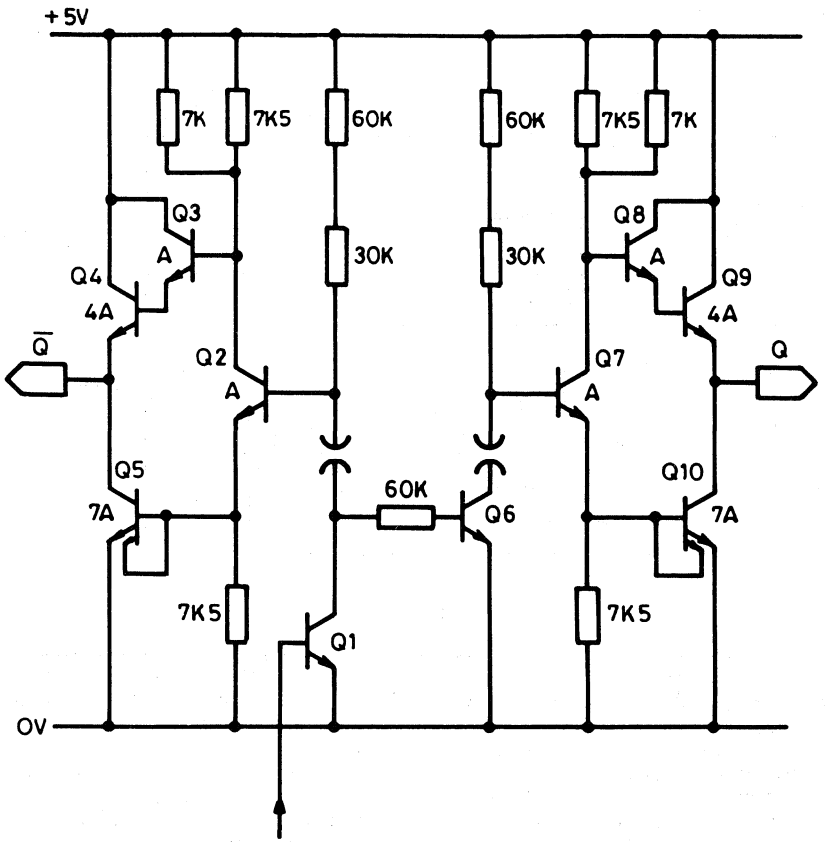


Fig.11

2.5 Load circuits

2.5.1 Transistor driven relay

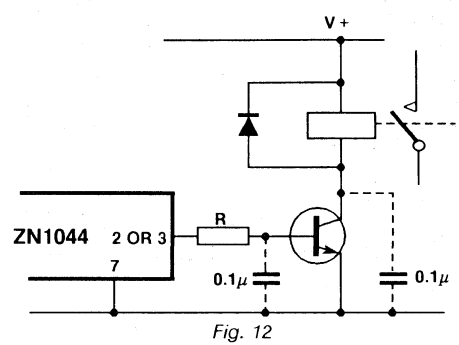


Fig. 12

The value of R is chosen to limit current to minimum required by the transistor under the worst condition.

If interference is experinenced suppression capacitors as shown may be needed.

2.5.2 Thyristor driven relay

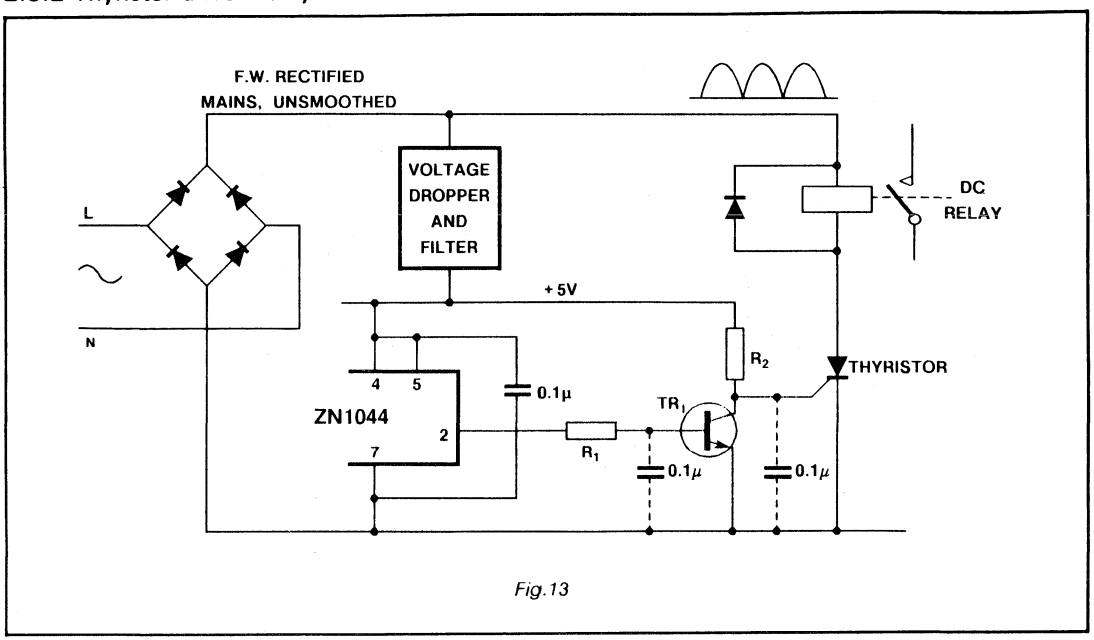


Fig.13

A thyristor gate may be driven via a limiting resistor directly from pin 2 for DELAY-TO-ON timers. Fig. 13 illustrates a circuit for achieving DELAY-TO-OFF using a thyristor. R_2 can be as high as 10k for low gate current thyristors. The thyristor is chosen such that the reduction in gate-cathode impedance achieved with a saturated transistor is sufficient to increase the holding current to a value which ensures turn OFF and R_1 is chosen so that the transistor (T_1) just reaches saturation.

For 240 volts a.c. mains it may be necessary to use a 110 volt d.c. relay with a dropping resistor of equal resistance since 220 volts d.c. relays are not easily obtainable.

2.5.3 Triac a.c. load circuit positive firing

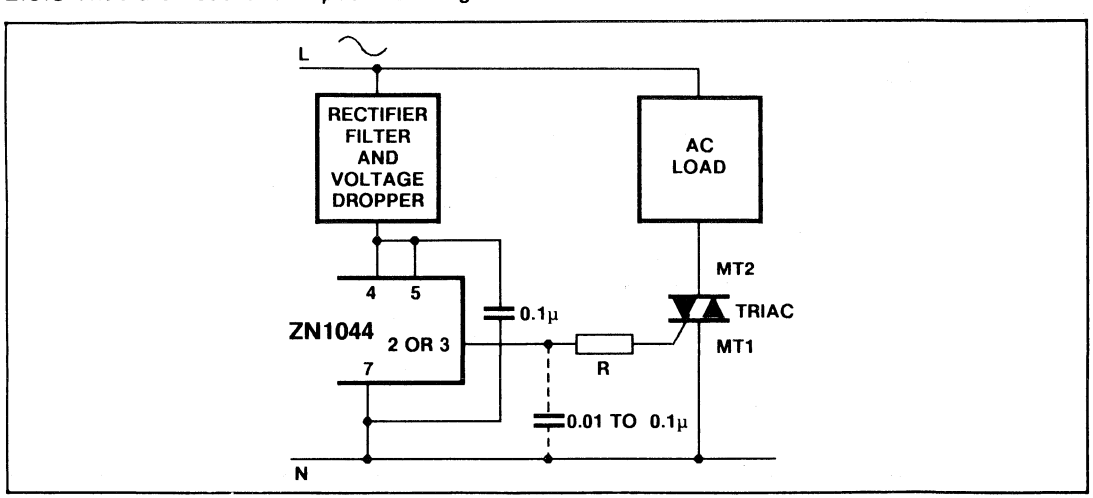


Fig.14

The value of R is chosen to limit the current to the minimum required by the triac for positive firing in both quadrants.

2.5.4 Triac a.c. load circuit negative firing

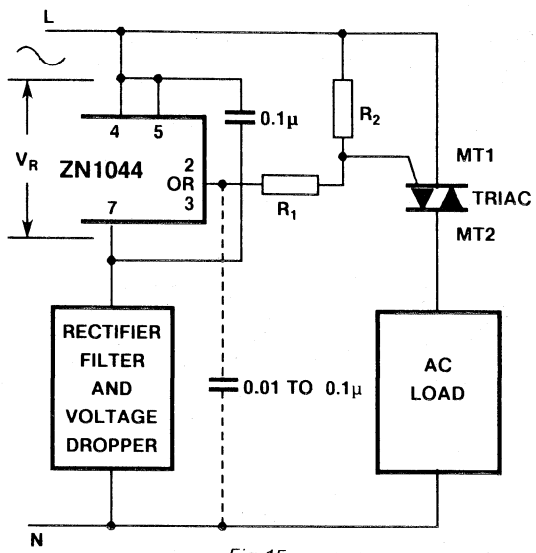


Fig.15

The value of R_2 is chosen to prevent any leakage currents biasing the triac gate ON during OFF periods. R_1 is chosen to limit the gate current to the maximum required by the triac for negative firing in both quadrants.

Triacs in general are easier to fire in the negative gate mode than the positive and in this configuration the ZN1044 output drive voltage is a maximum since the total output swing would be V_{RMin} - $V_{O(LO)\ Max}$ = 4.3V for a current of 25mA. Negative firing triac circuits therefore enable triacs of greater power to be driven directly from the ZN1044 outputs than would be the case for positive firing circuits.

2.5.5 Output state indication

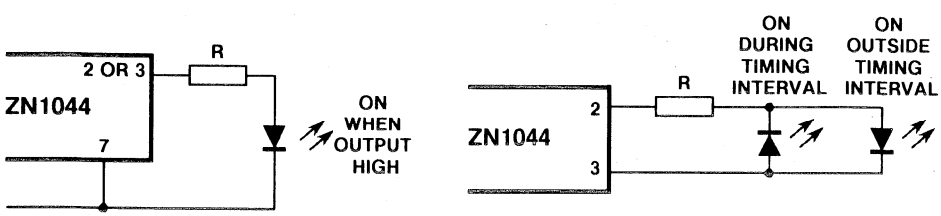


Fig. 16

The value of R is chosen to limit the current to the LED requirements. When mains supplies are used the extra power in the dropper resistor may make the use of neon indicators across the load preferable to LEDs.

SECTION 3 POWER SUPPLIES AND REFERENCES

3.1 Externally regulated supplies

If a 5V ± 10% supply rail is available then the internal shunt regulator is not necessary and by leaving pin 5 unconnected the minimum current drain of 2mA required is avoided. The current available from the supply should not fall below a level of:

$$I_{cc} = (5mA + \text{the output current from Pins 2 or 3})$$

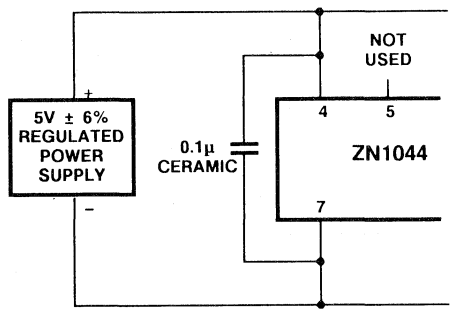


Fig. 17

N.B. The supply should be decoupled by 0.1µF capacitor connected as close as possible to Pins 4 and 7.

3.2 Internally regulated supplies

3.2.1 d.c. supplies greater than 5 volts

By connecting pin 5 to pin 4 an on-chip shunt regulator allows the use of unregulated d.c. supplies higher than 5 volts. To illustrate the use of the shunt regulator a supply circuit design for operation with a typical process equipment supply of +24V and ±25% is shown below.

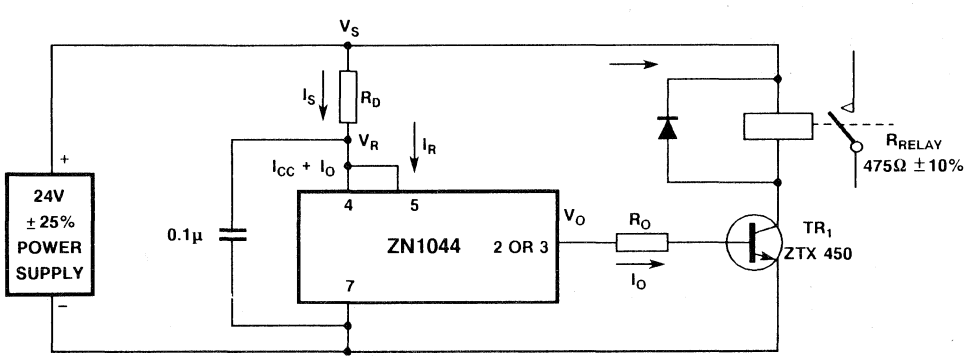


Fig. 18

N.B. The supply decoupling capacitor also acts as stabilisation for the internal regulator and the connection between pins 5 and 4 should therefore be as short as possible.

The values of R_O and R_D used in the circuit of Fig. 18 are calculated as follows. For R_O we need $I_{O(Min)}$, the minimum current required into the base of T_1 for worst case conditions.

$$I_{O(Min)} = I_{B(Max)}$$

$$= \frac{1}{h_{FE(Min)}} \times \frac{24(+25\%)}{475(-10\%)}$$

$$= \frac{1}{50} \cdot \frac{30}{427}$$

$$\mathbf{I_{O(Min)}} = \mathbf{1.4mA}$$

Deriving $V_{O(Min)}$ for the output circuit (Fig. 11)

$$V_{O(Min)} = V_{R(Min)} - 2 \times (\text{Internal } V_{BE})$$

$$= 4.7 - 1.4$$

$$\mathbf{V_{O(Min)}} = \mathbf{3.3 \text{ volts}}$$

Hence $$R_O = \frac{3.3 - V_{BE\,T_1}}{1.4}\ k\Omega \quad (V_{BE\,T_1} = 0.6V)$$

$$= 1.9k$$

Choose $\mathbf{R_O}$ = **1.8k** (Nearest lower preferred value)

To calculate R_D we need $V_{O(Max)}$ and $I_{S(Min)}$

As above $$V_{O(Max)} = V_{R(Max)} - 2 \times (\text{Internal } V_{BE})$$

$$= 5.3 - 1.4V$$

$$\mathbf{V_{O(Max)}} = \mathbf{3.9 \text{ volts}}$$

and with the value of R_O chosen the actual current is

$$I_{O(Max)} = \frac{3.9 - V_{BE\,T_1}}{1.8} = 1.8mA$$

From which the minimum allowable supply current can be obtained

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)}$$

$$= 5 + 1 + 1.8$$

$$\mathbf{I_{S(Min)}} = \mathbf{8.8mA}$$

Hence $$R_D = \frac{V_{S(Min)} - V_{R(Max)}}{I_{S(Min)}}$$

$$= \frac{18 - 5.3}{8.8}\ k$$

$$\mathbf{R_D} = \mathbf{1.5k}\ \text{(Nearest preferred value)}$$

The power dissipated in the dropping resistor and the ZN1044 can be obtained also from

$$I_{S(Max)} = \frac{V_{S(Max)} - V_{R(Min)}}{1.5k(-5\%)}$$

$$= \frac{30 - 4.7}{1.425} \text{ mA}$$

$$\mathbf{I_{S(Max)} = 18mA}$$

Hence the ZN 1044 dissipation = 90mW max. and power dissipation by dropping resistor = 450mW max.

The calculations assume ±2% tolerance resistors.

3.2.2 a.c. mains supplies

A transformer may be used to drop the voltage from the mains and a rectified d.c. supply provided as discussed in 3.2.1

However the on-chip shunt regulator makes the transformer unnecessary since the supply may be obtained directly from the mains or from any other source of a.c. or d.c. higher than 5 volts. With a load such as the directly driven triac (sections 2.5.3 and 2.5.4) a half wave rectifier is used since either the line or neutral has a connection common to the load circuit and the I.C. supply thus preventing the use of a bridge rectifier.

The calculation of the smoothing and voltage dropping components is described below.

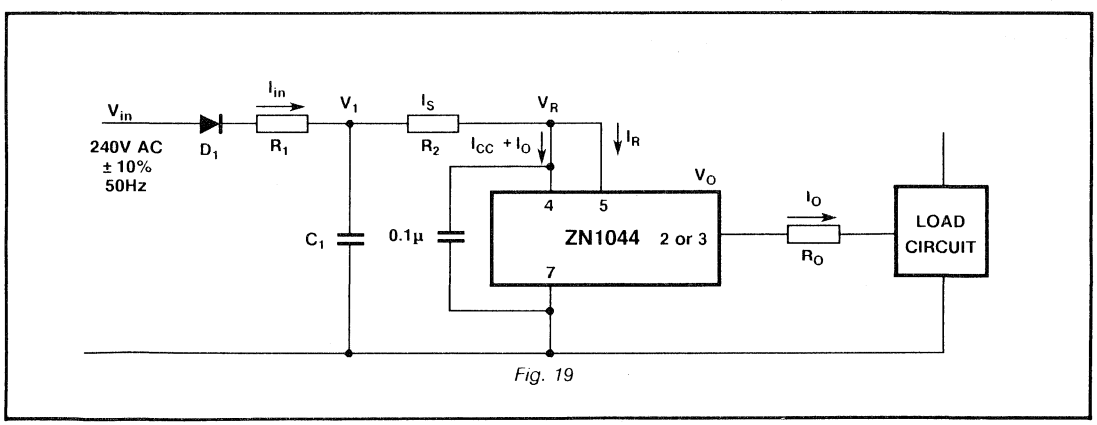


Fig. 19

The value of R_O and $I_{O(Max)}$ are calculated as in 3.2.1 and as an example a current $I_{O(Min)}$ of 10mA is assumed (the gate current for a 0.35A Triac, RS 202).

Therefore

$$\mathbf{V_{O(Min)} = 3.3V}$$

$$R_O = \frac{3.3 - V_G}{10.10^{-3}} \Omega \quad (V_G T_1 = 2V \text{ for RS 202})$$

$$\mathbf{R_O = 120\Omega} \text{ (Nearest lower preferred value)}$$

$$\mathbf{V_{O(Max)} = 3.9V}$$

Hence

$$I_{O(Max)} = \frac{3.9 - V_G}{0.12} \text{ mA}$$

$$\mathbf{I_{O(Max)} = 16mA}$$

And the minimum value of supply current for correct operation is therefore

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)}$$
$$= 5 + 2 + 16$$
$$\mathbf{I_{S(Min)} = 23mA}$$

If we assume that C1 is a 25 volt working capacitor and that 3 volts peak to peak ripple is allowable then the highest value for $V_{1(Min)}$ will be

$$V_{1(Min)} = 25(-20\%) - 3 \text{ (Allowing for } \pm 10\% \text{ variation in mains supply)}$$
$$\mathbf{V_{1(Min)} = 17V}$$

Therefore
$$R_2 = \frac{17 - V_{R(Max)}}{23}\ k\Omega$$
$$\mathbf{R_2 = 510\Omega} \text{ (Nearest preferred value)}$$

The current i_{in} will flow for very nearly the full half cycle, 10ms in the case of 50Hz supplies, since V_1 is low compared to the peak mains voltage.

Now
$$i_{in(avg)} = \frac{V_{in(pk)} - V_{1(avg)}}{\pi R_1}$$

and this current from the rectifier must be equal to the current into the timer circuit.

$$i_{in(avg)} = I_{S(avg)}$$

and the average value of this current is

$$I_{S(avg)} = \frac{V_{1(Min)} + V_{RIPPLE(avg)} - V_{R(Min)}}{R_2}$$
$$= \frac{17 + 1.5 - 4.7}{510}$$
$$= 27mA$$

Therefore
$$R_1 = \frac{\sqrt{2} \times 240\ (-10\%) - (17 + 1.5)}{\pi \times 27}\ k\Omega$$
$$= \mathbf{3k3} \text{ (Nearest preferred value)}$$

For the required ripple of 3V pk.pk. we can obtain

$$C_1 = \frac{I_{S(avg)} \times 10ms}{3}$$
$$C_1 = \frac{27 \times 10^{-5}}{3}$$
$$\mathbf{C_1 = 100\mu F} \text{ (Nearest higher preferred value)}$$

In order to calculate the maximum power dissipation in the dropping resistor we need to know $i_{in(avg)}$ for the upper limit of mains voltage.

Maximum value of $$i_{in(avg)} = \frac{V_{in(pk)(Max)} - V_{1(Max)}}{\pi R_1}$$

$$= \frac{2 \times 240\ (+10\%) - 20}{h \times 3.3 \times 10^3}$$

$$\textbf{Max. } i_{in(avg)} = \textbf{34mA}$$

and Max dissipation in R_1 $$= \frac{\pi^2}{4} \times i_{in}{}^2{}_{(avg)} \times R_1$$

$$P_{R1} = \textbf{9.4 watts}$$

When a d.c. load such as the thyristor relay driver of section 2.4.2 is required then a full wave bridge circuit can be used as shown below.

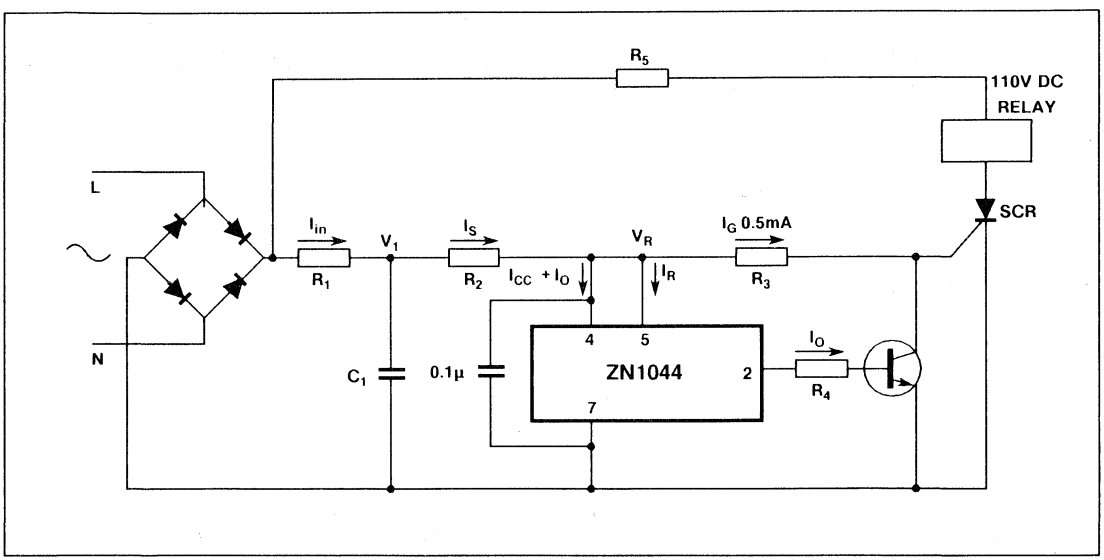


Fig. 20

The DELAY-TO-OFF timer circuit of Fig. 13 has been taken as an example. A typical circuit might have the relay resistance equal to $R_5 = 10k$ and for a 240V ± 10% mains supply the SCR could be a BRX49 which requires less than 0.5mA on gate current. To ensure gate turn-off a ZTX450 transistor with a base current of 0.5mA is sufficient with the above load.

Hence $$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)} + I_G$$

$$= 5 + 2 + 0.5 + 0.5$$

$$I_{S(Min)} = \textbf{8mA}$$

Choosing C_1 to be 25 volts working and 3 volts peak to peak ripple as in the previous example. Then

$$V_{1(Min)} = 25\ (-20\%) - 3$$

$$= \textbf{17 volts}$$

And $$R_2 = \frac{17 - V_{R(Max)}}{8}\ K\Omega$$

$$= \textbf{1.5k} \text{ (Nearest preferred value)}$$

To find the value of C_1 required estimate the angle of conduction. Thus for a sine wave input conduction with change when the voltage on the smoothing capacitor is equal to the instantaneous value of the input voltage less the rectifier voltage drop.

So $V_1 + 1.2 = V_{in(pk)} \text{ Sin } \theta$

and for small values $\theta = \text{Sin } \theta$

Hence $\theta = \dfrac{V_1 + 1.2}{V_{in(pk)}}$

(assuming 1.2 volt drop across the briage rectifier).

for the rising sine wave $\theta_r = \dfrac{V_{1(Min)} + 1.2}{V_{in(pk)}}$

and for the falling sine wave $\theta_f = \dfrac{V_{1(Max)} + 1.2}{V_{in(pk)}}$

$$\theta_{tot} = \frac{V_{1(Min)} + V_{1(Max)} + 2.4}{V_{in(pk)}}$$

$$= \frac{\mathbf{17 + 20 + 2.4}}{305}$$ (Taking lowest mains input as worst case).

$$= 0.13 \text{ radian}$$

The angle of non conduction $\theta_{tot} \simeq 8°$ and the capacitance will discharge by 3 volts in this period which in terms of time is

$$t = \frac{8}{180°} \times 10\text{ms (for 50Hz mains)}$$

$$= 0.44\text{ms}$$

and since $C \simeq \dfrac{\Delta t}{\Delta V} \cdot I_{S(Max)}$ $\quad (I_{S(Max)} \simeq I_{S(Min)} + 20\%)$

$$\simeq \frac{44 \times 10^{-5}}{3} \times 8 \times 10^{-3} \ (+20\%)$$

$$\simeq 1.4\mu F$$

So we can choose a $2.2\mu F$ of 25 volt working or higher for C_1.

The mains dropping resistor can be simply obtained with sufficient accuracy by assuming 100% conduction. Thus

$$R_1 = \frac{2}{\pi} \times \frac{V_{in(pk)} - V_{1(Max)}}{I_{S(Min)}}$$

$$= \frac{2 \times 305\ 1\ 20}{\pi \times 8 \times 10^{-3}}$$

(Lowest mains voltage gives worst case).

$$\simeq 22\text{k (Next lowest preferred value)}$$

In order to calculate the power dissipated by the dropping resistor P_{R1} we need to know $i_{in(avg)}$ for the higher limit of the supply.

Maximum value of

$$i_{in(avg)} \simeq \frac{2\,(V_{in\ (pk)\ (Max)} - V_{1(Max)})}{\pi\, R_1}$$

$$= \frac{2}{\pi}\left(\frac{2 \times 240\ (+10\%) - 20}{22 \times 10^{-3}}\right)$$

$$i_{in(avg)} = \mathbf{10mA}$$

Hence

$$P_{R1} = \frac{\pi^2}{8} \times \mathbf{10^{-4}} \times \mathbf{22} \times \mathbf{10^3}$$

$$P_{R1} = \mathbf{2.7\ watts}$$

The calculations have been performed using the 235V ± 10% 50Hz mains figures. Similar calculations may be done for 110V 60Hz or whatever supplies are available.

Note 3.3 Reference supply

The 2.6V reference on pin 16 may be used for an external reference other than for the timing components.

SECTION 4 INTERFERENCE SUPPRESSION

Two types of interference, mains borne and electromagnetically radiated interference, can affect the operation of the timing circuit. In environments where such noise is encountered steps should be taken to reduce its effect on the timing circuit and the following notes should enable the circuit designer to avoid interference problems. The points discussed are illustrated by referring to a mains delay-to-on, and timer design illustrated in Figs. 21 and 22.

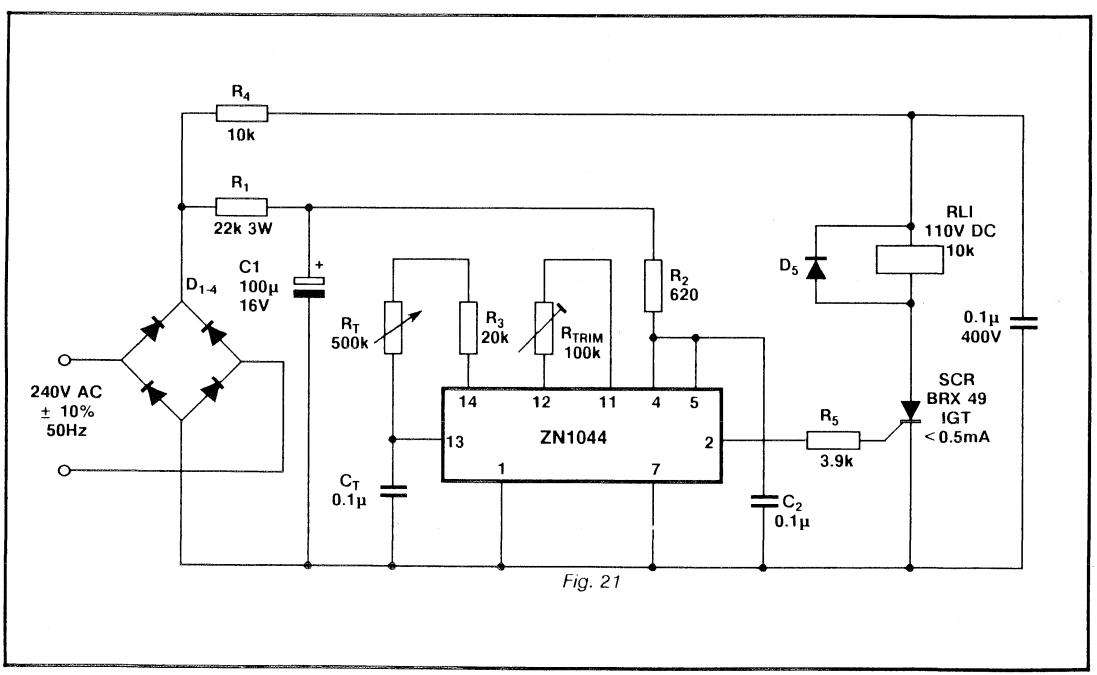


Fig. 21

If the supply is reduced below (typically) 3.5V at any time, even for less than a microsecond then the logic and counter section of the ZN1044 will be reset and restoration of the normal supply may result in the initiation of a new timing period regardless of the initiation state. The effects of pulses on the supply are described in operating note 2.1.

Positive spikes are effective only when they produce a negative overshoot large enough to cause reset.

Negative spikes can be reduced by using a full diode bridge circuit, as in Fig. 21 which rectifies the spikes as well as the a.c. supply, or a half bridge where an a.c. load is being driven and the timer ground cannot be separated from neutral. The dropping resistor R_1, with C_1, forms a low pass filter for mains smoothing and additional filtration is provided by R_2 and C_2. These filters will also attenuate noise spikes. The shunt regulator in conjunction with the dropping resistors R_1 and R_2 provides considerable spike attenuation as well as d.c. regulation. The circuit of Fig. 21 for example, has an attenuation of supply spikes of 15000:1 due to the regulator alone. When a 5V supply designed for TTL, or similar requirements is available and the shunt regulator is not connected, protection against interference is not usually necessary since the supply itself should be capable of suppressing mains borne interference. If a transformer is used to isolate the timer from the mains then the voltage drop can be divided between the transformer and the series resistor. The greater the series resistance then the greater the attenuation of noise by the shunt regulator and the smoothing capacitor. A transformer drop to 24V d.c. is a useful compromise allowing the use of 24V relays. The transformer itself will attenuate high frequency spikes. The greater the series resistance then the greater the attenuation of smoothing capacitor. A transformer drop of 24V d.c. is a useful compromise allowing the use of 24V relays. The transformer itself will attenuate high frequency spikes.

Note 4.2. Electromagnetically induced noise

The ZN 1044 oscillator frequency is determined by the time taken to change C_T via R_T from about 1.6 to 2.2V on Pin 13. A single interference pulse of 0.1V on this pin could cause an error on a single time constant of 20% but since the timing period of a ZN1044 timer is made up of 4095 RC charging times then a larger number of interference pulses in a timing period would be required to cause such a timing error. Where such interference exists, and bearing in mind that for a constant rate of interference pulses the effect becomes greater for increasing length of time period, steps should be taken to screen Pin 13 from electro-magnetically induced noise.

Any leads connected to Pin 13 are susceptable to interference pick-up and should be screened.

When the ZN 1044 oscillator frequency is near to that of the mains supply, or tolow harmonics, care should be taken in the layout of the circuitry and in the position of components such as mains transformers to obviate this effect. Stray coupling of mains frequencies can have the effect of locking the oscillator to that frequency and producing a band over which variation in timing components will not cause a corresponding variation in timing period.

Section 8

Application Notes

Satellite Receiver Design

The start-up phase of engineering developments is often characterised by a multiplicity of opinions and solutions to the problem, adding great interest but not a little confusion to the subject. In the course of time the situation clarifies with one or two solutions gradually gaining wide acceptance due to their simplicity and cost effective nature. Such is the situation in the satellite receiver market at the present time, where standards are few and far between with even transmission characteristics differing from one broadcast company to another, but with a trend towards a more standard receiver emerging.

In order to simplify the situation, only the single conversion and block conversion systems will be discussed here although much of the applications information and most of the products will be appropriate to other situations.

SINGLE CONVERSION RECEIVERS

The simplest form of receiver is probably the single conversion type shown in Fig.1. Here, the incoming signal is amplified and mixed with the local oscillator signal to produce a lower intermediate frequency in a similar manner to a conventional TV. Unfortunately both the amplifying and mixing processes have to be performed close to the dish, the first due to noise considerations, the second because it is not economic to transmit the high frequencies used in satellite reception via a relatively long coaxial cable.

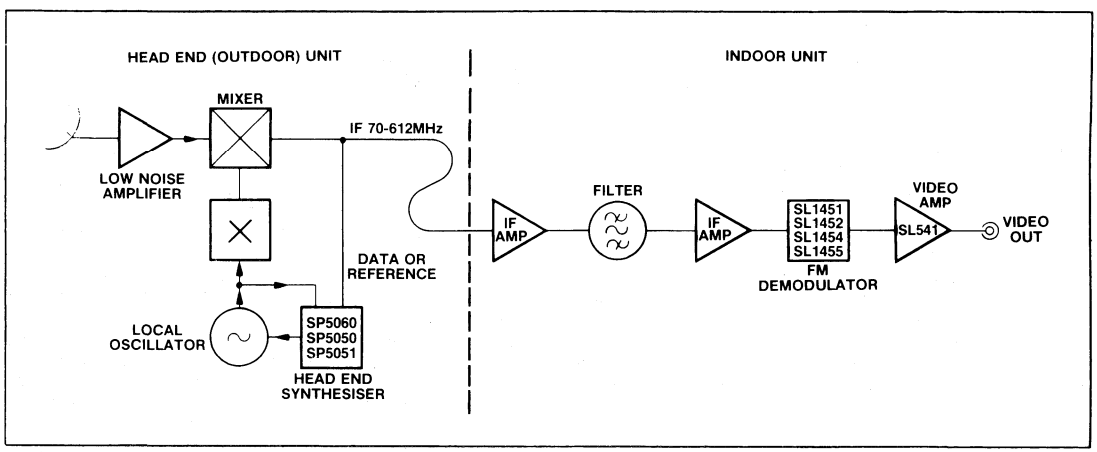


Fig.1 Simplified block diagram of single conversion receiver

The intermediate frequency is received by the indoor unit where an IF filter passes only the required signal to the FM demodulator. The choice of this intermediate frequency is one of the main areas of disagreement between designers, some using the existing 70MHz standard used in microwave link communications, but others adopting various higher frequencies up to 612MHz, making use of the low cost demodulators, SAW filters and amplifiers becoming available for these frequencies.

Now that the high cost objections to high IF usage have been overcome, other technical advantages, such as greater demodulator linearity (due to the lower percentage deviation) and simpler receiver design (because the inherently higher image rejection makes tracking filters unnecessary), will eventually ensure the universal adoption of high intermediate frequencies.

Design of single conversion receivers is complicated to some degree because programme selection is determined at the head end, requiring in the simplest case of a non-synthesised receiver, a variable DC tuning voltage to be passed from the indoor to outdoor units.

This will probably require an additional cable, because the DC power supply for the head end unit will already be carried by the signal coax. Where synthesised tuning is required the situation is additionally complicated as digital tuning information or a variable frequency reference must be transferred to the head end. Because the programme selection is determined at the receiver head end, the single conversion receiver has the disadvantage that reception of only one signal is possible from a dish, removing the possibility of watching alternative programmes in different rooms of a house and making the system unsuitable for feeding apartment blocks or hotels.

BLOCK CONVERSION RECEIVER

The block converter type of receiver shown in Fig.2 overcomes most of the disadvantages of the single conversion type by using a fixed frequency local oscillator at the head end. By this method all the available signals in the satellite band sharing the same polarisation are down-converted to an intermediate frequency usually ranging from 950MHz to 1450MHz or 1750MHz for transmission to the indoor unit. this technique transfers programme selection to the indoor unit and so removes the need for data or reference transmission to the head end. The technique also allows connection of several receiver units tuned to different signals and provides good image rejection due to the use of a relatively high IF. Programme selection is obtained by further down-converting the required signal to a fixed second IF using a voltage controlled local oscillator. A SAW filter or other type of bandpass filter is used at this point to reject unwanted signals. The choice of second IF is flexible as in the case of the single conversion receiver, with the same arguments causing a trend towards the use of higher frequencies.

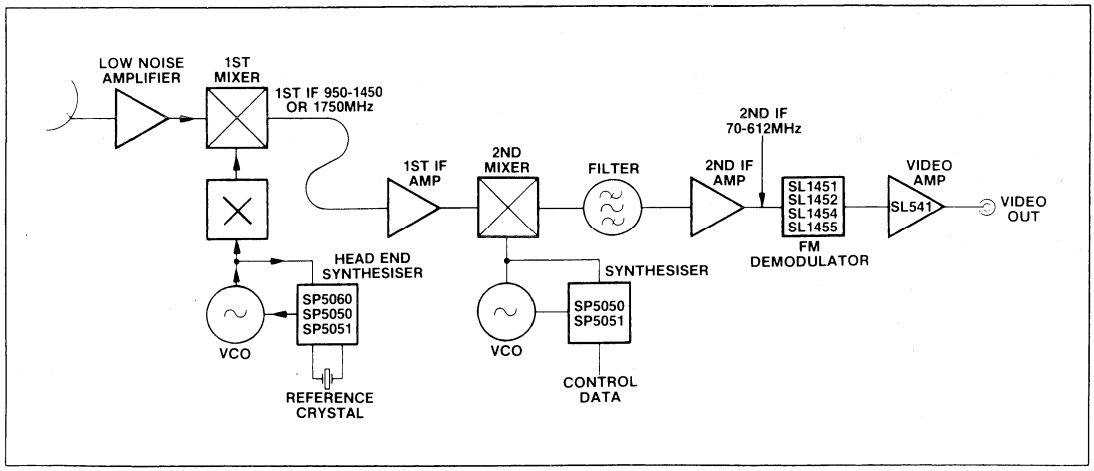


Fig.2 Simplified block diagram of block conversion satellite receiver

SIGNAL TO NOISE THRESHOLD

In a frequency modulated system, as used in satellite TV reception, the demodulated signal to noise ratio decreases linearly with decreasing carrier to noise ratio before demodulation, until a level known as the threshold point is reached. Below the threshold point, the output signal to noise ratio decreases rapidly, producing short duration high amplitude impulses which in the context of TV reception manifest themselves as light or dark spots on the picture commonly known as 'sparklies'. The threshold is defined as that point where the output signal to noise ratio departs by 1dB from the straight line relationship with the input carrier to noise ratio.

THRESHOLD EXTENSION

In an ideal world, the best method of obtaining a perfect picture at all times would be to ensure a good carrier to noise ratio under all reception conditions by using an adequate receiving dish, but in urban situations or in fringe areas, the size of dish required might be unacceptable and some method of extending the threshold point of the detector is desirable.

Although in many cases some form of threshold extension will be found necessary to achieve the required receiver performance, it should be noted that (as is often the case in engineering) improved performance in one direction means a compromise in another. Threshold-extended FM demodulators are no exception, and unless carefully designed, problems such as picture tearing on fast black to white transitions can occur. Although threshold extension techniques can successfully delay the onset of sparklies, under poor carrier to noise ratio conditions the effect **will** occur, generally producing noise pulses of longer duration than those from an unextended demodulator such as the SL1452.

Frequency Synthesiser Applications

SP5060 2GHz FREQUENCY SYNTHESISER

In the block converter type of receiver shown in Fig.2, the local oscillator signal to the first mixer is a fixed frequency and is often controlled by a dielectric stabiliser. A more stable control of frequency may be obtained by using a phase locked loop synthesiser with crystal reference, such as the SP5050 or SP5051. Although either of these products could be used in such an application, the need for a 16-bit input word to select the operating frequency is a disadvantage when the device is situated at the remote end of the receiver downlead. Local generation of the necessary data word using CMOS logic elements or sending a suitably coded data word along the downlead are possible solutions to the problem, but it may be simpler to use the SP5060 fixed frequency synthesiser. The SP5060 can synthesise any frequency in the range 300MHz to 2.0GHz when fed with the appropriate reference.

The C-band satellite signals cover the range from about 3.67 to 4.17GHz and using a frequency doubling mixer with low side oscillator injection, down conversion to the 950-1450MHz standard IF range will occur if the oscillator frequency is set at 1.36GHz. Since the multiplication ratio between the local oscillator and the reference input to the SP5060 is 256, a 5.3125MHz crystal reference will be required, as shown in Fig.3. A similar system but with a much greater degree of local oscillator multiplication could be used in a block down converter for 12GHz DBS reception.

The SP5060 can also be used for head end tuning in single conversion receivers by feeding a variable reference frequency along the downlead from the indoor unit. Since the reference is at a very different frequency from the IF the two can be easily separated with a minimum of filtering.

The variable reference frequency for this type of system is best generated using a low frequency synthesiser contained in the indoor unit, and a system using the Plessey NJ8820 is shown in Figs. 4 and 5.

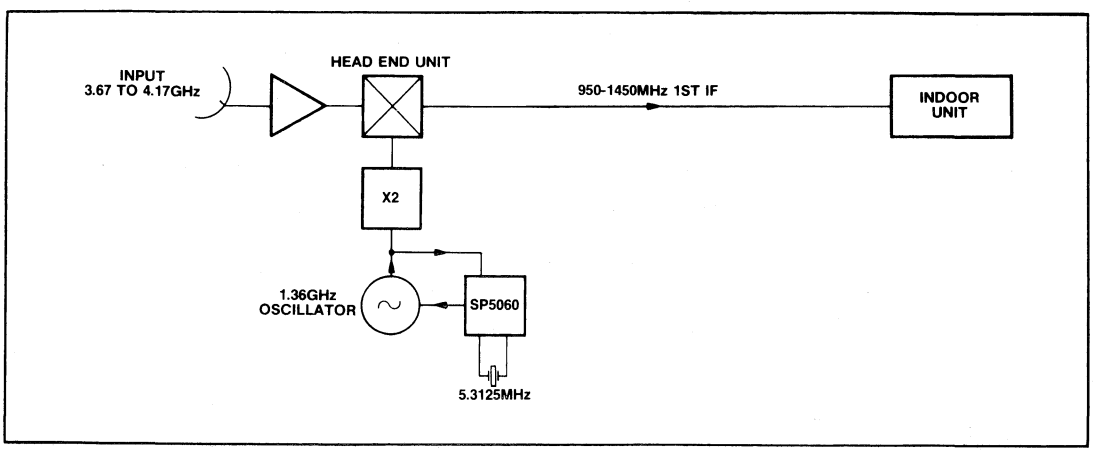


Fig.3 Synthesised block down converter system

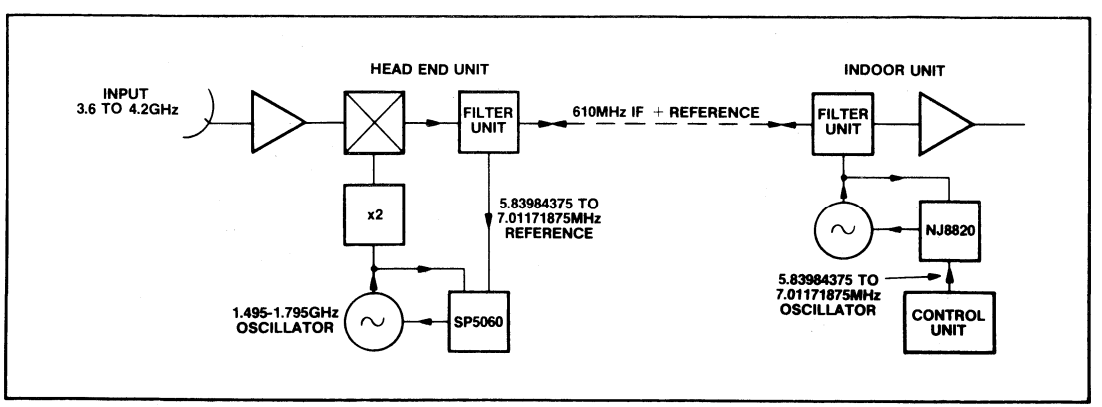


Fig.4 Block diagram of synthesised single conversion receiver

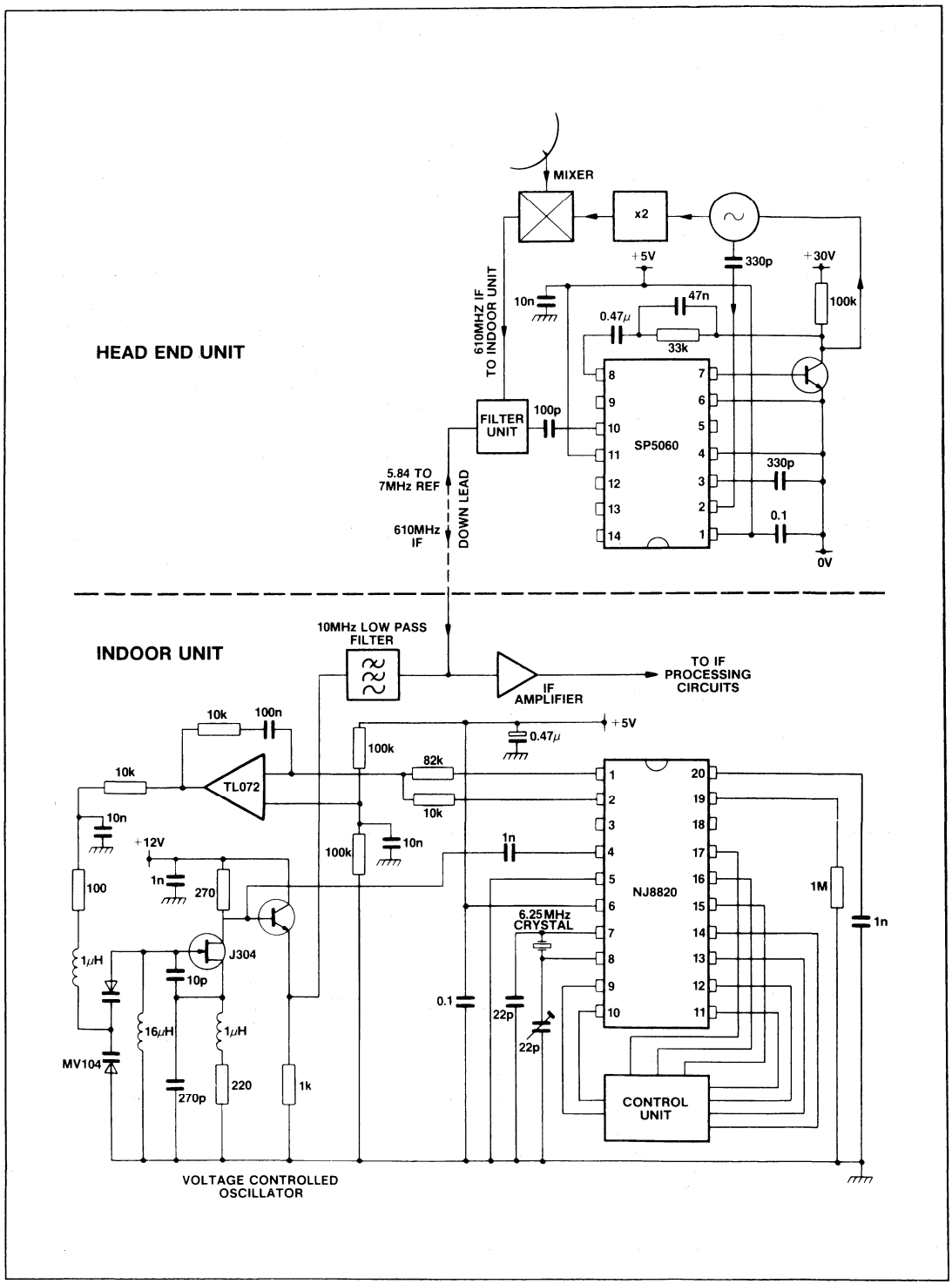


Fig.5 Circuit of double synthesiser

Using a frequency doubling mixer or x2 multiplier and assuming a 3.6 to 4.2GHz tuning requirement, 610MHz IF and a low side local oscillator, the required oscillator frequency range will be 1.495 to 1.795GHz.

The ratio of reference frequency to synthesised frequency of the SP5060 is 256, giving a reference requirement to be produced by the NJ8820 of 5.83984375 to 7.01171875MHz. Similarly, if the step size at the mixer is set at 10MHz the reference step becomes 19.53125kHz.

Although these numbers are beginning to look somewhat formidable, the NJ8820 is capable of producing the required output if a 6.25MHz reference crystal is used with the reference counter programmed to divide by 160, or 320 including the fixed divide by 2. Frequency adjustment to anywhere in the required range can now be obtained by setting the ratio of the N counter in the NJ8820 as follows:

$$\text{Step size of NJ8820} = \frac{\text{crystal reference frequency}}{160 \times 2}$$

$$= \frac{6.25\text{MHz}}{320}$$

$$= 19.53125\text{kHz}$$

Programming input for reference counter

$$= \text{binary } 160$$

$$= 00010100000$$

To tune a minimum frequency of 5.83984375MHz (for a mixer LO input of 2.99GHz) requires input to the NJ8820 N counter of:

$$\frac{5.83984375\text{MHz}}{19.53125\text{kHz}} = 299$$

$$= 0100101011$$

NOTE: Using this scheme the ratio at the NJ8820 N counter is equal to the local oscillator mixer input frequency in GHz x 100. For example, if the LO input to the mixer is required to be 3.15GHz the ratio will be 315 or binary 0100111011.

The flexible programming ability of the NJ8820 will allow a receiver using this system to be controlled using either a microprocessor or a multi-position switch in conjunction with a PROM as shown in the NJ8820 data sheet.

SP5051 2GHz SYNTHESISER

Block conversion receivers generally produce a first IF ranging from 950MHz to 1450MHz in the case of the US C-band services, and from 950MHz to 1750MHz for the proposed DBS services. Using a high side local oscillator necessary to obtain the required tuning range, and with a European standard 480MHz 2nd IF the required frequency range will be 1430MHz to 2230MHz obtainable by raising the SP5051 reference frequency to about 4.36MHz. Although calculating a suitable reference frequency to just cover the maximum requirement will give the smallest step size and therefore greatest resolution if fine tuning for AFC is used, the step size for any data bit does not coincide with the 19.18MHz standard DBS channel spacing, possibly increasing the complexity of the control software. A better solution might be to increase the reference frequency to 4.795MHz giving a rather curious minimum step size of 0.14984375MHz but producing a 19.18MHz step for the 2^7 data bit.

For a C-band system, a suitable reference frequency might be 5MHz giving a 20MHz step for the 2^7 data bit with a minimum step size of 0.15625MHz and a theoretical maximum synthesised frequency of 2.5598GHz, well above that required for a 612MHz IF.

REMOTE PROGRAMMING OF SP5000 SERIES SYNTHESISERS

Although remote programming of SP5000 series synthesisers appears complex at first sight, with a requirement for Chip Enable and Data Clock signals as well as the frequency data, the task can be greatly simplified using the circuit shown in Fig.6.

Obviously it is most convenient to have only a single downlead between the head end and indoor units of a satellite receiver, and therefore the system shown in Fig.6 sends data along the downlead at a relatively low frequency (125kHz) which can be easily filtered from the IF signal. The data is sent as a burst of 125kHz, representing a '1', and a logic '0' by the absence of signal. The duration of each logic bit is 64 cycles of 125kHz equivalent to a time period of 0.512ms (see Fig.7).

Data Clock and Chip Enable inputs are generated locally from the data input to avoid having to encode these on the overworked downlead, the process being initiated by the leading edge of the first data bit which must always be logic 1. Since the first data bit is used only by the band select or control outputs, this causes no frequency setting limitation and the second bit is still available for use as a polarisation setting control.

Circuit Description (Fig.6)

The 567 phase locked loop tone decoder chip is set to detect the bursts of 125kHz, producing a low output at pin 8 when the input is present. Loop and output filter components are selected to give fast response consistent with reasonable noise performance. As the first bit in the data stream must always be a logic '1', the negative-going edge at pin 8 produced at the beginning of bit 1 is used to trigger the R-S flip-flop formed by two CMOS NAND gates thus initiating the decoding process. Pin 8 also provides the data input to the SP5000 series device whilst the R-S flip-flop provides Chip Enable.

Once the R-S flip-flop is triggered, the output of the 567 oscillator, at or very close to 125kHz (depending on the presence or lack of 125kHz at the input), drives the 4040 counter. After 32 cycles of the 125kHz input data stream the Q6 output on pin 2 goes high providing a data clock signal to the synthesiser in the centre of the 64 cycle data period. Data clock pulses will continue from pin 2 until all 16 data bits are clocked, when the Q10 output on pin 14 goes high resetting the R-S flip-flop and terminating the chip enable signal. The R-S flip-flop also resets the 4040 leaving the system to be retriggered by the next data stream.

A suitably encoded data stream can be generated under program control from a microprocessor or perhaps more easily by gating under program control the divided output from the microprocessor oscillator (often 4MHz, which, when divided by 32 gives 125kHz).

A low pass filter such as that shown in Fig.6 should be inserted between the downlead and data generating logic to prevent harmonics from the logic section interfering with the picture when fine tuning is used. The same filter will also prevent loading of the IF output by the logic.

MICROPROCESSOR CONTROL

Although as shown above there are various down conversion systems applicable to satellite reception, all have a requirement for some form of control system. A microprocessor used in this control function usually gives greatest flexibility allowing decoding of remote control and local keyboard inputs, generation of input data for synthesisers, channel display and a program memory feature using a single component.

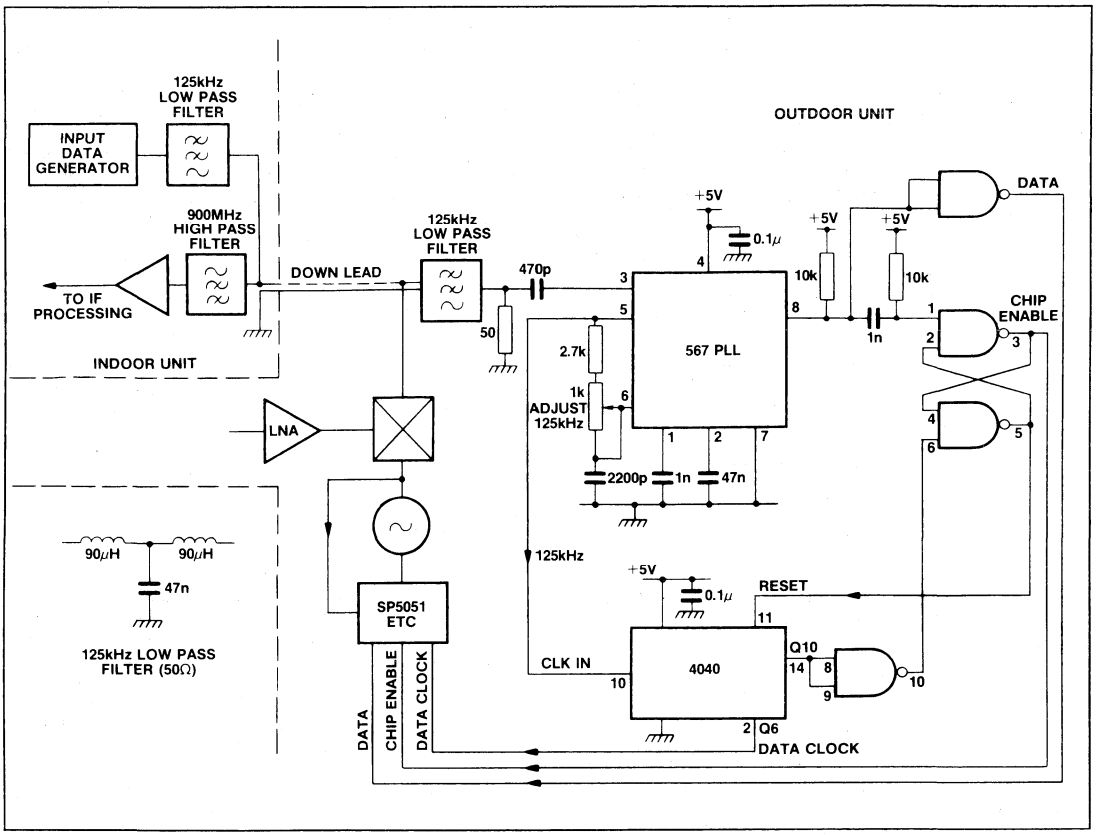


Fig.6 Remote data receiver circuit diagram

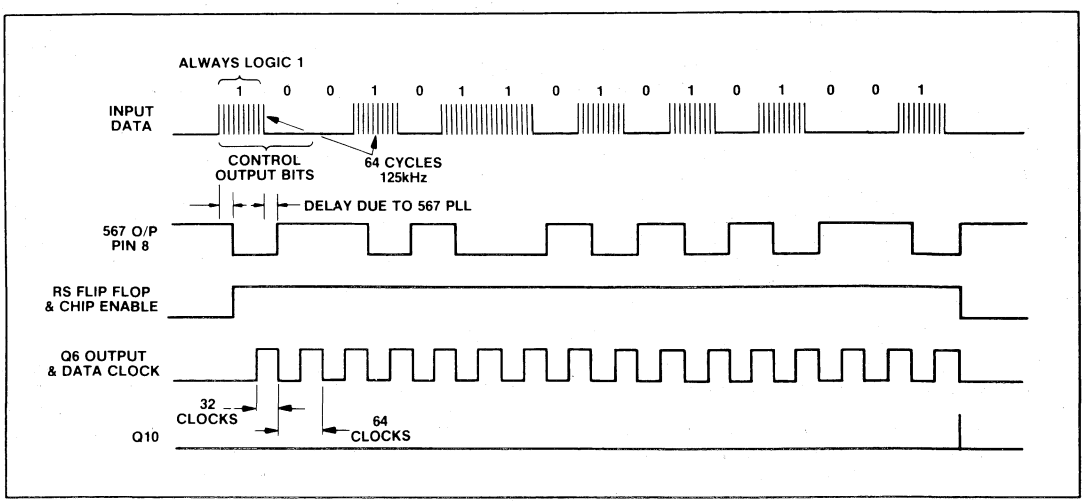


Fig.7 Remote data receiver waveforms

A Low Cost 1.5 to 2.2GHz Voltage Controlled Oscillator

The introduction of the GPS range of 2GHz synthesisers and prescalers for low cost applications such as consumer satellite TV reception has created the requirement for an economic VCO design covering a frequency range from around 1.5GHz to 2.2GHz. Although suitable hybrid oscillator designs are available from various manufacturers, these generally carry a price tag at least an order of magnitude higher than the synthesiser, thus making their use in consumer equipment hopelessly uneconomic.

The design shown in Fig.8 has been developed using low cost components which should be easily available, the varicap diodes being normal UHF TV tuning types and the transistor a standard catalog item.

A major problem when operating at these frequencies is that the series inductance of most capacitors becomes very significant compared with that required in the resonator circuit and also prevents good decoupling. These problems are overcome when designing fixed frequency oscillators by replacing the normal resonant circuits and decoupling capacitors with open or short circuited resonant transmission lines, but a design requiring wide frequency variation must use more conventional techniques.

The transistor is biased to about 15mA using a 22kΩ resistor from collector to base. Any problems with decoupling at the emitter are avoided by connecting the emitter direct to ground. Stabilisation of the bias point relies on the 330Ω collector load resistor providing a degree of feedback. A small inductor in series with the collector load resistor reduces any loading and improves the effectiveness of the +12V supply decoupling. A series tuned circuit consisting of a small inductor and two varicap diodes is connected between collector and base with a 390pF capacitor providing DC isolation of the varicap diodes from the collector voltage. To avoid the introduction of any additional series inductance, the varicap diodes are connected direct to the transistor base without a coupling capacitor. The oscillator frequency is varied by adjusting the varicap bias voltage from 0 to 30V via a 47kΩ isolating resistor. Output amplitude from the basic oscillator is much higher than the input requirements of the synthesiser or prescaler and therefore about 10dB of attenuation is provided by a resistive attenuator.

As might be expected with an oscillator operating at this frequency, layout is fairly critical and the layout shown in Fig.9 should be followed accurately or extensive trials made before any variations are attempted. The prototype oscillators were made on standard 1/16 inch fibreglass board, but it was found impossible to mount the frequency determining components on the board without greatly affecting the frequency range available; these components are therefore mounted off board, relying on short lead lengths to provide sufficient rigidity.

OSCILLATOR SPECIFICATION

Operating voltage : +9V to +14V
Frequency range : 1.5GHz to 2.2GHz
Varicap voltage range : 0V to +30V
Output level : (with 10dB attenuator) -10dBm (70mV)

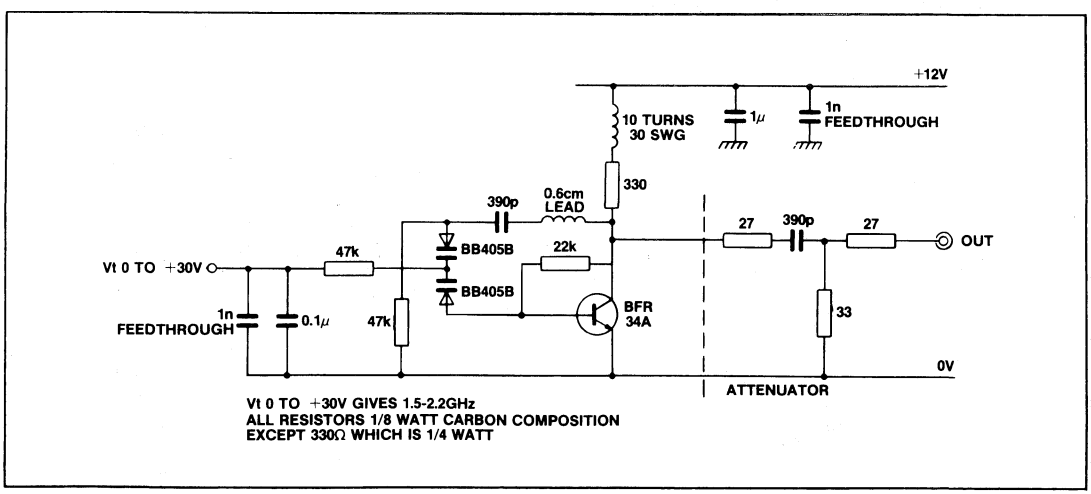
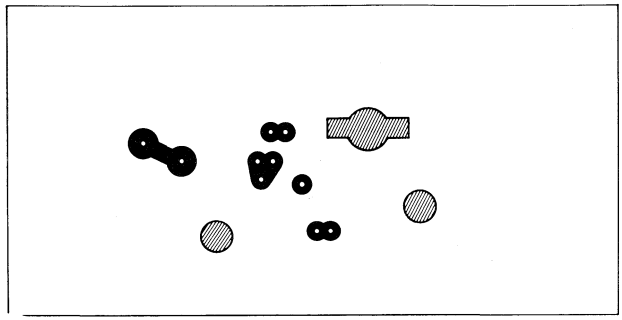
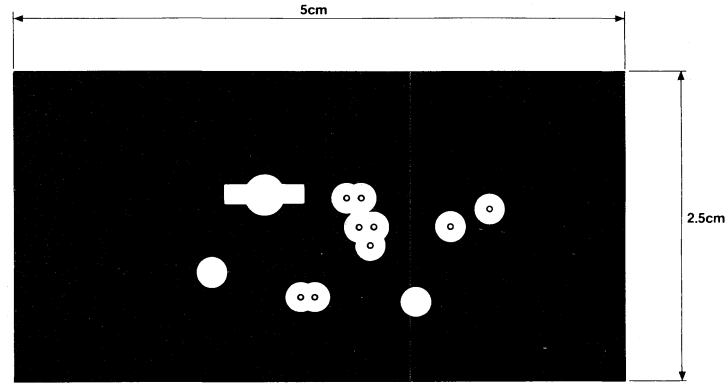


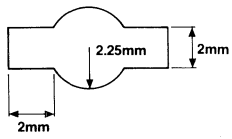
Fig.8 2GHz VCO circut diagram



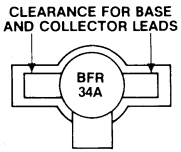
Track side



Ground plane

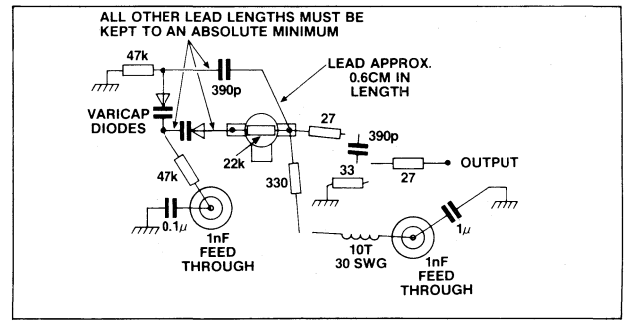


CUT-OUT



EMITTER
LEAD SOLDERED TO GROUND LANE

Transistor mounting details. In order to reduce the transistor lead lengths to a minimum, a hole is cut into the board as shown and the transistor mounted flush on the component side of the board.



Component overlay

Fig.9 Oscillator printed board layout

FM Demodulator Applications

SL1451 THRESHOLD EXTENDED DEMODULATOR

The SL1451 is a Phase locked loop FM demodulator for use at intermediate frequencies in the 400-700MHz range. The chip contains all the necessary building blocks to form a complete demodulator as shown in the simplified block diagram Fig.10.

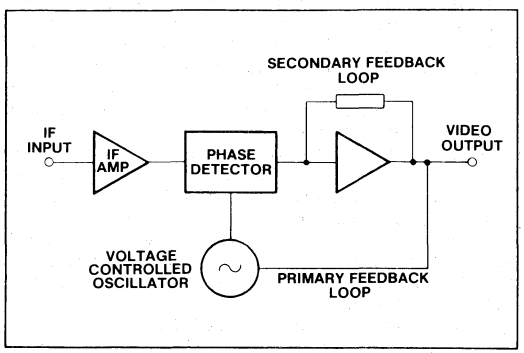


Fig.10 Block diagram of PLL

A 'basic' circuit configuration suitable for demodulating a 612MHz, 13.5MHz peak to peak signal is shown in Fig.11, whilst the circuits in Figs.12-15 are variations tailored to give improved performance under various conditions. These circuit variations will be discussed later.

The on-chip oscillator consists of a single transistor with emitter, base and collector connections bonded out to pins 3, 4 and 5 (see Fig.12). The collector, pin 5, is internally decoupled to ground, preventing the use of oscillator configurations requiring a signal output from the collector. Bias for the transistor is provided by internal resistors.

Using the Clapp variant of the well known Colpitts oscillator, the physical size of inductor required to achieve the operating frequency is increased to acceptable proportions by reducing the effective inductance using a series capacitor, in this case the varicap diode D1. The inductor can take the form of a straight 25mm length of 22 SWG wire separated by about 3mm from the ground plane or 2 turns 22 SWG approximately 4mm in diameter. Tuning to the precise centre frequency is accomplished by bending the straight inductor closer or further from the ground plane or by opening or closing the turns of the coil. In either case, correct tuning is established when the voltage at the video output pin 14 is at 4.5V DC (centre of linear video amplifier range and therefore centre of lock range). Alternatively the 3.9pF capacitor C5 can be replaced by a trimmer to adjust centre frequency.

The oscillator output from the emitter, at an optimum level (-10dBm) for threshold performance, is coupled by C8 to one input of the differential phase detector, the other being decoupled to ground by C10.

Differential outputs from the phase detector are internally connected to the video amplifier, which in turn drives the varicap diode D1 via the RF-blocking filter L1, maintaining phase lock with the RF input signal on pin 11. With the component values shown, the oscillator frequency gradient is approximately 14MHz/Volt giving a 1V video output from a 13.5MHz peak to peak deviation input signal.

The input amplifier is of differential design and is internally connected to the phase detector, this signal input being coupled to pin 11 via C11. A capacitor C6, decouples the other input to ground.

Although the input amplifier is of variable gain, programmable by varying the voltage on pin 10, most applications of the device give best threshold performance when the gain is at maximum. This is ensured by connecting the resistor R6 from pin 10 to VCC.

An AGC detector circuit connected to the RF amplifier output, provides an output at pin 9 which may be used to control the gain of preceding receiver amplifier circuits. The input amplifier has a signal handling range at pin 11 between -25dBm and 0dBm.

All capacitors associated with the oscillator and RF portions of the circuit should be suitable for use at high frequencies. Ceramic chip types are recommended.

Capacitors C1 and C2 connected between the differential inputs and outputs of the video amplifier determine the loop filter response and in Fig.11 are optimised for the DBS standard 13.5MHz peak to peak deviation at a centre frequency of 612MHz.

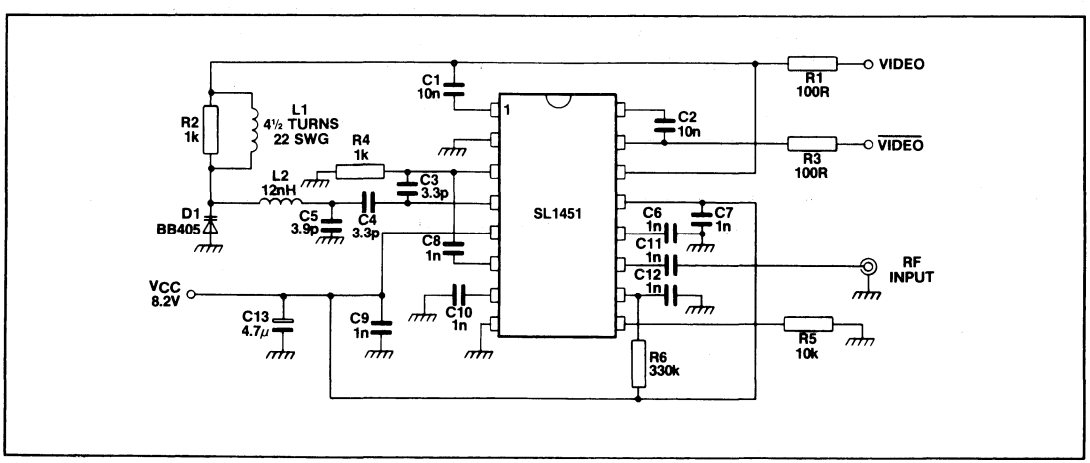


Fig.11 612MHz demodulator 13.5MHz peak to peak deviation

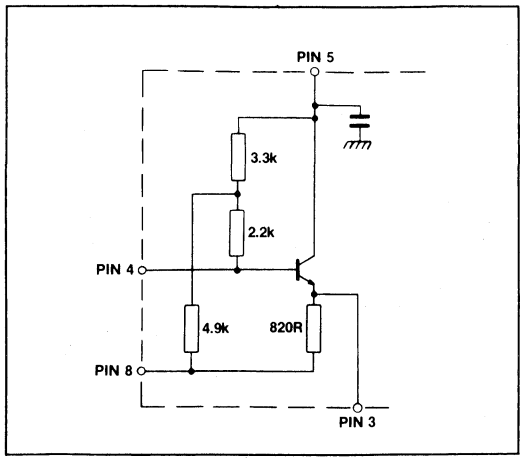


Fig.12 On-chip oscillator circuit

The circuit in Fig.11 has a measured threshold of 8dB and an 18MHz video bandwidth.

Although the circuit shown in Fig.11 gives optimum threshold performance for signals with peak to peak deviations up to about 15MHz, for wider deviation signals the loop filter components must be changed to prevent picture tearing on fast black to white transitions. The loop filter changes have a slight detrimental effect on the obtainable threshold.

For slightly wider deviation signals from about 15 to 20MHz peak to peak it is only necessary to reduce the feedback capacitors C1 and C2 from 10nF to 330pF giving a noise threshold of 8.5dB.

Signals with deviations greater than 20MHz can be accommodated by changing the video amplifier to a single sided configuration by decoupling one input and output (pins 15 and 16) as shown in Fig.13. A 330pF loop filter capacitor is connected between the active input and output pins. This circuit also exhibits an 8.5dB noise threshold.

When the signal to noise ratio at the input of the demodulator approaches the noise threshold point, sparklies (noise spikes), primarily occur in the saturated colour areas of the video. This effect can be reduced by increasing the open loop gain of the PLL at the chroma subcarrier frequency. A parallel tuned circuit (tuned to the chroma frequency) incorporated in the secondary feedback loop will increase the gain of the video amplifier at the chroma frequency and hence increase the open loop gain. For example, for a PAL system (f = 4.433MHz) a parallel tuned circuit comprising a 270pF capacitor and 4.77μH inductor in series with the standard feedback component in Fig.13 will improve the chorma performance. The Q of this tuned circuit must be greater than 10. A complete circuit diagram incorporating this modification is shown in Fig.14.

All the circuits shown so far have a 612MHz oscillator, but when required, it is relatively easy to modify the design for use at other frequencies. Fig.15 shows a design for 480MHz signals of 26MHz peak to peak deviation.

Due to the high operating frequency of the SL1451, particularly the oscillator and input amplifier circuits, care is needed in layout and component selection. A board layout for the circuit configuration with chroma trap (Fig.14) is shown in Fig.16.

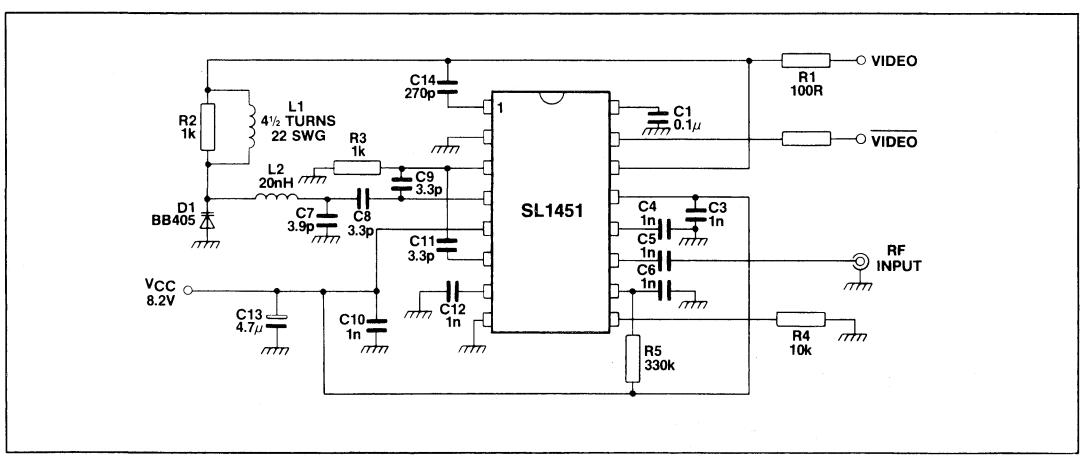


Fig.13 612MHz demodulator for up to 28MHz peak to peak deviation

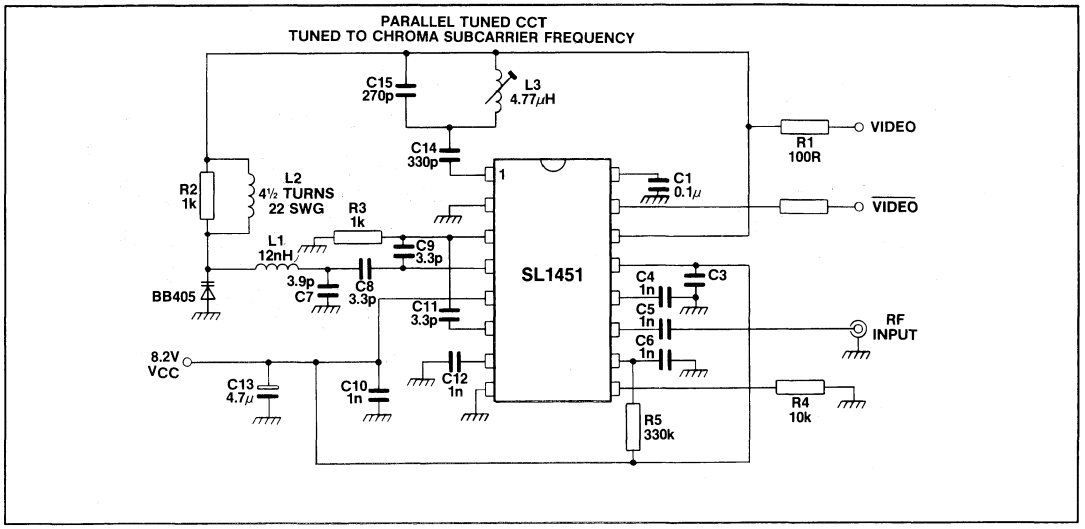


Fig.14 612MHz demodulator for up to 28MHz peak to peak deviation with improved chroma response (recommended PC board layout is given in Fig.16)

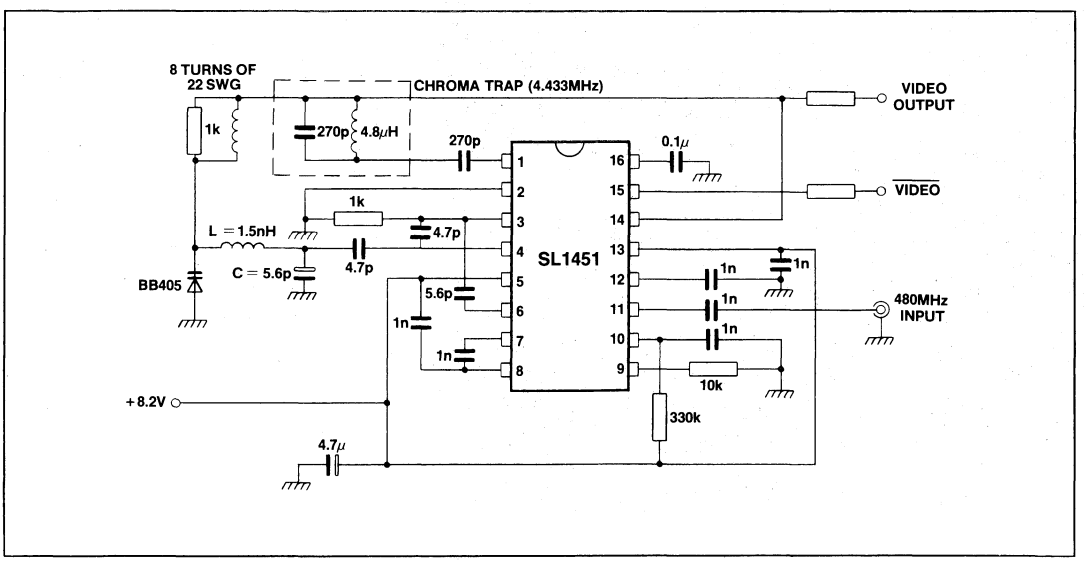
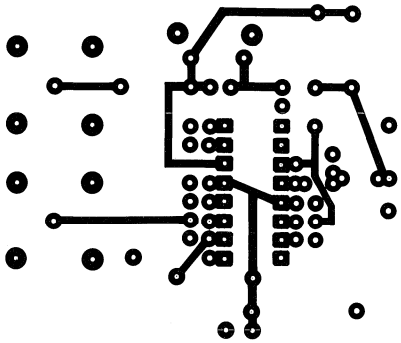
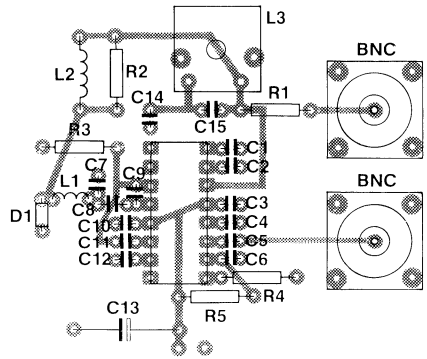


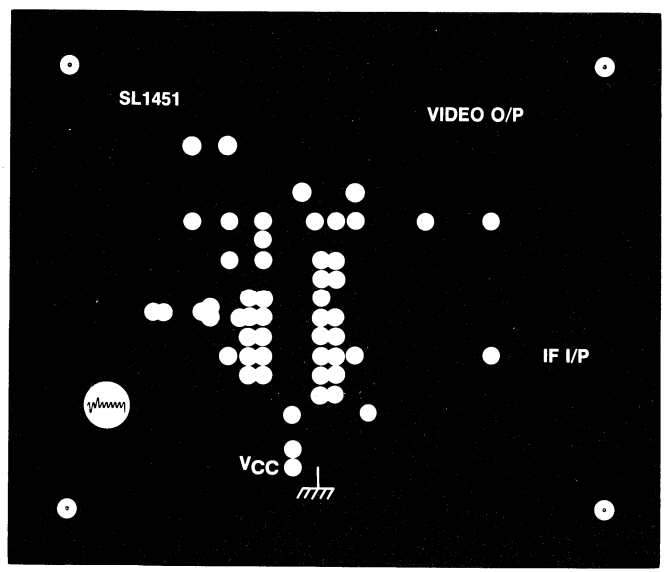
Fig.15 480MHz demodulator for up to 26MHz peak to peak deviation



Track side



Component overlay



Ground plane

COMPONENTS			
R1	100Ω	C1	0.1μF
R2	1k	C2	0.1μF
R3	1k	C3	1n
R4	10k	C4	1n
R5	330k	C5	1n
		C6	1n
L1	12nH	C7	3.9p
L2	4½ TURNS 22 SWG	C8	3.3p
L3	4.6μH TUNABLE	C9	3.3p
	TO CHROMA	C10	1n
	FREQUENCY	C11	3.3p
		C12	1n
D1	BB405	C13	4.7μ
		C14	330p
		C15	270p

Fig.16 SL1451 612MHz FM demodulator demonstration board with chroma trap (circuit shown in Fig.14)

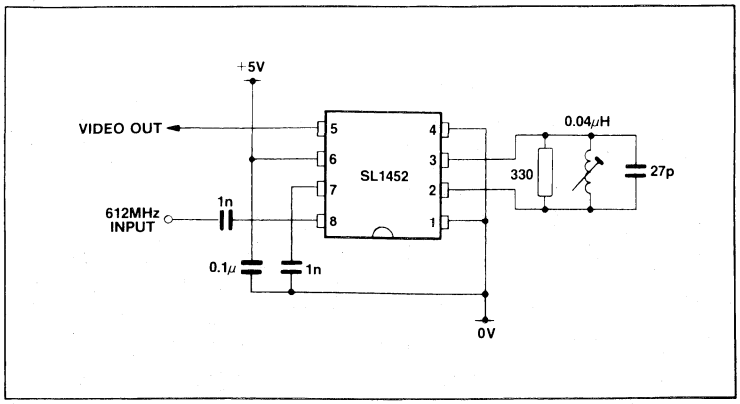


Fig.17 Typical application of SL1452

SL1452 QUADRATURE DEMODULATOR

The SL1452 FM demodulator has a simple application with very low external component count. This is demonstrated by the applications circuit diagram Fig.17, but as with most integrated circuits, particularly those working at high frequencies some attention to good RF layout techniques and correct component selection will ensure optimum results.

A good layout can usually be ensured by the simple precaution of keeping all components close to the SL1452, maintaining short lead lengths and ensuring a good low impedance ground plane. Double sided board layout enables these objectives to be easily met, but is not essential for satisfactory operation. All coupling and decoupling capacitors should be chosen for low impedance characteristics at high frequencies: multilayer ceramic types usually providing small size and adequate high frequency performance. For the quadrature coil tuning capacitor a fairly stable component should be selected to prevent excessive drift. The power supply decoupling capacitor from pin 6 to ground should be 0.1μF minimum but the input coupling and decoupling values can be smaller, about 330pF being adequate.

The only remaining components to be selected are those forming the quadrature circuit on pins 2 and 3 and some care in the determination of values for these is required if maximum performance is to be obtained.

First determine the quadrature circuit operating frequency, which is a quarter of the input frequency on pin 8 due to the two internal divide by 2 circuits (see Fig.2 on data sheet).

Choose suitable values for L and C to resonate at the correct frequency using:

$$f = \frac{1}{2\pi\sqrt{(LC)}}$$

The value of C should be greater than 15pF to prevent stray capacitance effects introducing errors and distortion of the demodulation curve, but the use of very large capacitances with small inductance values will lower the impedance of the tuned circuit at the required Q value, reducing the drive level to the demodulator and thereby restrict the video output available. In general for operation in the 400 to 600MHz range, an inductance value between 40 and 60nH is recommended.

Once suitable L and C values have been determined, the working Q for the quadrature circuit should be set, the Q value determining the video output level and bandwidth. Video output is proportional to Q whereas video bandwidth is inversely proportional. The effect of Q variations on video bandwidth and amplitude can be determined from Table 1 and the graphs in Fig.18.

A value for total damping resistor value to obtain the required Q can be calculated from:

$$R = Q2\pi fL$$

The internal 800 resistor between pins 2 and 3 must be allowed for when calculating R.

Example

Design a quadrature circuit to demodulate a carrier on pin 8 with centre frequency 480MHz and video bandwidth of 10MHz.

For L = 40nH and f_{quad} = 120MHz,
C = 43.98pF (nearest preferred value 47pF)
From Table 1, Q required is approximately 6
therefore total R required is:

$$R = Q2\pi fL$$

$$= 6 \times 2 \times \pi \times \frac{480}{4} \times 10^6 \times 0.04 \times 10^{-6}$$

$$= 181 \text{ ohms}$$

allowing for the internal 800 ohm resistance between pins 2 and 3 (see Fig.3 of data sheet), the external resistance required is 234 ohms. Choose 270 ohms.

It should be remembered that the internal 800 ohm resistance is subject to production tolerances and if fairly close control of video bandwidth is required, the L and C ratio may require some adjustment to ensure that the external R is sufficiently low to swamp the effect of internal resistance changes. The value of 270 ohms obtained in the example is low enough to allow adequate control.

In order to overcome the effects of component tolerances, it will usually be necessary to make either the L or C a variable component, the value being adjusted to obtain best linearity.

Q	BANDWIDTH
10	7.5MHz
6	14MHz
4	23MHz

Table 1

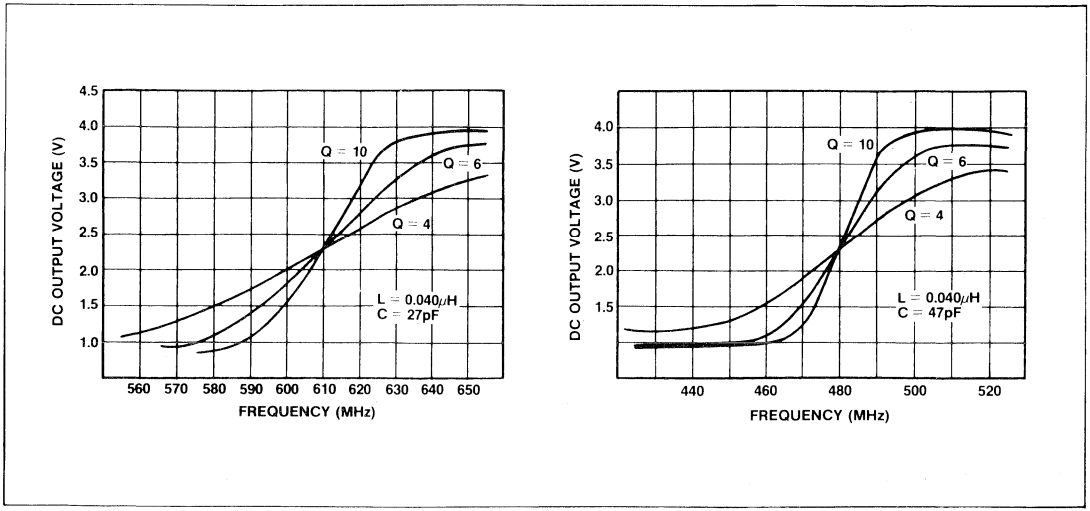


Fig.18 Output voltage versus input frequency

SL1455 EXTENDED THRESHOLD DEMODULATOR

The SL1455 is a wideband FM detector designed for Satellite TV applications. Fig.1a shows a typical application circuit for demodulating 612MHz and 480MHz wideband FM signals. The device is similar in principle to the SL1452 demodulator, but with the first divide by two stage replaced by an injection locked oscillator running at half the input frequency. Replacing the first divider in this way has the advantage that the noise threshold point can be extended by up to 3dB compared with a conventional quadrature detector such as the SL1452.

The span of input frequencies over which the oscillator will lock is referred to as the 'lock range'. The lock range of the oscillator is symmetrical about the centre frequency of the FM signal and can be altered by adjusting the input level to the device. Fig.20 shows how the lock range increases with input level.

An additional advantage of this device is the ability to program the degree of extension available by controlling the input level to the circuit.

Threshold extension is achieved by reducing the lock range of the oscillator so that it is just capable of locking onto the input FM signal (usually the peak to peak deviation +10MHz). The effect of reducing the lock range on noise threshold of a 612MHz demodulator is shown in Fig.21. The only detrimental effect of reducing the lock range is that it reduces the video bandwidth, see Fig.22.

The application circuits consists of 2 main sections, the tuned circuit for the oscillator and the quadrature network. The oscillator tuned circuit is designed to resonate at half the FM signal centre frequency with the internal device capacitance of 11pF between pins 3 and 4. The simplest solution is an inductor across pins 3 and 4. The value of this inductor can be calculated from:

$$L = \frac{1}{C_{INT}(2\pi f)^2} \quad C_{INT} = 11pF$$

However, this will produce a very small value of L for high frequency oscillators. A larger value of inductor can be used in series with a capacitor which effectively reduces inductance. The value of this capacitor can be calculated from:

$$C = \frac{1}{(Lp - L)(2\pi f)^2}$$

Lp = inductance used
L = inductance needed for resonance

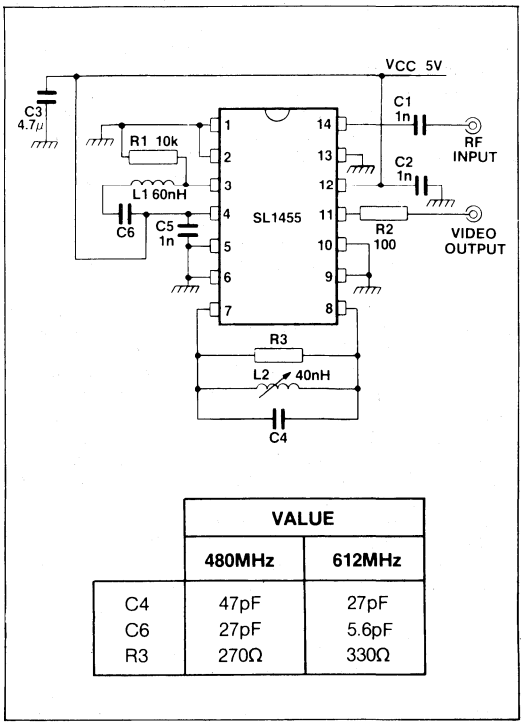
Lp must not be too much larger than L otherwise impractical values for C will be obtained.

Example

For a 612MHz FM demodulator a 306MHz oscillator is to be designed.

L = 24nH for resonance with the internal 11pF.

This is a rather small and non-standard value of inductor, so a more readily available value 60nH is chosen. To convert this to an effective inductance of 24nH, 7.6pF would theoretically be added in series but as practical track layout has some finite inductance (about 10nH in the layout shown in Fig.24) a revised capacitance of 5.6pF is more accurate.



	VALUE	
	480MHz	612MHz
C4	47pF	27pF
C6	27pF	5.6pF
R3	270Ω	330Ω

Fig.19 Typical application 480 and 612MHz threshold extended demodulator

One of the components in the tuned circuit should be made variable to fine tune the oscillator to half the FM signal centre frequency. The centre frequency needs to be relatively accurate for optimum threshold performance.

Calculations to determine the values of quadrature components between pins 7 and 8 are exactly as for the SL1452 (p.15), as are those given in the example for the damping resistor between pins 7 and 8 (pins 2 and 3 on the SL1452).

The Q factor determines the video output level and bandwidth (although with Q factors of below 10 the video bandwidth is defined by the lock range of the oscillator).

Video output is proportional to Q whereas video bandwidth is inversely proportional. The effect of Q variations on video bandwidth and amplitude can be determined from Table 1 and the graphs in Fig.23.

Practical System Design

When designing the PCB for the SL1455 good RF layout techniques should be applied. All track lengths should be kept to a minimum and decoupling capacitors placed as close to the device as possible. A ground plane is recommended - see Fig.24 for an example of layout.

With this form of demodulator a further increase in threshold extension can be achieved by designing a circuit in which the injection-locked oscillator tracks the incoming FM signal. To do this a varactor diode is incorporated in the oscillator circuit to produce a voltage controlled oscillator. This VCO can then be controlled by feedback from the video output. The amplitude of the video feedback to the oscillator is calculated so that the oscillator tracks the FM input very closely.

The only problem encountered when designing a system with video feedback is compensating for a 40ns delay introduced by the SL1455 between the FM input signal and the video output. This delay is insignificant for low frequency feedback to the tracking oscillator, but does effect the chroma feedback. For a PAL system (chroma subcarrier frequency = 4.433MHz) a phase advance of 63° in the feedback network is necessary to compensate for this delay. For an NTSC system a phase advance of 50° is necessary (chroma subcarrier frequency = 3.58MHz).

Most satellite broadcasts employ pre-emphasised signals in which the chroma and high frequency information has a much larger peak-to-peak deviation than the low frequency information. The feedback network needed to feed back the full demodulated video with the correct phase and amplitude would be very complex. But as a large portion of the signal is chroma subcarrier, using simple chroma feedback the overall noise threshold can be improved.

Fig.25 shows a 612MHz demodulator with chroma feedback for a PAL signal. The feedback network consists of an amplifier with phase correction components (C7, R4, R5, C9, R10). The voltage to frequency gain of the VCO is 5MHz per volt. As the oscillator locks to half the input frequency it will effectively track the input frequency at 10MHz per volt. The quadrature components are set to give a 1V peak-to-peak output for an input signal with a 20MHz peak-to-peak deviation. For the oscillator to track the chroma correctly a voltage gain of 2 is required in the feedback network.

The centre frequency of the oscillator is governed by the supply voltage and the variable 60nH inductor.

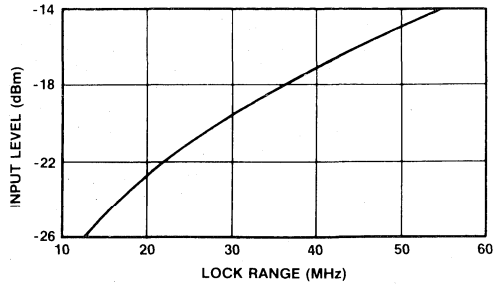


Fig.20 Lock range versus input level

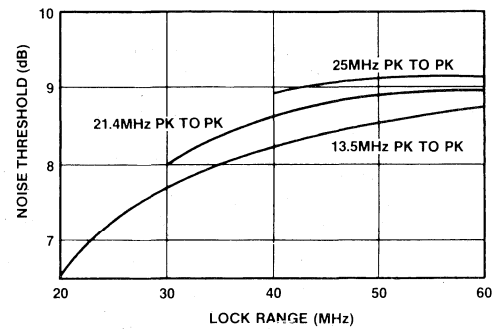


Fig.21 Lock range versus threshold

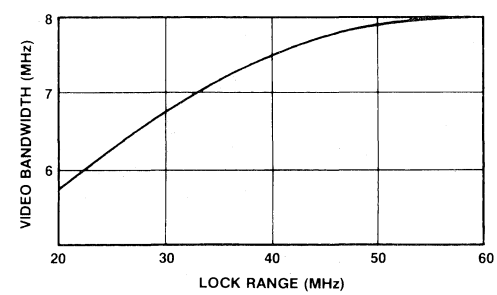


Fig.22 Lock range versus bandwidth

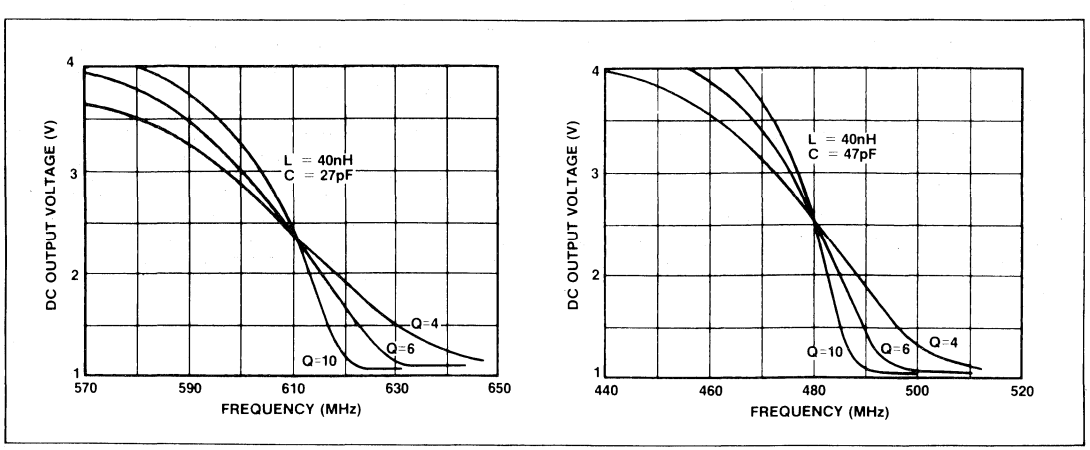
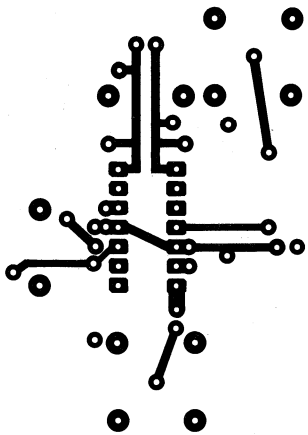
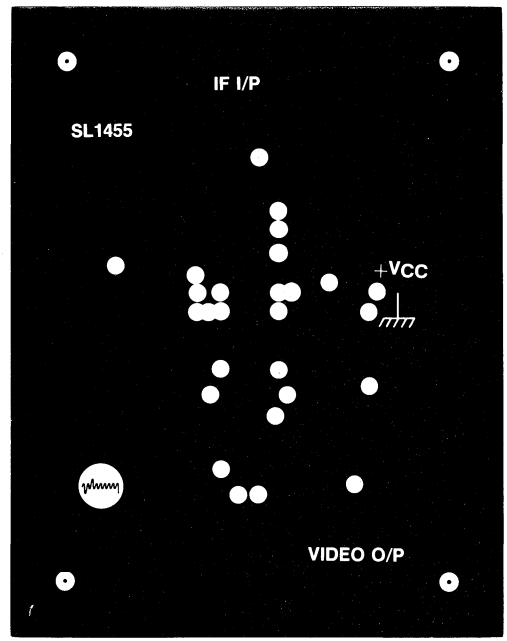


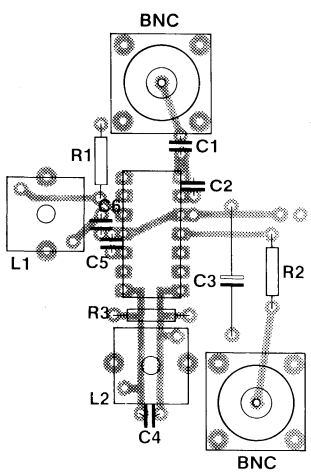
Fig.23 SL1455 output voltage versus input frequency for large lock range



Track side



Ground plane



Component overlay

COMPONENTS			
R1	10k	C1	1n
R2	100Ω	C2	1n
R3	330Ω	C3	4.7μ
		C4	27p
		C5	1n
		C6	5.6p
L1	60nH TOKO COIL		
L2	40nH TOKO COIL		
	+2 BNC SOCKETS		

Fig.24 Recommended board layout for 612MHz SL1455 FM demodulator circuit of Fig.19

This circuit improved the chroma noise threshold response without deteriorating the black and white noise threshold. Components for an NTSC version are C7 = 390pF, all others are the same as with the above PAL version.

To check that the feedback loop has a gain of just less than 1 (for stability) and that the phase compensation network is correct, the loop can be opened at point A and a signal (chroma frequency) injected from a signal generator to the VCO (via C11) and the output of the emitter follower (B) monitored. L3 should be adjusted for maximum output and the overall gain may be altered by varing R8. If the phase is incorrect, C9 and C7 should be checked. These measurements should be done whilst no signal is applied to the input of the device.

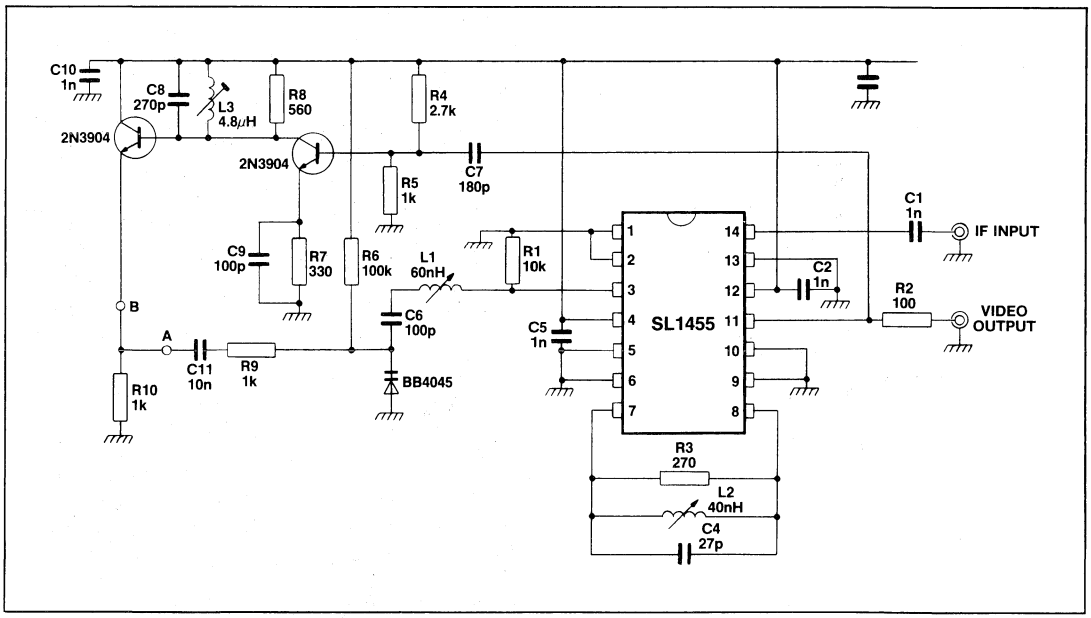


Fig.25 612MHz demodulator with chroma tracking injection locked oscillator

SL1454 LOW FREQUENCY QUADRATURE DEMODULATOR

The SL1454 FM demodulator has a simple application with very low external component count. This is demonstrated by the applications circuit diagram Fig.26, but as with most integrated circuits, particularly those working at high frequencies, some attention to good RF layout techniques and correct component selection will ensure optimum results.

A good layout can usually be attained by the simple precaution of keeping all components close to the SL1454, maintaining short lead lengths and ensuring a good low impedance ground plane. Double sided board layout enables these objectives to be easily met, but is not essential for satisfactory operation. All coupling and decoupling capacitors should be chosen for low impedance characteristics at high frequencies. A fairly stable component should be selected for the quadrature coil tuning capacitor to prevent excessive drift. The power supply decoupling capacitor from pin 6 to ground should be 0.1μF minimum, but the input coupling and decoupling values can be smaller, about 1nF being adequate.

The only remaining components to be selected are those forming the quadrature circuit on pins 2 and 3 and some care in the determination of values for these is required if optimum performance is to be obtained.

Choose suitable values for L and C to resonate at the intermediate frequency you are applying to the device using:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

The value of C should be greater than 15pF to prevent stray capacitance effects introducing errors and distortion of the demodulation S curve, but the use of very large capacitances with small inductance values will lower the impedance of the tuned circuit at the required Q value, reducing the drive lead to the demodulator and thereby restrict the video output available.

Once suitable values for L and C have been determined, the working Q for the quadrature circuit should be set, the Q value determing the video output level and bandwidth. Video output is proportional to Q whereas video bandwidth is inversely proportional. The effect of Q variations on video bandwidth and amplitude can be determined from Table 2 and the graphs in Fig.27.

A value for total damping resistor value to obtain the required Q can be calculated from:

$$R = Q2\pi fL$$

The internal 800Ω resistor between pins 2 and 3 must be taken into account when calculating R.

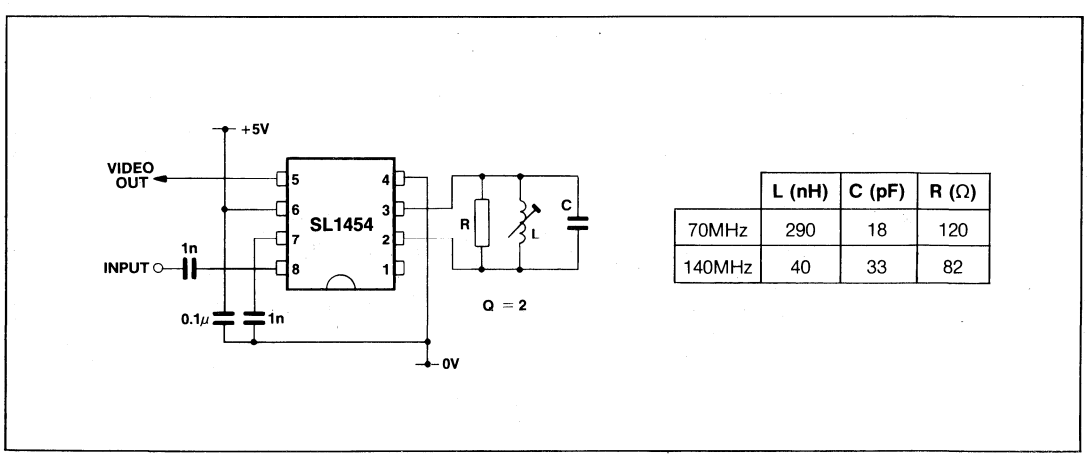
As can be seen from the graphs in Fig.27, for the demodulator to demodulate a 20MHz peak-to-peak deviation signal with optimum linearity a very low Q value needs to be chosen (<2). But this has the disadvantage of producing a demodulator with a very low peak-to-peak video output level.

One way of increasing the linear region of the S curve without reducing the video output level is to incorporate a dual tuned circuit to the normal quadrature tuned circuit.

Fig.28 shows an example of this form of dual tuned circuit, both sections have the same Q factor and the coupling capacitors are chosen to give the best linearity (linear phase response). Fig.27(b) shows the advantages of the dual tuned circuit. The effect of varying the Q factor of the dual tuned circuit on bandwidth is also described by Table 2.

Q	BANDWIDTH
6	10MHz
4	11MHz
2	12MHz

Table 2



	L (nH)	C (pF)	R (Ω)
70MHz	290	18	120
140MHz	40	33	82

Fig.26 Typical applications for 70 and 140MHz

Example

Design a quadrature circuit to demodulate a 140MHz carrier with 21.4MHz peak-to-peak deviation, modulated with a 25Hz triangular dispersion waveform of 2MHz peak-to-peak deviation. The video bandwidth required is 9MHz.

Choose L $= 0.04\mu H$
then C $= 32.309pF$ (nearest preferred value $= 33pF$)

The next value to choose is the Q factor. As dispersion is employed linearity over the full 21.4MHz range needs to be optimised. The graphs in Fig.28 show that either a single tuned circuit with a Q of 2, or a dual tuned circuit with a Q of 3 is adequate. The dual tuned circuit has the advantage that the peak-to-peak video output is larger than that of the single tuned circuit, but extra components are required. Both circuits have a larger video bandwidth than the required 9MHz. The value of the damping resistor for the required Q is calculated as below:

For Q $= 2$

Total R $= Q2\pi fL$

$= 2 \times 2 \times \pi \times 140 \times 10^6 \times 0.04 \times 10^{-6}$

$= 70.37\Omega$

Allowing for the internal 800Ω resistor the external resistance should be 77.1Ω, choose 82Ω.

For Q $= 3$

Total R $= Q2\pi fL$

$= 3 \times 2 \times \pi \times 140 \times 10^6 \times 0.04 \times 10^{-6}$

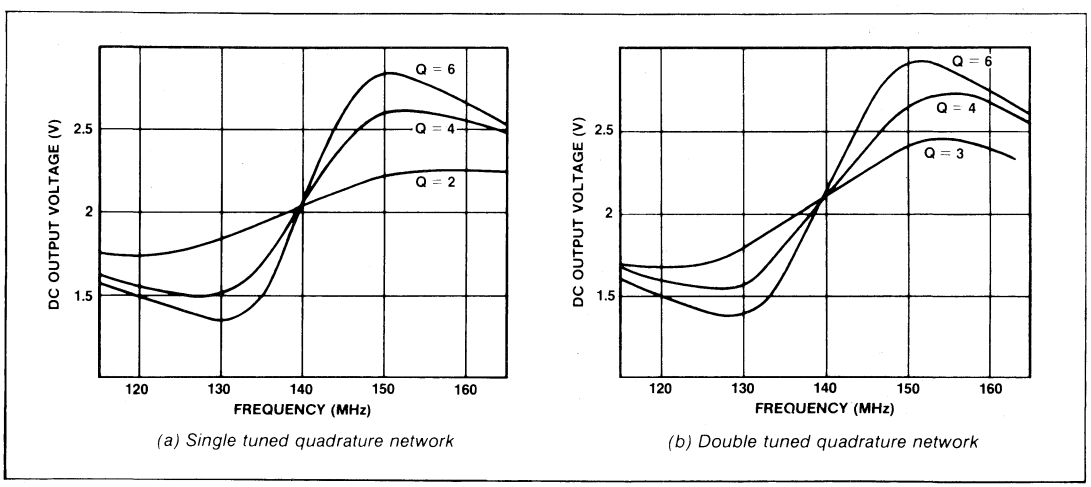
$= 105.56\Omega$

Allowing for the internal 800Ω resistor the external resistance should be 121.5Ω, choose 120Ω.

When using a dual tuned circuit the value of coupling capacitor is dependent on the Q factor. Table 3 gives a guide to the values need for best linearity.

Q	COUPLING CAPACITOR
6	3.9p
4	5.6p
3	10p

Table 3



(a) Single tuned quadrature network

(b) Double tuned quadrature network

Fig.27 Output voltage versus frequency

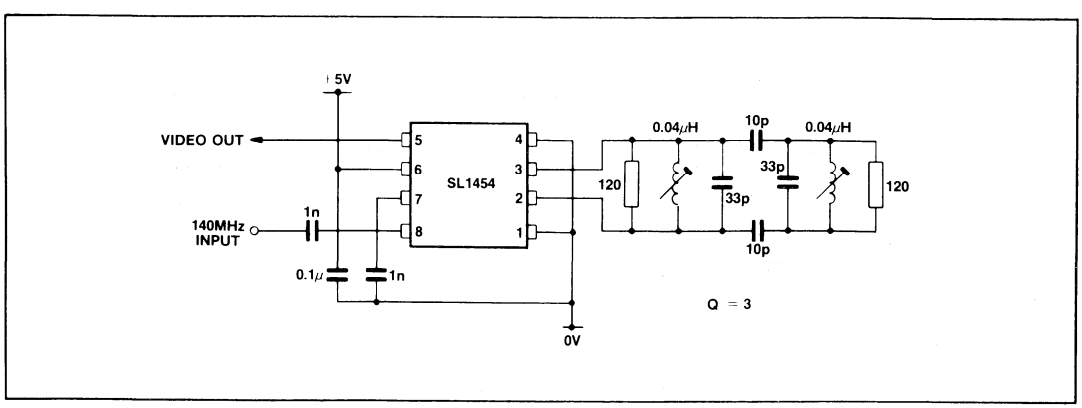


Fig.28 Example of a double tuned quadrature circuit

Designing with the SL1451 Phase Locked Loop

The SL1451 is a phase locked loop circuit originally designed as a demodulator for satellite TV signals. As a consequence of the trend towards high frequency IF design in satellite receivers, the SL1451 has been designed to operate at frequencies up to 612MHz, but despite this very high maximum operating frequency and specific design objective, the SL1451 is still useful as a general purpose phase locked loop in many other applications.

In order to demonstrate the versatility of the part, a design for an FM demodulator for broadcast radio was tested. The circuit diagram of the demodulator is shown in Fig.1 and a block diagram of the PLL system is shown in Fig.2. When designing for uses other than satellite TV demodulation, two main circuit areas require design changes, these are the oscillator and loop filter components.

OSCILLATOR DESIGN

The design is fairly straight forward as only a single transistor is involved as shown in Fig.3. Any conventional oscillator configuration is possible except those requiring an output from the collector as this is internally decoupled to ground. When operating at lower frequencies, in this case 10.7MHz it is simpler to use a Hartley type oscillator with tapped coil rather than the Colpitts type employed in the satellite demodulator since the low value internal bias resistors will not allow direct connection to the tuned circuit without excessive damping.

When designing the oscillator the centre frequency (in this case 10.7MHz) must be obtained at the centre point of the linear range of the output amplifier (4.5V) on pin 14, and the slope of the oscillator voltage/frequency characteristic must allow the output amplifier to remain within its linear range at the maximum expected deviation of the input signal. In this case, the oscillator slope has been set at about 0.1MHz/Volt, giving a maximum output swing of 1.5V p-p for a 150kHz deviation FM signal. The 68pF and 27pF capacitors associated with the varicap diodes control the oscillator slope characteristic. An isolating network preventing loading of the tuned circuit by the amplifier output is required. Values must be chosen to present a high impedance at the oscillator operating frequency (10.7MHz) but allow feedback of the maximum demodulated frequency, say 20kHz for mono FM radio.

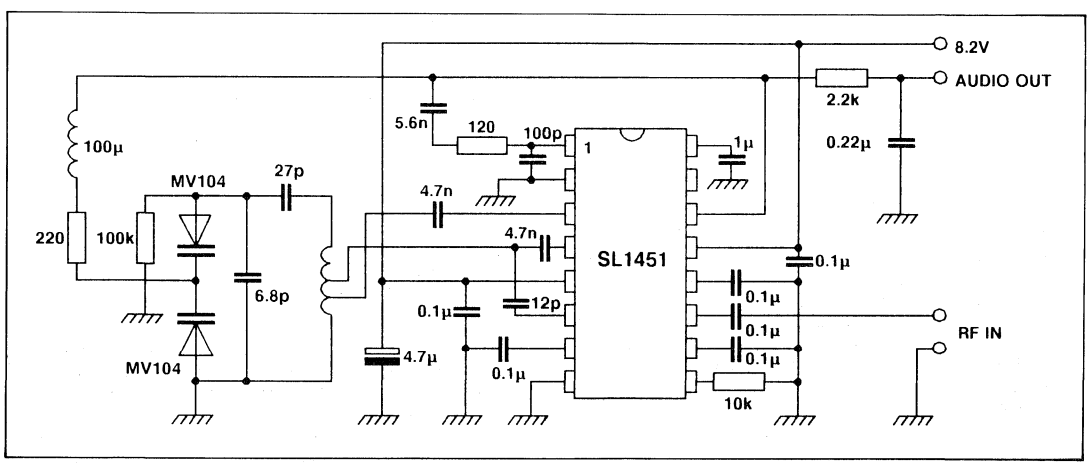


Fig.1 FM radio demodulator circuit

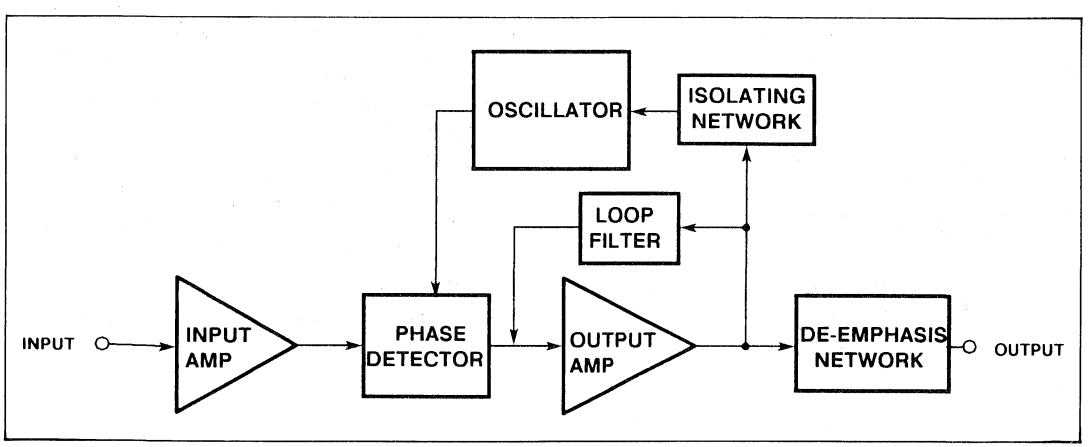


Fig.2 Phase locked loop configuration

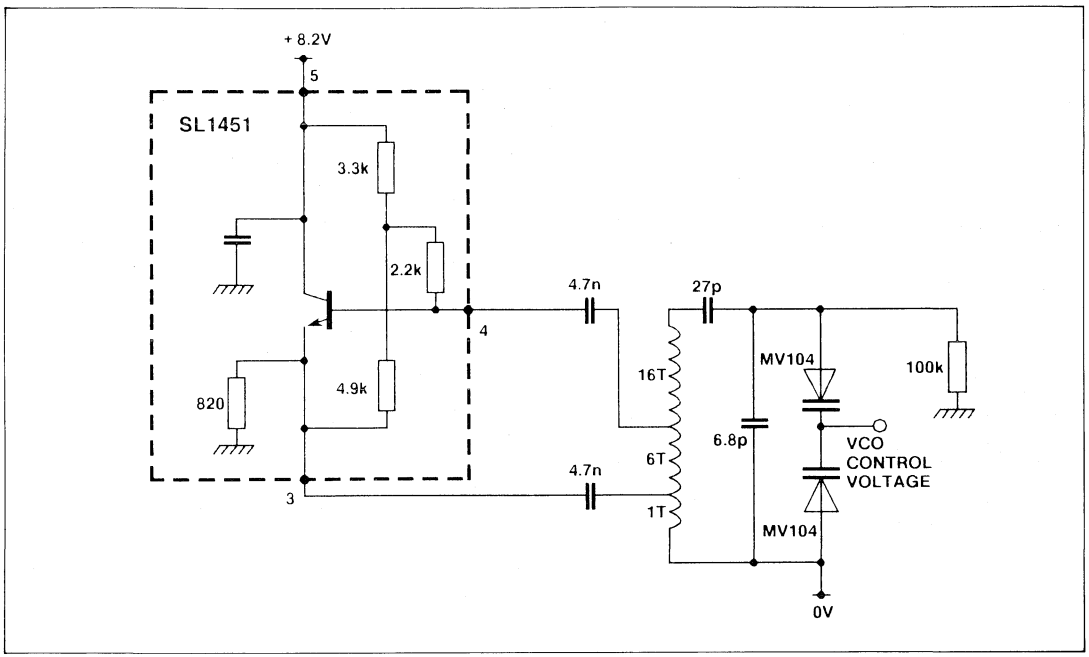


Fig.3 Oscillator configuration

LOOP FILTER

Having determined a suitable oscillator design, the most critical part of the design, the calculation of suitable values for the loop filter components is required. The equivalent circuit of the output amplifier with loop filter components is shown in Fig.4, and as can be seen, the choice of component is restricted to some extent, since R1 and part of R2 are internal.

The value of C can be determined from:

$$C = \frac{K_O K_D}{R1\ \omega n^2}$$

where: K_O is the phase detector gain in V/radian
K_D is the oscillator slope in radian/volt second
ωn is the natural loop bandwidth

Having determined the value of C, R2 can be obtained from:

$$R2 = \frac{2}{C\ \omega n}$$

where: is the damping factor
ωn is the natural loop bandwidth

For the prototype FM sound demodulator, the following parameters were used.

K_O = 0.5V/rad (from data sheet)
K_D = 0.628Mrad/Vs (100kHz/V oscillator design)
R1 = 570Ω (from Fig.4)
ωn = 0.314Mrad/Vs (50kHz natural loop bandwidth)
= 0.7071 (critical damping)

giving:

$$C = \frac{0.5 \times 0.628 \times 10^6}{570 \times (0.314 \times 10^6)} = 5.58nF$$

$$R2 = \frac{2 \times 0.7071}{5.58 \times 10^{-9} \times 10.314 \times 10^6} = 807.14\Omega$$

allowing for R2 int = 680Ω, R2 ext = 127Ω

All remaining components are non critical, being for coupling/decoupling purposes, apart from the 2.2k/0.022μF RC time constant on the output which provides a 50μs de-emphasis characteristic.

The demodulator was tested in a standard FM receiver using a CA3089 type limiting strip and quadrature demodulator. A connection was made between the input of the SL1451 and the output of the 3089 limiting strip on pin 8 thus bypassing the quadrature detector. Compared to the standard quadrature detector, a noticeable improvement in output signal to noise ratio at low input levels and an improvement in adjacent channel rejection was found.

SUMMARY OF SL1451 FM DEMODULATOR PERFORMANCE

Centre of IF		10.6MHz
Pull in range	10.5MHz to 10.75MHz Input	= -30dBm
Hold range	10.37MHz to 10.75MHz Input	= -30dBm
Input sensitivity for ±75kHz deviation at 15kHz		-30dBm
Distortion with ±75kHz deviation at 1kHz		<1%

CONCLUSION

The SL1451 is useful as a general purpose phase locked loop as well as in satellite TV FM demodulator applications.

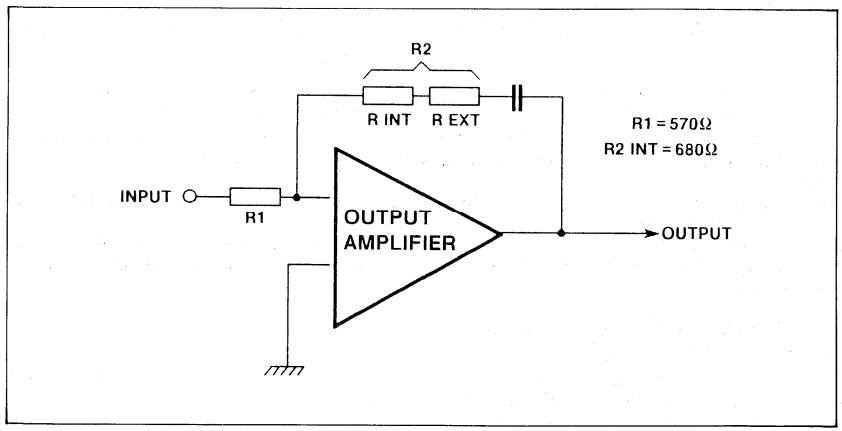


Fig.4 Equivalent circuit of amplifier with loop filter components

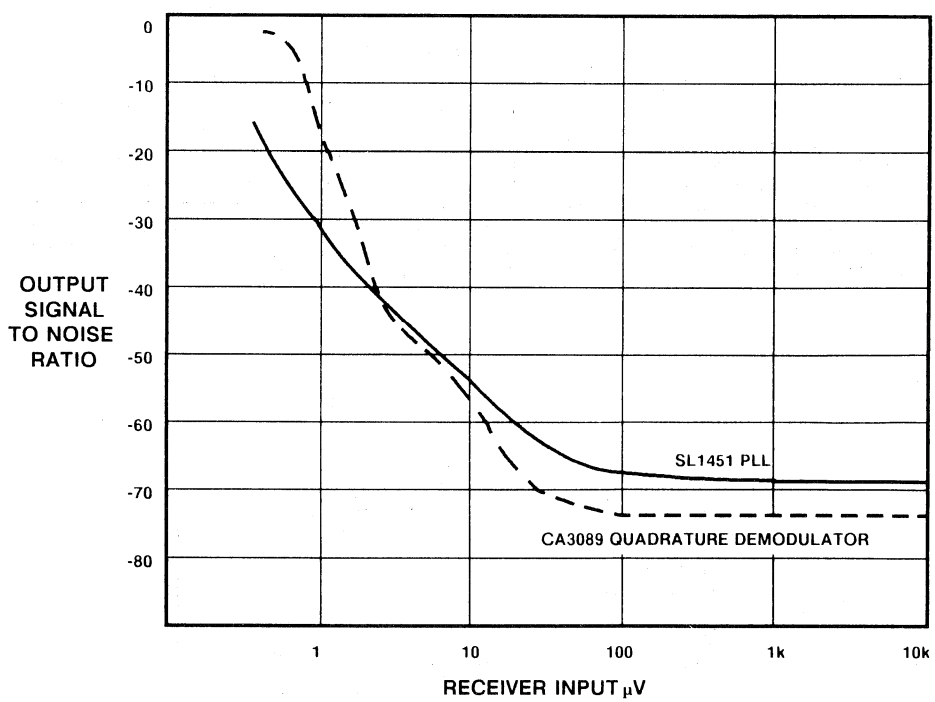


Fig.5

MV500 CMOS Remote Control Transmitter AN37

This application note describes a number of circuits using the MV500 which show how, by utilising various device characteristics, its use may be extended from the standard application circuit shown in the data sheet.

One of the main features of the MV500 is its ability to work at low supply voltages. Reduction in the supply voltage, however, has the drawback of limiting the range of the infra-red link. One possible method of improving this range is shown.

It is sometimes desirable to transmit data via a fixed wire link instead of using infra-red and two examples are given of this type of communication.

Occasionally, it is required to interface a remote transmitter to a logic system rather than a simple keyboard. In these cases, it is often desirable to present data to the transmitter in the form of a binary code and a method of achieving this is shown.

INCREASING THE RANGE OF AN INFRA-RED LINK AT LOW SUPPLY VOLTAGES

The intensity and therefore range of the infra red link is determined by the current in the transmitting diodes. As the supply voltage is reduced, the minimum current available from the MV500 output drops from 50mA at 6V to 10mA at 3V. The transistor driving the transmitting diodes is required to work in a saturated mode with very low collector voltage in this application, particularly with the supply reduced to 3V. Under these conditions, the available gain to be expected from the output transistor will be low, preventing a suitable drive current being available for the transmitting diodes if the standard single transistor circuit is used.

Fig. 1 shows a circuit suitable for use at lower voltages where an additional transistior is used to ensure adequate diode current.

To ensure a low saturation voltage for the PNP transistor, the base drive is set to around a tenth of the required output current by the 8.2Ω resistor in series with the base. The requirements for saturation voltage are less critical for the NPN transistor which is operating at a collector current only one tenth that in the output transistor. In this case a much higher gain can be expected and the 10mA available from the MV500 is quite adequate.

The critical characteristics for the transistors used in the prototype are as follows.

PNP TYPE - ZTX749

Parameter	Typ.	Max.	Conditions
$V_{CE\ (SAT)}$	0.23V	0.5V	$I_C = 2A$, $I_B = 200mA$
h_{fe}	75	150	$I_C = 2A$, $V_{CE} = 2V$

NPN TYPE - ZTX650

Parameter	Typ.	Max.	Conditions
$V_{CE\ (SAT)}$	0.12V	0.3V	$I_C = 1A$, $I_B = 100mA$
h_{fe}	100	200	$I_C = 500mA$, $V_{CE} = 2V$

The peak current in the diodes is controlled by the 1Ω resistors in series. Using this value the current is approximately 750mA in each diode.

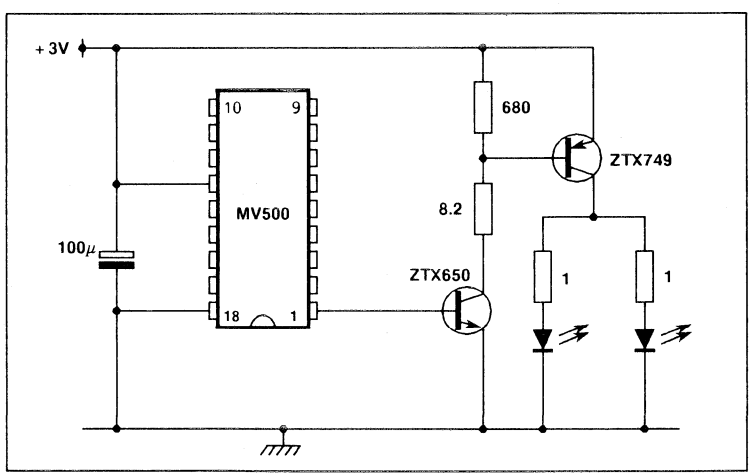


Fig.1 Increasing range of infra-red link

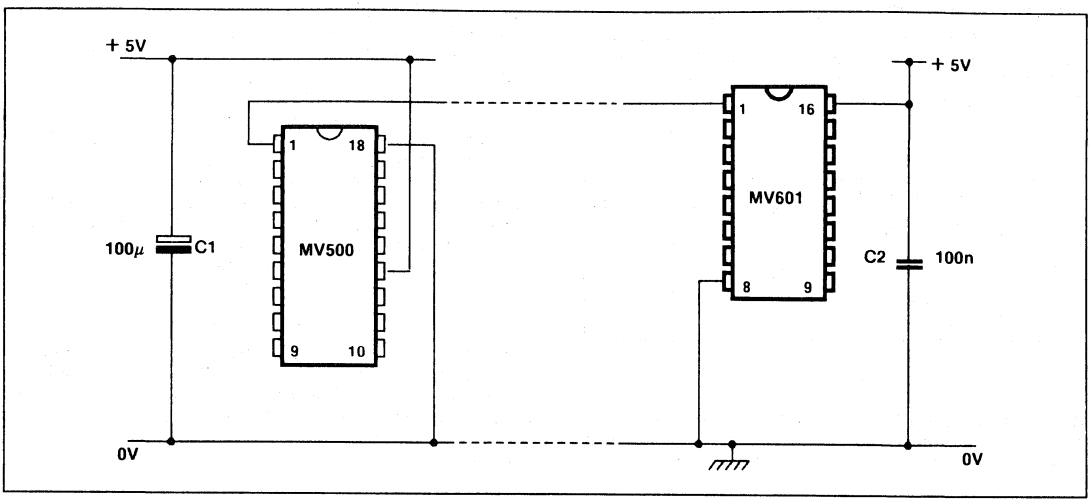


Fig. 2 Two-wire data link, separate supply

DATA TRANSMISSION OVER FIXED WIRE LINK

The MV500 is normally used to transmit remote data via an infra-red link, however, transmission over a dedicated wire link is possible. By using it in conjunction with an MV601 receiver, the MV500 may be connected via a simple two wire link as shown in Fig. 2. The maximum distance between transmitter and receiver will be limited mainly by the noise picked up from the environment in which it is used.

The circuit of Fig. 2 assumes that separate power supplies are available at the transmitter and the receiver; however it is necessary to common the two ground supplies of the transmitter and receiver.

If separate supplies are not available and a three-wire link is undesirable, it is possible to use a two-wire link for both power and data transmission. The circuit of Fig. 3 shows how this may be achieved. Power for the MV500 is supplied along the line, with C1 keeping the supply to the MV500 constant. Output pulses from the MV500 turn TR1 on, which short-circuits the power supply temporarily and creates brief negative going pulses at the input to the MV601. D1 isolates the supply to the MV500. Resistor R1 acts as the terminating impedance for the 100Ω twisted pair line, which allows communication over a reasonable distance.

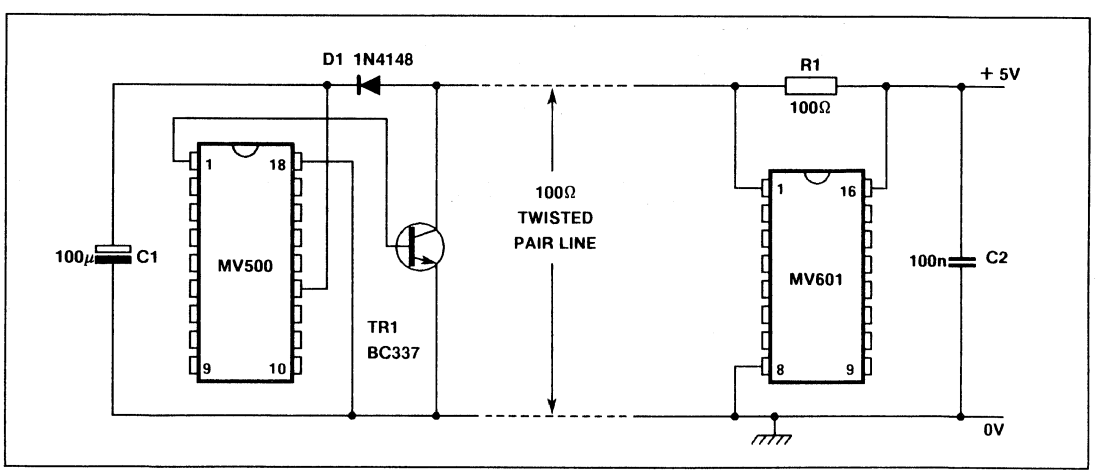


Fig.3 Two wire supply and data link

INTERFACE TO LOGIC SYSTEM

The MV500 keyboard inputs can be driven directly from binary logic provided that certain precautions are taken. Only five of the inputs are used to control up to 32 different output codes, as listed below,

Bit No.	Name	Pin No.	True or Inverted
4	100XX	5	T
3	010XX	7	T
2	001XX	8	T
1	XXX10	11	I
0	XXX01	12	I

where bit 4 is the MSB and is transmitted last. Bits 0 and 1 need to be inverted for correct binary coding, as shown in Fig. 4. The unused inputs should be left open circuit.

LOGIC VOLTAGES AND CURRENTS

Assuming the MV500 is being used with a 4.5V to 5,5V DC supply, then the logic levels should be within the following limits:

V_{IL} max. = 1.2V
V_{IH} min. = 3.5V

Since in normal operation the inputs are supplied by currents from within the MV500 and the contact sensing relies on switching these inputs to the supply rails, some current limiting is needed. This can be provided by connecting a series resistor in series with each input or by limiting the logic source to the following currents:

I_{OH} max. = 1.2mA
I_{OH} min. = 75μA
I_{OL} max. = −1.2mA
I_{OL} min. = −75μA

If a resistor is used some allowance should be made for the voltage drop across it to ensure the correct logic level is being reached. A value of 4.7kΩ is recommended: this will have a 0.36V drop across it and the logic levels V_{IH} min. and V_{IL} max. will need to be 3.86V and 0.84V, respectively.

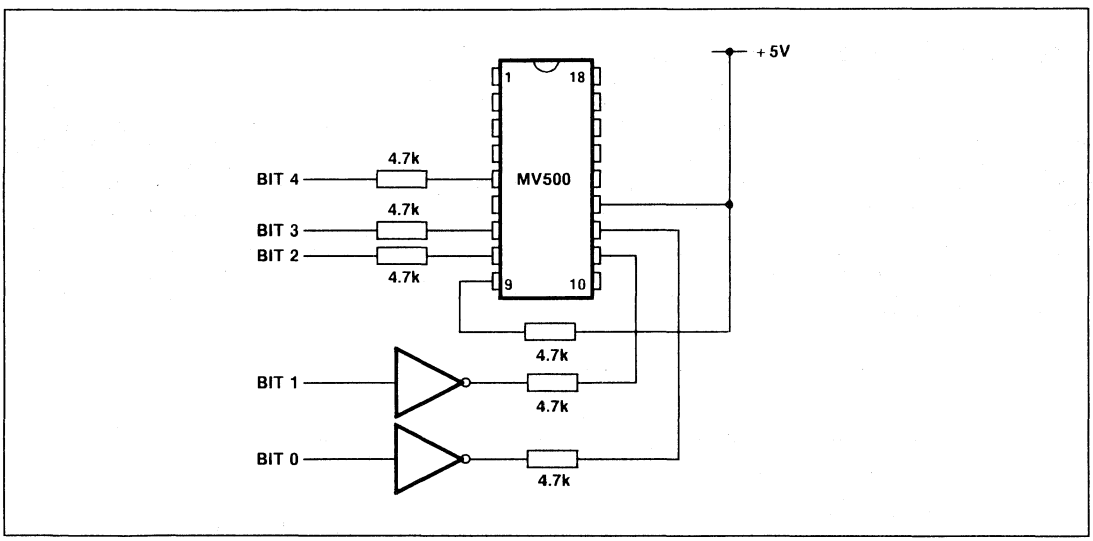


Fig.4 MV500 logic interface

SL490 to MV601 Interface

This application brief describes how to use the SL490 remote control transmitter with the MV601 remote control receiver. The MV601 is designed to work with a ceramic resonator to generate a stable clock. When this device is used with its counterpart transmitter (MV500), which also uses a ceramic resonator, no setting-up is required for either transmitter or receiver. The SL490 can be used to transmit to the MV601, as both devices use the same coding of data. This brief describes how to design the circuit around the SL490. The interface link is commonly infra-red but could be either radio, ultra-sonic or a wire link. In this example the frequency of the ceramic resonator is 500kHz.

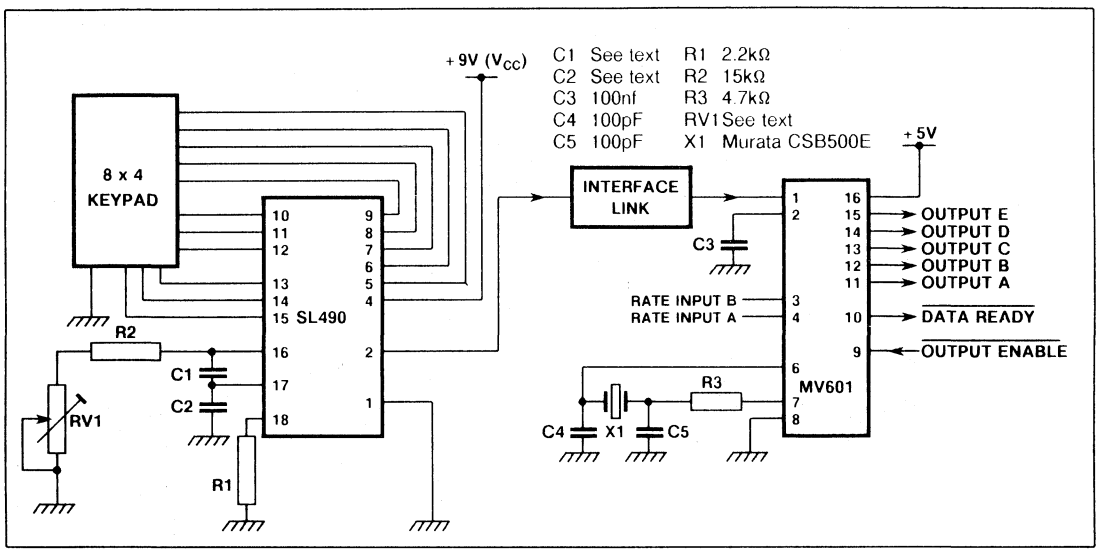


Fig.1 Circuit diagram

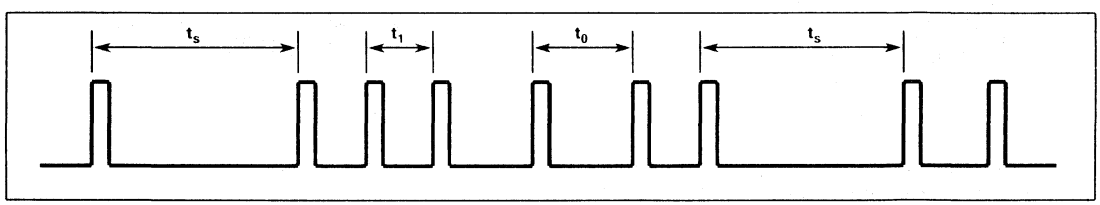


Fig.2 Typical received / transmitted data

Three time intervals are transmitted by the SL490:

t_S is the inter-word gap and is of duration 6T

t_1 is the pulse to represent a '1' and is of duration 2T

t_0 is the pulse to represent a '0' and is of duration 3T

T is the length of time derived from the RC oscillator on the SL490. This period must match the time interval of the MV601, calculated from the frequency of the ceramic resonator, X1, and the rate settings.

For the SL490:

$T = 0.475 \times C1 \times (R2 + RV1)$

For the MV601,:

$T = CC/f_C$

where f_C is the frequency of the ceramic resonator. CC, the number of clock cycles, is dependent on the rate settings (MV601 pins 3 and 4).

Pin 3 =	0	0	1	1
Pin 4 =	0	1	0	1
CC =	NV	2048	1024	512 (NV = Not Valid)

EXAMPLE

Let $f_C = 500kHz$ with CC set to 2048 (pin 3 = 0V, pin 4 = +5V)

$T = 2048/500000$

$= 4.096 \times 10^{-3}$

$\therefore C1 \times (R2 + RV1) = 4.096 \times 10^{-3}$

Let C1 = 100nF

$R2 + RV1 = 41k\Omega$

This is the theoretical value for these resistors. Due to manufacturing tolerances of all the components, it is advisable that R2 is set to the minimum value for pin 16 (15kΩ), with RV1 a 47kΩ potentiometer. The circuit can then be tuned to match the MV601 decoder. Other data rates can be easily calculated from the above information. It is advisable to stick with the values suggested for R2 and RV1 and to change the value of C1.

A 600MHz AGC Controlled IF Amplifier for the SL1455

From the SL1455 data sheet and application note, it will be seen that the degree of threshold extension and the video bandwidth are determined by the input level. For best results some method of accurately setting the input level and maintaining it under varying signal conditions is desirable. Various methods of controlling signal level are possible including the use of PIN diode attenuators, limiting amplifiers, etc. but the AGC system described here appears to offer a low cost flexible system with adjustable output level and wide AGC range (up to 45dB) which cannot be easily obtained by other means.

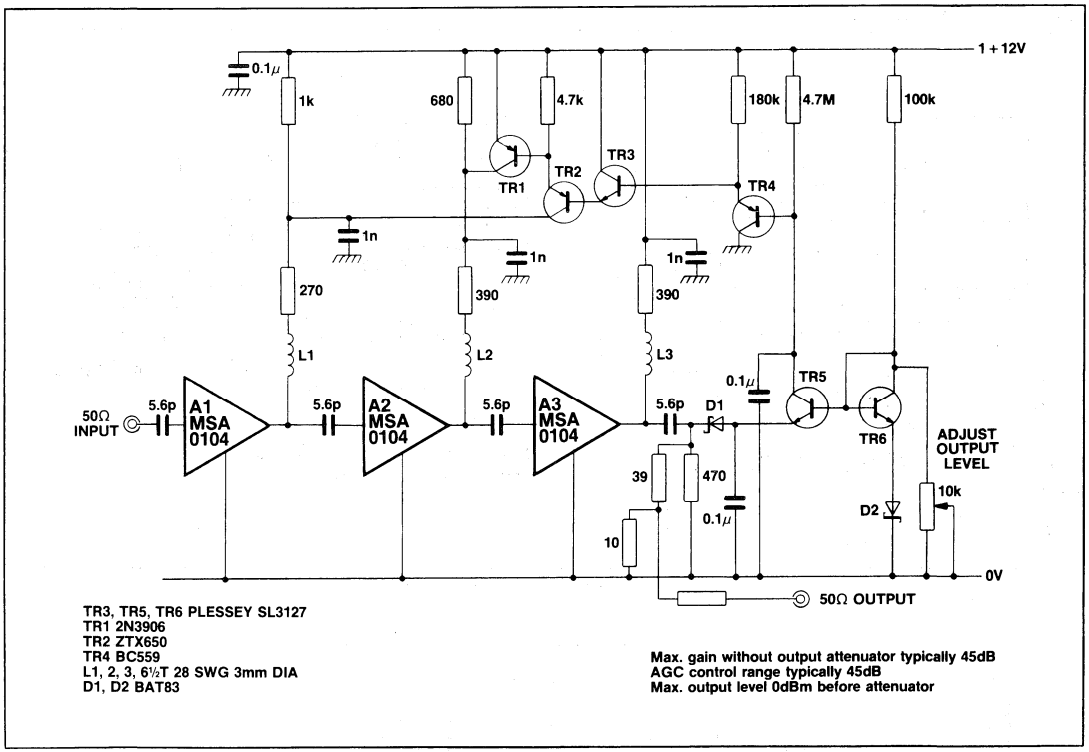


Fig.1

Gain is provided by a cascade of three Avantek MSA-0104 amplifiers with a gain of about 15dB per stage. The output from the third stage is detected and the resulting DC used to control the gain of the first two amplifier stages.

In order to allow detection at the low signal levels required by the SL1455, and to allow a degree of temperature compensation in the AGC point, a balanced arrangement of two transistors and Schottky diodes is used, increasing signal levels at the output producing an increasingly negative output at D1 anode. The negative output from the diode turns on TR5 which decreases the current in the first amplifier stage via the emitter followers TR2, 3 and 4 thus reducing the gain and maintaining constant output.

As the input signal is increased further, current in the first amplifier reduces until TR2 is no longer passing sufficient current to hold TR1 on, at which point the supply current to amplifier two is reduced, continuing the AGC action until TR1 is fully switched off.

The 1k and 680Ω resistors in parallel with TR1 and TR2 set a minimum current level in the amplifiers which is designed to allow a minimum gain level consistent with sufficient signal handling to drive subsequent stages. This together with the sequencing of the gain reduction system prevents overload in any of the amplifiers for all input signal levels within the dynamic range.

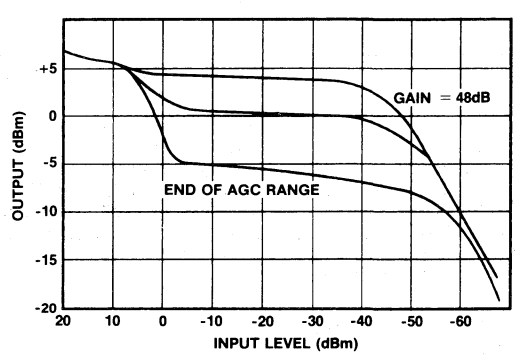


Fig.2 Characteristics of IF strip with AGC at 610MHz

Despite the balanced detector arrangement, it is still not possible to provide reliable AGC detection at the typical -20dBm level required for best threshold performance in the SL1455 and therefore a fixed T type attenuator is used to reduce the output level. Fine control of output level is provided by the potentiometer RV1 which allows adjustment for IC and other component tolerances.

An AGC System for Satellite Receiver IF Strips using the SL1451

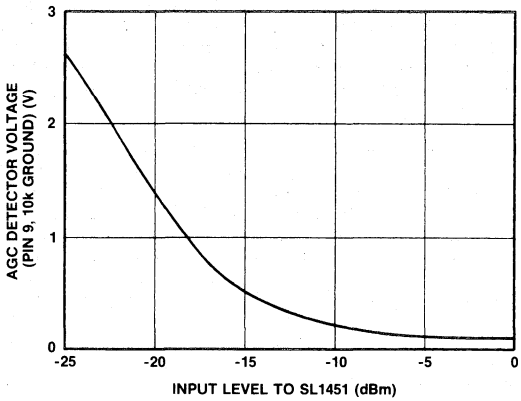


Fig.1 SL1451 AGC output characteristic

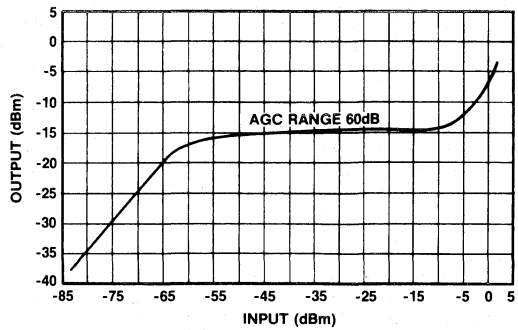


Fig.2 AGC characteristic of 612MHz IF strip

The detector output from the Plessey SL1451 has a characteristic described by Fig.1.

This characteristic can be used in an AGC circuit as shown in Fig.3. The maximum gain of the IF circuit is 45dB and this occurs when TR1 is switched off, hence TR2, TR3, TR4 provide the current for the first two amplifying stages. the gain of these stages can be reduced by reducing their supply current. As TR1 is gradually turned on the current supply to the first amplifier is reduced until all the current is supplied via the 1k resistor, then the second stage current is reduced until all the current for it is supplied via the 680Ω resistor. As the gain is reduced the detector output level increases and TR1 is switched further off, thus stabilising at a given output level. The gain of the system is set by the 100Ω and 180k resistors and the system is damped by the 180k and 4.7μF time constant. The output level is adjusted by altering the switch on point of TR1. This is done by varying the base bias of TR1 (via the 2.2k variable resistor). -15dB is the optimum level for the input to the SL1451.

The IF filter can either be situated after the IF strip or between amplifying stages. It may be advantageous to place the filter before the final amplifying stage as this reduces the out of band noise and adjacent channel levels which could deteriorate the performance of the final amplifier.

The IF strip provides a 60dB AGC range which is more than adequate for all satellite receiver applications (see Fig.2).

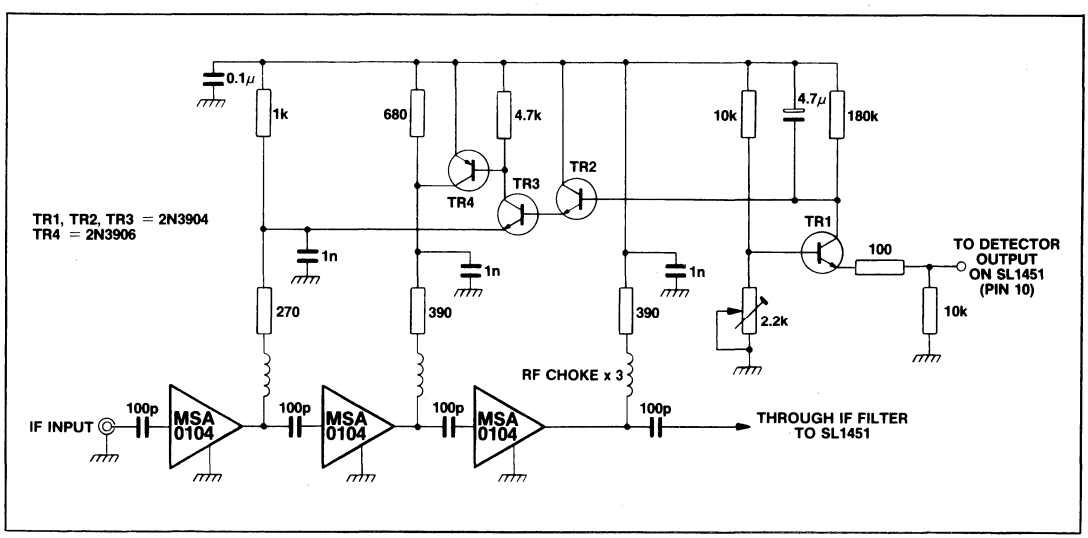


Fig.3 IF strip for satellite receiver, incorporating an AGC using the detector from the SL1451 (AGC range 60dB)

More Codes from the MV601

The MV500/MV601 form a remote control transmitter / receiver pair normaly giving 32 codes. Where more than 32 codes are required, there are various methods of obtaining more provided the use of a shift key is acceptable. Using this method , a single transmitter could be used to control two pieces of equipment, each requiring up to 32 codes. The shift function uses a latched switch on the transmitter to select a different transmission rate. Alternatively this same shift function can be utilised in a single piece of equipment with two modes of operation, for instance in a combined TV receiver and video recorder where the same set of transmitter switches could be used to control both TV and video recorder, reducing the complexity and cost of the transmitter circuit.

The most obvious method of acheiving this form of operation is to use an MV601 circuit for each 32 code set, and where a single transmitter is used for several equipments, this is essential. Selection of the various transmission rates is acheived simply by hard wiring the rate inputs on the MV601s to match the transmitter.

When a single piece of equipment with several operating modes is being designed, some economies in the circuit are possible as shown in the circuit diagrams Figs. 1-3. Fig. 1 shows a scheme which can use up to 3 MV601 circuits with 3 shift levels at the transmitter giving a total of 96 possible codes. The MV601 PPM inputs are connected in parallel to a single SL486 and only a single ceramic resonator is used since the oscillator output of one circuit can drive the oscillator inputs of the other two. Only a single RC time constant is required for power on clear as again these inputs can be connected in parallel. The outputs from the MV601 form a 15 bit bus which could be read by a microprocessor when interrupted by the combined data ready signal.

Fig. 2 shows a slightly modified system where the data ready outputs from each chip are connected to the output enable inputs forcing the data outputs into the high impedance state when no valid data is received. The data outputs of the three chips can now be connected in parallel since only one rate can be transmitted at any one time and only the receiver set to that rate will respond. Which chip is responding can be determined from the separate data ready signals.

When only a single shift function is required giving 2 sets of 32 codes, a simpler circuit using only a single MV601 is possible as shown in Fig. 3.

The pulse output from the SL486 is fed to the base of TR1, which provides an inverted lower impedance output applied to the MV601 PPM input. TR1 output is also fed to a simple filter, R2,R3 and C1 which produces a DC level dependant on the rate of received IR pulses. When the input rate is sufficient, the voltage rises to a level at which TR2 is switched on and TR3 off, taking the B rate input to the MV601 high. Using this method with automatic switching of the rate inputs dependant on the data transmission rate, the MV601 can be made to respond to the highest and lowest data rates selectable, provided care is taken with selection of the time constants in the SL486 pulse stretch circuit and in the filter components R2,R3 and C1. TR3 also provides the sixth output bit giving the indication of shift state. The values shown are correct for use with 500kHz ceramic resonators on the MV500 and MV601. At the fastest rate setting, when transmitting an all ones code, the SL486 pulse stretch capacitor should give approximately a 1:1 mark space ratio at the SL486 stretch output. Due to noise received by the SL486, the output from TR3 may bounce when no signal is transmitted, but provided the data is only used when data ready is true, the circuit operation should not be affected.

A transmitter circuit with single shift function giving 64 codes and suitable for use with the single MV601 application of Fig. 3 is shown in Fig. 4. An additional rate switch connected to pin 15 of the MV500 would allow the transmitter to be used with three levels of shift, providing up to 96 codes from the applications shown in Figs. 1 and 2.

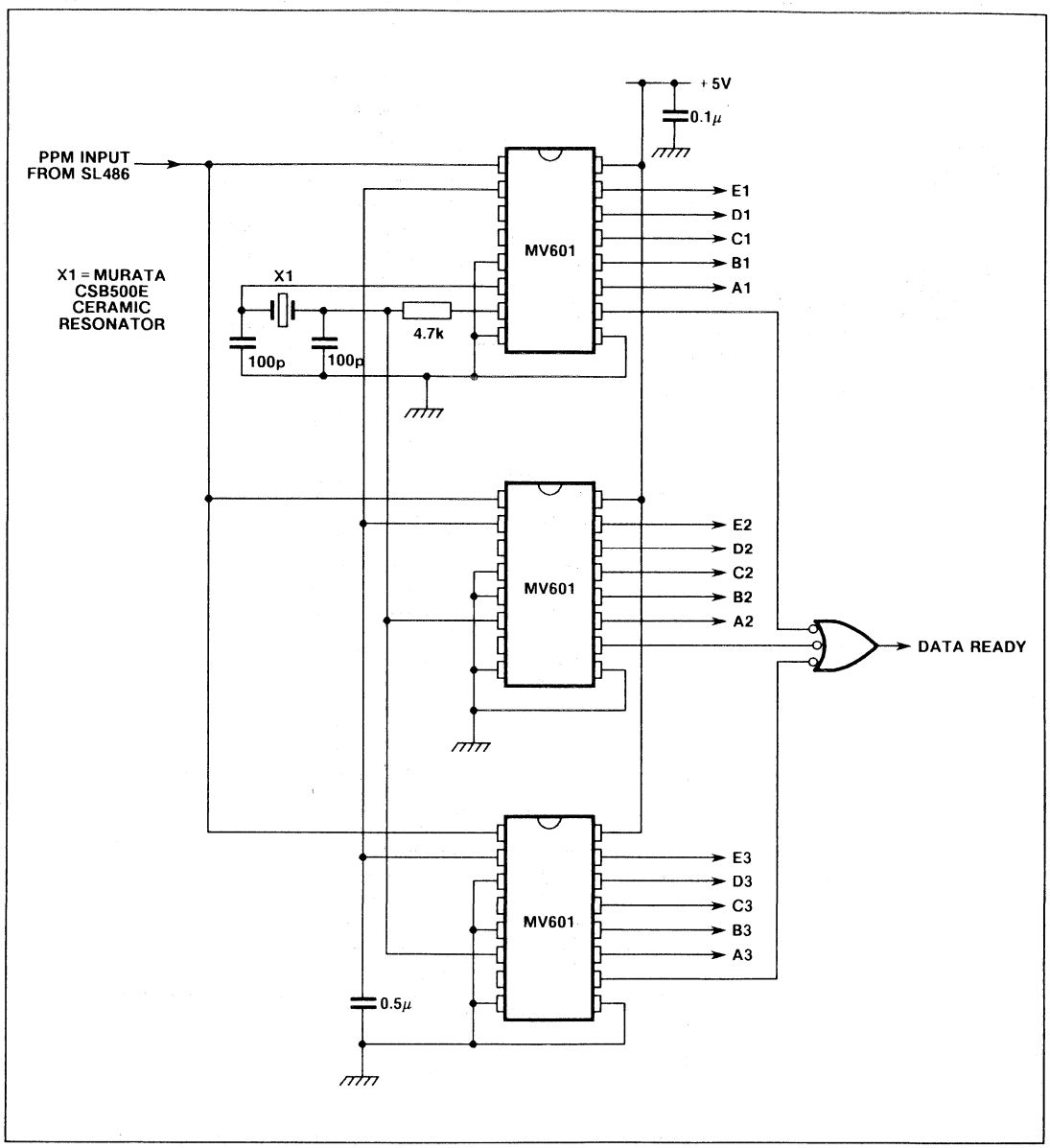

+5V
0.1μ
PPM INPUT
FROM SL486
X1 = MURATA
CSB500E
CERAMIC
RESONATOR
X1
4.7k
100p
100p
MV601
E1
D1
C1
B1
A1
MV601
E2
D2
C2
B2
A2
DATA READY
MV601
E3
D3
C3
B3
A3
0.5μ

Fig.1

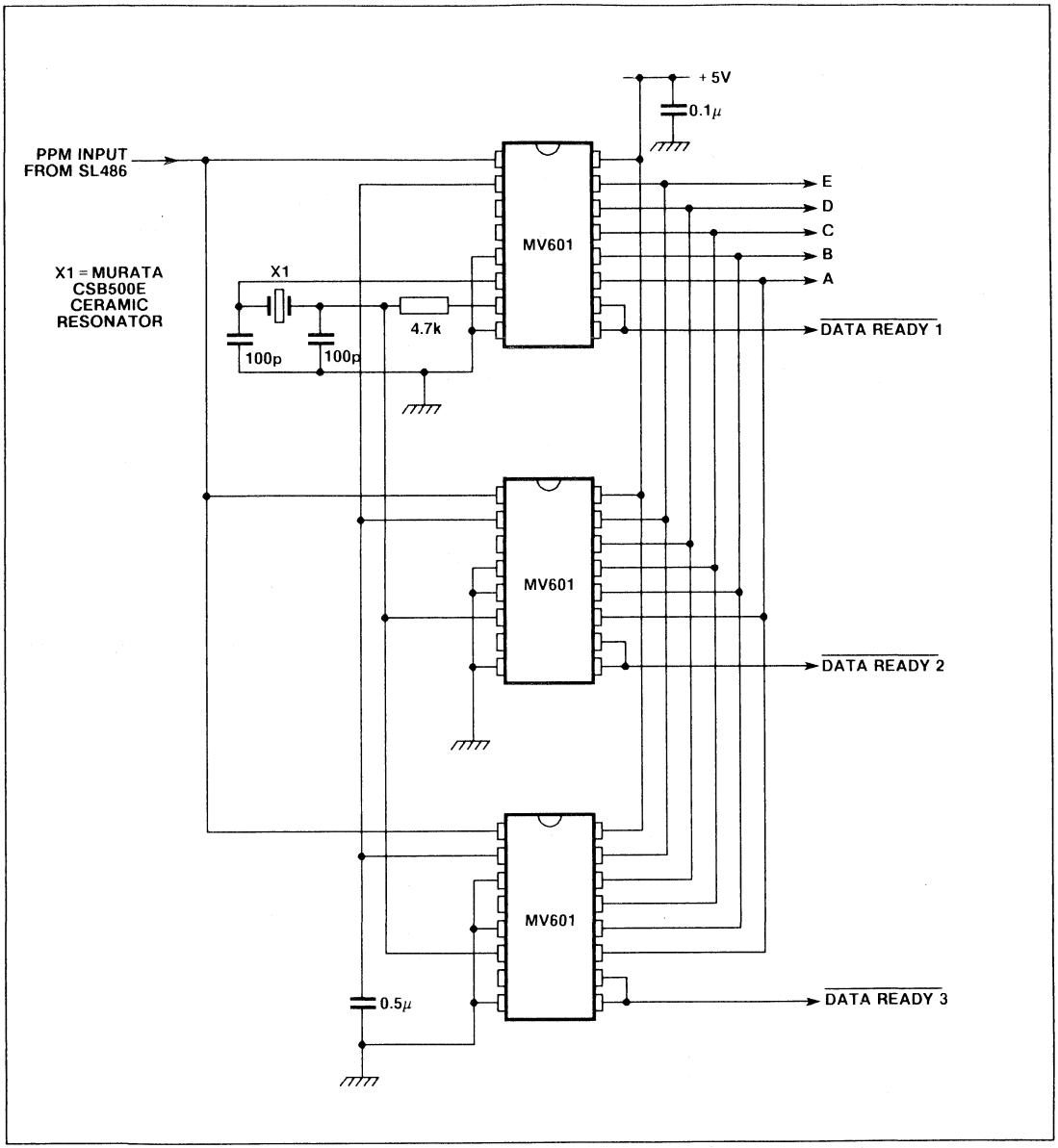

+ 5V
0.1μ
PPM INPUT
FROM SL486
X1 = MURATA
CSB500E
CERAMIC
RESONATOR
X1
100p
100p
4.7k
MV601
MV601
MV601
E
D
C
B
A
DATA READY 1
DATA READY 2
DATA READY 3
0.5μ

Fig.2

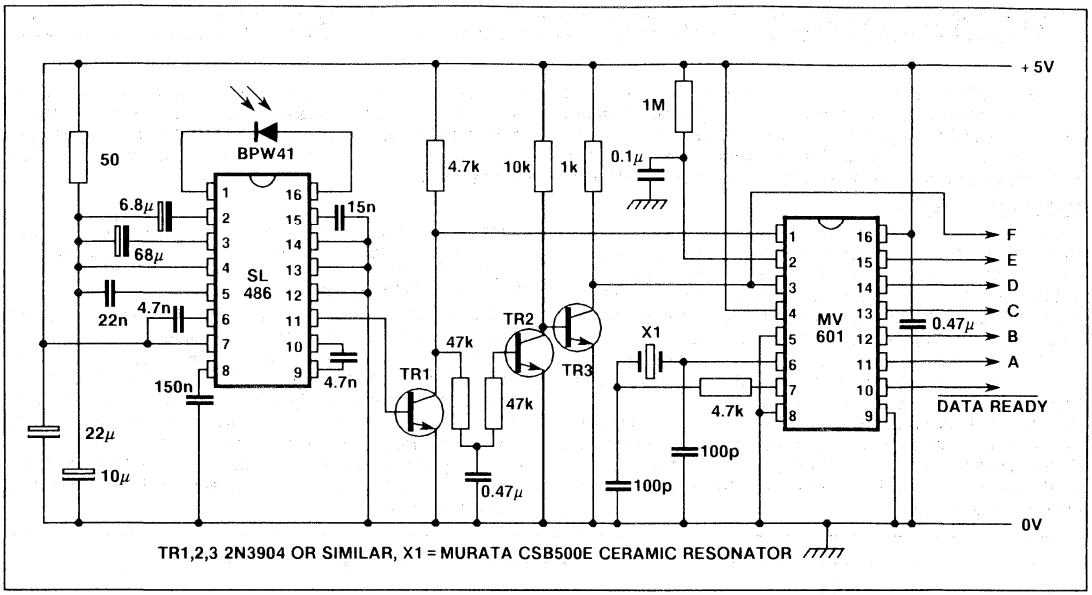

+ 5V
1M
50
BPW41
4.7k
10k
1k
0.1µ
6.8µ
68µ
22n
4.7n
15n
SL
486
4.7n
150n
22µ
10µ
47k
TR1
TR2
TR3
47k
0.47µ
X1
MV
601
0.47µ
F
E
D
C
B
A
DATA READY
4.7k
100p
100p
0V
TR1,2,3 2N3904 OR SIMILAR, X1 = MURATA CSB500E CERAMIC RESONATOR

Fig.3

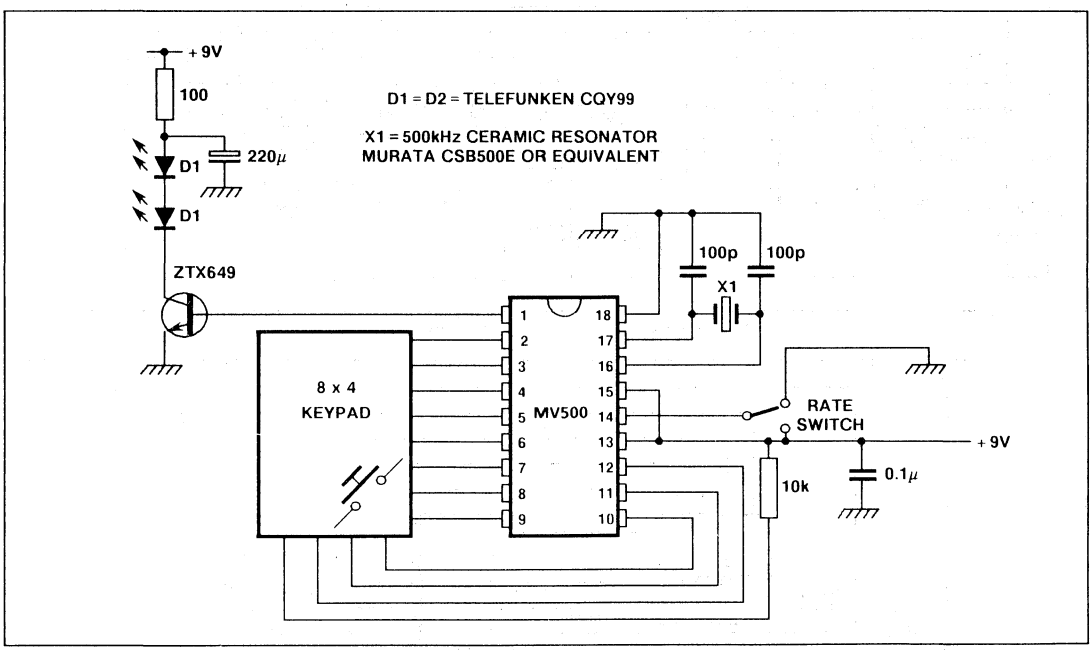

+ 9V
100
D1
220µ
D1
ZTX649
D1 = D2 = TELEFUNKEN CQY99
X1 = 500kHz CERAMIC RESONATOR
MURATA CSB500E OR EQUIVALENT
100p
100p
X1
8 x 4
KEYPAD
MV500
RATE
SWITCH
+ 9V
10k
0.1µ

Fig.4

MV500/MV601 Demonstration Boards

The MV601 is a general purpose remote control receiver, useful as a microprocessor interface and as an industrial controller for lighting, heating and ventilation fans etc. The demonstration board set, comprising a receiver board using an MV601 PPM receiver with an SL486 preamplifier and a transmitter board using the MV500 operating over an infra-red link, has been designed for the latter applications. The receiver board uses five LEDs to display the binary code of the key pressed on the transmitter board.

RECEIVER BOARD

Switches included on the receiver board (Fig. 1) allow various options to be selected, but in a typical application these would be replaced by hard wiring. Two single-pole switches control the rate inputs, which must be set to match those on the transmitter. The rate inputs on the MV601 have pull-up resisters to V_{DD} so they can be left unconnected where a high level is required. The use of the rate inputs, in combination with different ceramic resonator frequencies, allows units to be constructed to control several functions or to build matched receiver/transmitter pairs which would not interact when used in the same area. All the control signals and the ground connection are available via a 0.1in connector to enable easy microprocessor interfacing.

If the indicator LEDs are required, the $\overline{\text{OUTPUT ENABLE}}$ (pin 9) must be held low. Refer to the MV601 data sheet for rate switch settings.

TRANSMITTER BOARD

The MV500 transmitter board (Fig. 2) also has several features to allow greater flexibility of use; again these can be omitted in many applications. Two rate switches are provided to match those on the receiver. The resistors and capacitors connected to the rate inputs are only necessary when rate input switches are required; they prevent the rate inputs from floating during the switch change-over period. A 4×4 keypad provides 16 switches for transmitting the lower 16 codes, i.e., 00000 to 01111. Refer to the MV500 data sheet for rate switch settings.

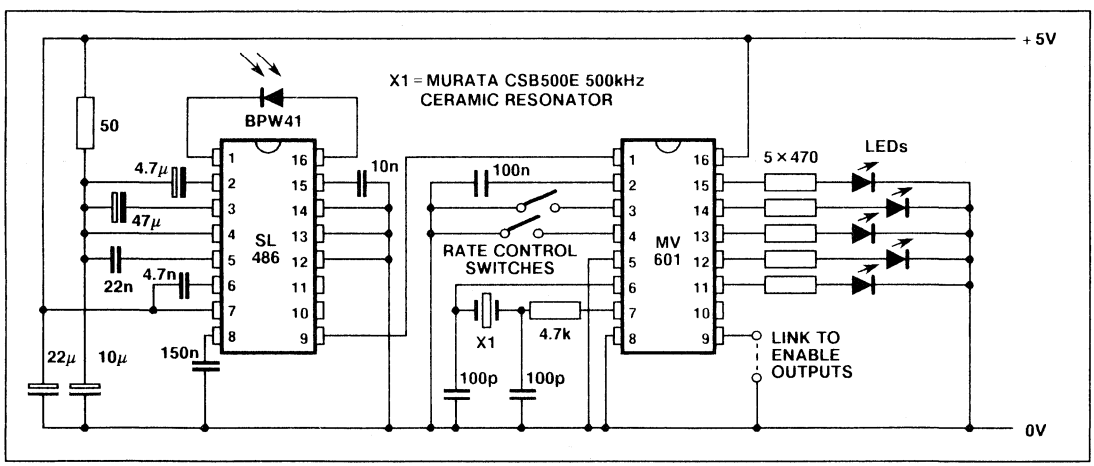


Fig.1 MV601 demonstration receiver circuit diagram

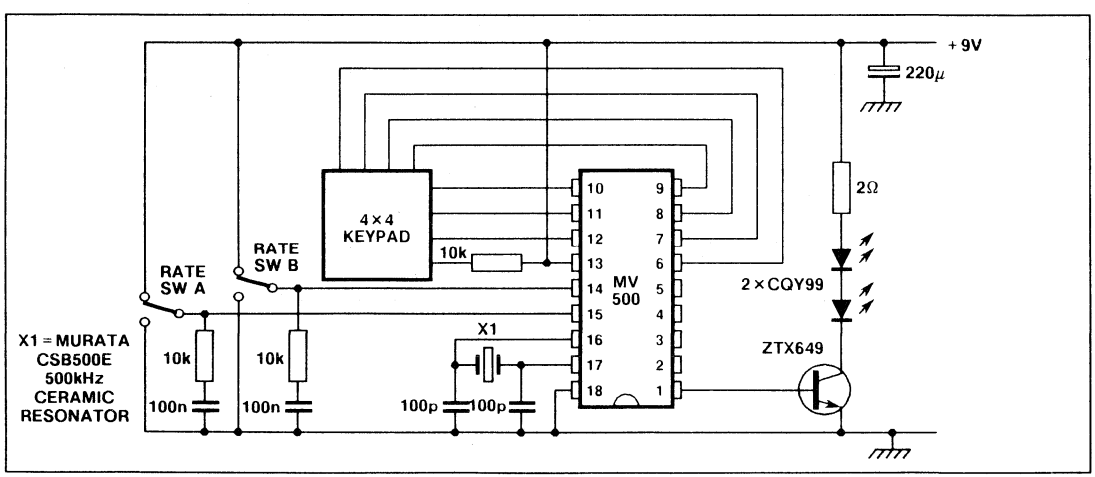


Fig.2 Circuit diagram or demonstration transmitter with variable rates

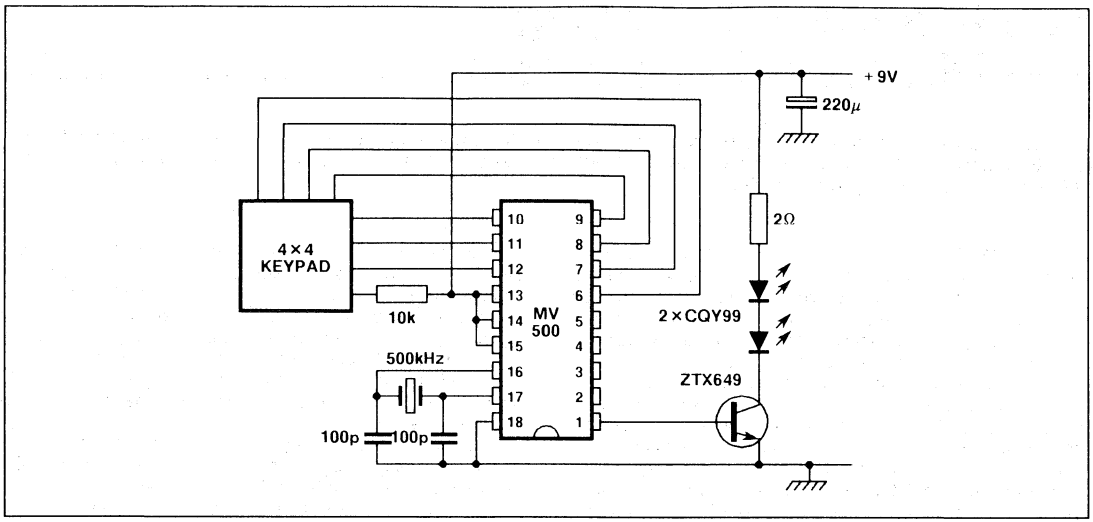


Fig.3 Circuit diagram of transmitter with fixed rate inputs

SL486 Infra-red Ranging and Directional Information

AB19

There is a requirement in many situations for a receiver to obtain ranging and directional information from a remote transmitter. This note describes how the SL486 may be used to provide this information. A block diagram of the ranging system is shown at Fig. 1.

The SL486 is a high gain pre-amplifier designed to form an interface between an infra-red receiver diode and the digital input of remote control receivers. The device contains two other circuit elements, one to provide a stretched output pulse facility and a voltage regulator to allow operation from a wide range of supplies.

The infra-red ranging application utilises the automatic gain control (AGC) decouple output on pin 8 of the SL486. 20ms bursts of 100kHz infra-red radiation are received by the SL486. These bursts produce an AGC voltage as shown in figure 2a.This voltage waveform has a variance of 300mV on a DC level. The 300mV signal varies with range and it is this signal which is used to provide the ranging information. The DC level varies slightly around 2V with changes in the surrounding light level, and so an ambient sample and hold is necessary to maintain an ambient reference level.

A synchronising pulse generator is edge triggered from the buffered AGC signal to provide a sample pulse for the ambient sample and hold circuit.

This synchronising pulse is also used to drive the sample pulse generator which produces a short duration sample pulse for the output sample and hold stages.

With the ambient infra-red level subtracted from this signal, a pulse is extracted from the resulting waveform to give a 10ms wide pulse whose height corresponds to the distance from the remote transmitter. This pulsed voltage is sampled and held to give a DC voltage level which represents range.

In order for directionality to be achieved at the receiver station, two ranging systems are used in parallel; with the receiving diodes mounted at 90° to each other.

The system's open loop range may be limited to a desired maximum operating range by simply altering a parallel resistor value on the receiver diode.

The operation of the system is illustrated in Fig. 2 in terms of the circuit waveforms.

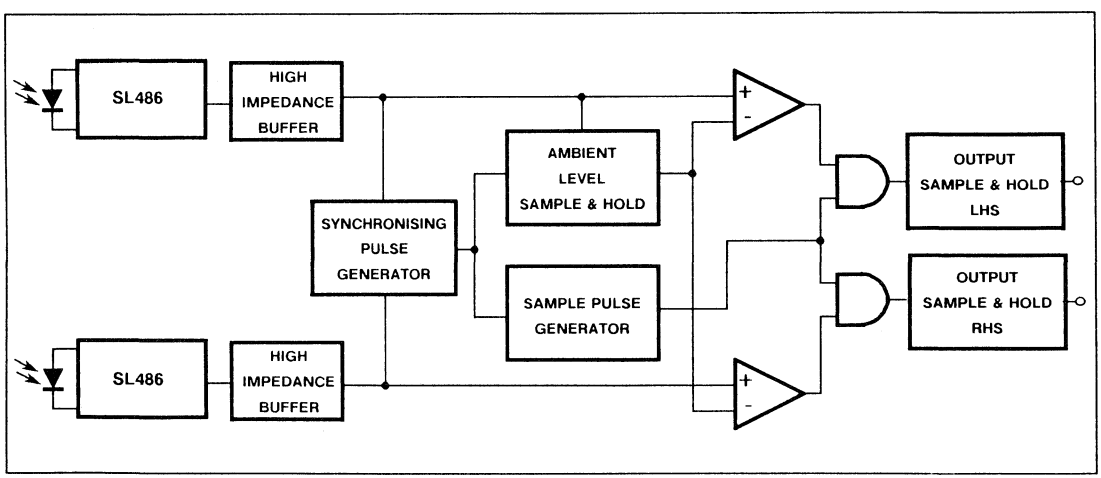
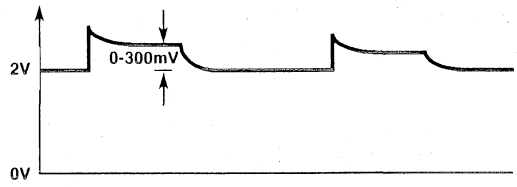


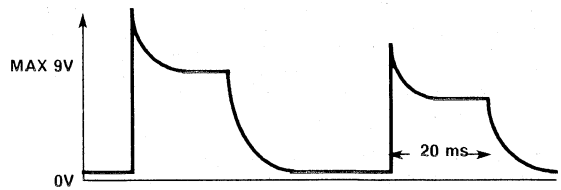
Fig.1 System block diagram

a. This buffered AGC output waveform is the system's starting point. The buffer is necessary to prevent loading of the SL486 AGC pin.



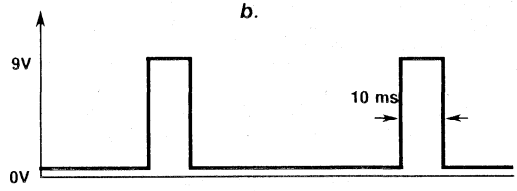
a.

b. With the 2V ambient level subtracted and the result amplified, this waveform is obtained. The shelf height is proportional to range.



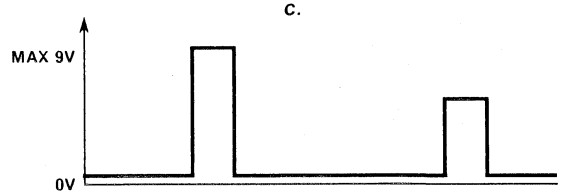
b.

c. This sample waveform is generated so that the shelf in b. may be extracted.



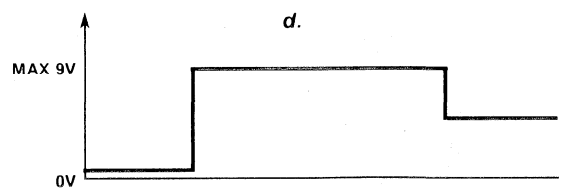
c.

d. The result of AND'ing together b. and c. produces this waveform whose pulse height represents range. This may then be sampled and held.



d.

e. This sample and held dc level is proportional range from the transmitter. A strong signal represents closer proximity.



e.

Fig. 2. System waveforms

MA818: A Microprocessor Controlled Digital PWM Motor Control IC

With a growing trend towards microprocessor control of pulse width modulated AC motor drives, GEC Plessey Semiconductors introduces the first fully digital stand-alone PWM generator IC for use in such drive units.

AIM

Several manufacturers have for some years been producing analog pulse width modulated (PWM) generator circuits for use in drive systems. These rely upon potentiometer control of parameters such as speed, acceleration and deceleration rates, pulse deletion and pulse delay (underlap) times. However, a growing demand has emerged in the drives market for digitally controlled drive units with direct keypad entry of operating parameters, and often with the ability to communicate with external computers/ controllers.

To this end, GEC Plessey Semiconductors have produced the first fully digital PWM generator IC family incorporating an industry standard microprocessor interface to produce full feature motor control with minimal hardware and software overhead whilst giving unprecedented stability, accuracy and speed range.

In addition, this low cost solution can be software configured to be used with the whole spectrum of power switches (including silent operation with fast switches) and also incorporates DC injection braking capability.

PULSE WIDTH MODULATION TECHNIQUES

The process of pulse width modulation is shown in Fig. 1. The desired power waveform is compared to a triangular waveform of considerably higher frequency and slightly greater amplitude (termed the *carrier waveform*). The intersections of these two waveforms dictate the digital transitions of the PWM output.

The voltage swings of the digital PWM output are stepped up by a power switch stage (see later) before being fed to the machine. The inherent low-pass characteristic of the machine will filter out the high frequency components due to the chopping behaviour, leaving the desired power waveform only.

The MA818 (and family) use a very similar process to that described above, but differ in the sampling of the desired waveform, as shown in Fig. 2. Since the devices use a digital implementation of the PWM process to increase stability and reduce drift problems, the desired waveform is sampled at the peak and trough of the triangular carrier waveform. This is termed *double edged regular sampling*. The comparison of the two waveforms is still carried out on a continuous basis however. The MA818 has three such PWM channels working simultaneously to produce the required outputs for a three phase machine, each being transposed 120°from the next.

The process described above is *asynchronous*, that is, the carrier frequency is set independently and is therefore not necessarily a fixed multiple of the desired frequency (which is varying). This allows for easy interfacing of the MA818 to the power electronics.

The alternative approach - *synchronous PWM* - locks the carrier frequency to an exact integer multiple of the power frequency . This implies that the carrier frequency varies directly with the power frequency which would make interfacing to the power electronics considerably more difficult, and in some cases, impossible.

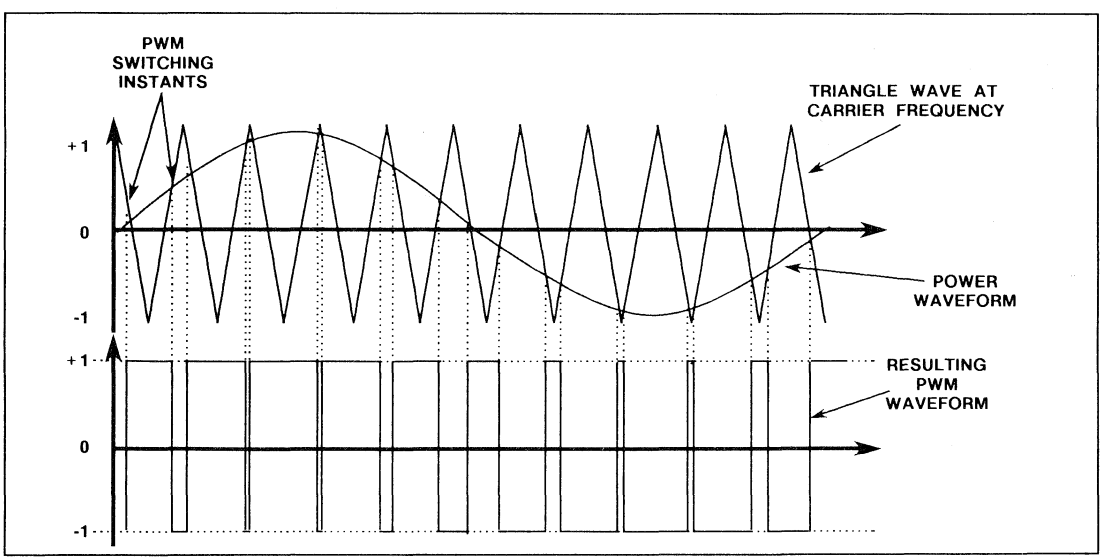


Fig.1 Natural PWM as used in analog implementation of the process

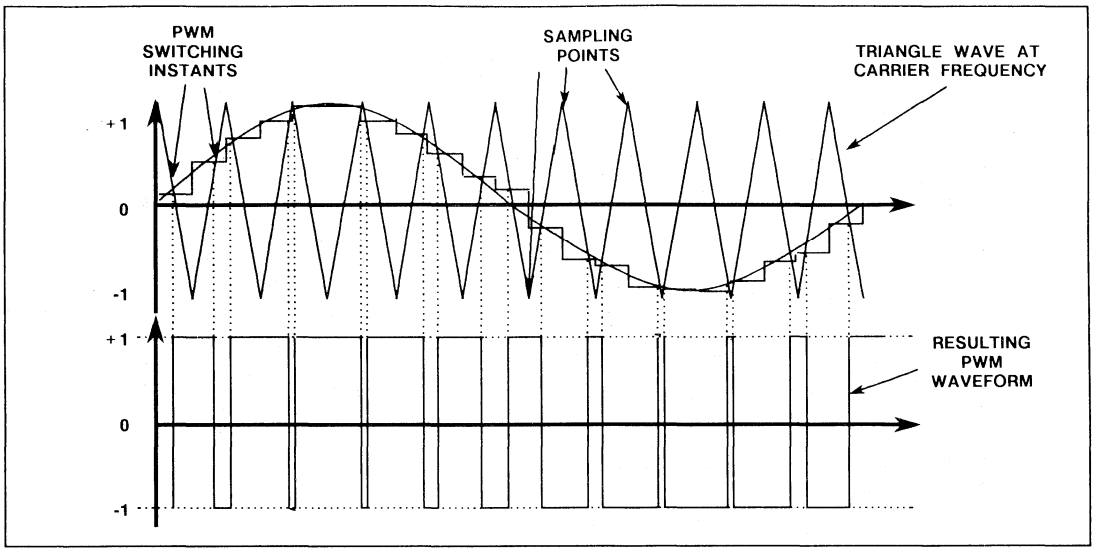


Fig.2 Asynchronous PWM generation with 'double-edged' regular sampling as used on the GPS PWM family

FUNCTIONAL DESCRIPTION

Microprocessor Interface

The block diagram in Fig. 3 shows the internal architecture of the MA818. The device is controlled via an 8-bit industry standard microcontroller/ microprocessor interface. Decode logic has been integrated on-chip so that no 'glue-logic' is required between the microprocessor and the MA818. The device also features a novel 'bus identifier' which automatically adjusts the interface to accept Motorola or Intel machine cycle formats with no user intervention. This is referred to as a MOTEL* interface. Microprocessors such as the 8085, 8088 etc. can be used directly with the device as can microcontrollers such as the 8051 and 6805.

Full chip select and read/write strobing inputs are provided and in addition a reset line allows the user to return the device to a known condition at any time.

The whole device, with the exception of the microprocessor interface, is timed via the clock input. The clock will normally be generated from a crystal of up to 12.5MHz to ensure good temperature and ageing characteristics.

It should be noted that the microprocessor interface is entirely independent of the clock generator circuit such that the microprocessor can load all parameters asynchronously.

Internally, the device has a series of registers which may be written to directly from the interface . These are used to tailor all aspects of the PWM output pulses, including carrier frequency, pulse deletion, pulse delay and rotational speed. This gives cost advantages both in terms of component savings and in allowing the same circuit to control a number of different motor drives simply by changing the microprocessor software.

Carrier Frequency

The carrier frequency, i.e. the frequency of the triangular waveform is derived directly from the master clock input according to the contents of the Initialisation Register. Carrier frequencies up to 24kHz are available to allow the use of the entire spectrum of power switches from fast MOSFETs and IGBTs (at ultrasonic carrier frequencies) down to bipolars at low carrier frequencies. If a different carrier frequency is required, the crystal frequency may be changed.

Power Frequency Range Selection

The power frequency range (that is, the frequency range of the desired power output waveform) can be selected via the Initilisation Register and is also a direct function of the carrier frequency. As a result, a 'sliding scale' is implemented giving power frequency ranges from 0 to 1.95Hz up to 0 to 4000Hz, depending upon the choice of carrier frequency. Hence an unprecedented range of frequencies can be selected. In fact there are forty-two combinations of carrier frequency and power frequency range.The power frequency range also serves to limit the maximum frequency supplied to the motor to provide a safe operating range.

Rotational Frequency Control

The actual frequency at which the waveform is emulated is governed by a 12-bit binary word, written directly to the MA818 by the micro. In addition, a sign bit is provided which changes the phase sequence from R-Y-B for forward rotation to B-Y-R for reverse rotation. Hence an effective 13 bits of speed control is achieved. This, in combination with the power frequency range control mentioned above gives speed control from $\pm 500\mu$Hz to $\pm$4000Hz without reconfiguring hardware, giving over 300 000 selectable speeds.

* *MOTEL is a registered trademark of Intel Corp. and Motorola Corp.*

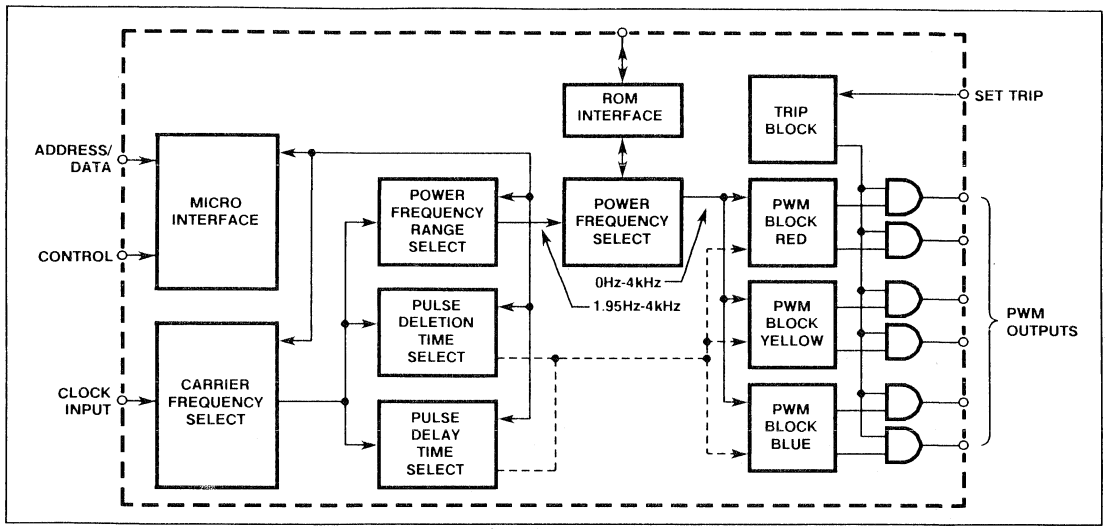


Fig.3 Block diagram of the MA818

Zero frequency may always be selected irrespective of the carrier frequency and power frequency range to provide a 'rotor retention' or DC injection brake facility. This is of particular use in machine tools where the work may be held perfectly stationary with no risk of run-on.

Power Waveform

The desired waveshape is read from an external ROM or EPROM in order that it may easily be changed to suit specific requirements. This ROM is connected directly to the MA818 via dedicated pins. No other circuit elements are necessary – all addressing and decoding is done on-chip.

Only the positive half-cycle of the waveshape is stored in order to minimise the size of the ROM. Hence the only limitation placed on the waveshape is that it must be symmetrical about the 180° axis- see Fig. 4.

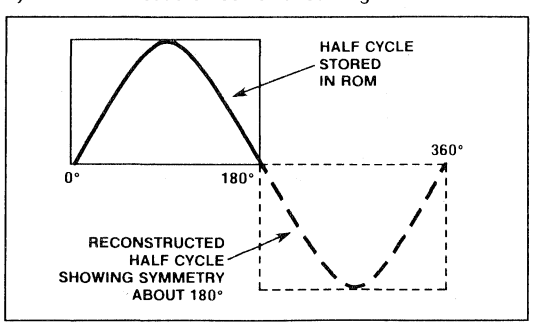


Fig. 4 Reconstruction of full cycle from ROM

For the vast majority of applications two specific wave shapes are sufficient:

1. Pure sine wave. Used in applications where waveform purity is of particular importance.
2. Sine wave with third harmonic superimposed at one sixth the amplitude of the fundamental.

Due to inverter operation it can be shown that the maximum achievable output from a PWM system such as this is only 86.6% of the input voltage swing. This clearly does not make for an efficient system and inevitably leads to motor derating.

In order to make full use of the input voltage swing it would be necessary to increase the output voltage to 1/0.866 = 1.154 of its nominal value - i.e. an increase of 15.4%.

This is achieved by adding an attenuated third harmonic component as shown in Fig. 5.

Fig. 5a shows the two individual frequency components and Fig. 5b shows the composite signal when they are summed. The phase output voltage remains unchanged but the line voltage is now increased by 16.7% due to the cancellation of cophasal (odd triplen) harmonics in a three phase system (as shown by the dotted line of Fig. 5b).

This increase in performance is obtained with no increase in harmonic component of the output due to the harmonic cancellation effect.

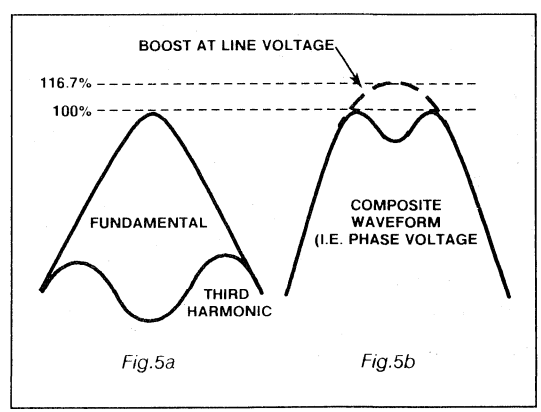


Fig.5 Construction of composite phase voltage

AMPLITUDE CONTROL

In the majority of drive applications, two particular kinds of amplitude response are required, as shown below in Fig. 6.

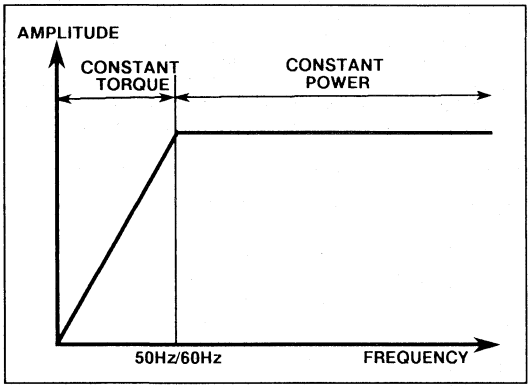


Fig. 6a Amplitude response for motor control

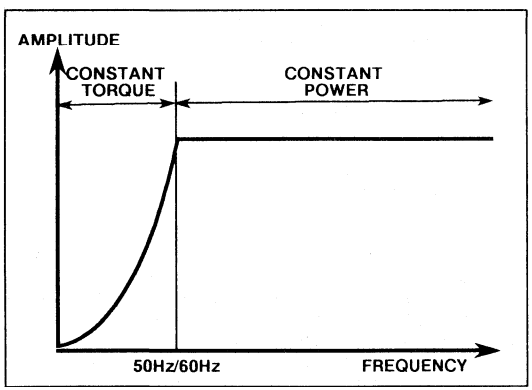


Fig. 6b Amplitude response for fan control

If the device is to be used with a motor load, a curve such as that shown in Fig. 6a will be required. Alternatively, if a fan load is used a square-law curve such as Fig. 6b should be used.

Successive 8-bit amplitude words can be written to the MA818 from the controlling microprocessor in order to reproduce these curves, or for that matter, any complex amplitude function. Usually, these curves will be retained in a small look-up table within the microprocessor memory and the amplitude will be changed whenever the power frequency is altered.

If the device is to be used as part of a switched mode power supply, uninterruptible power supply or any other waveform generator application, a constant amplitude will generally be required. In this case the amplitude word will be set to full scale at all times.

Pulse Deletion / Pulse Delay

Fig. 7 shows the typical inverter network used in three-phase PWM systems.

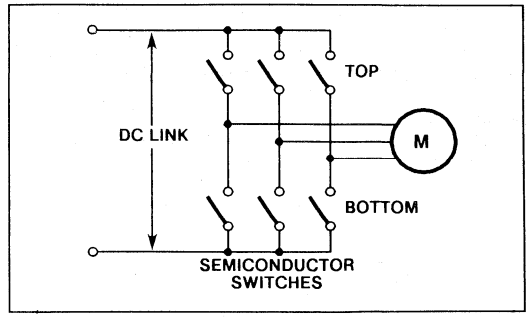


Fig. 7 Three phase power bridge

It is essential when firing the switches in a network such as that in Fig. 7 to ensure that both switches in any one vertical arm are off before one switch can be turned on. If this rule were not obeyed there would be a risk of *shoot-through* i.e. a dead short across the DC link when both switches are on simultaneously. Such a scenario would inevitably arise if the sense of both switches in an arm was changed simultaneously due to the finite turn-off time associated with semiconductor devices.

To circumvent this problem, the MA818 allows for a pulse delay or 'underlap' time when neither switch is enabled. When sufficient time has elapsed to ensure that both switches are fully off, another change of state is allowed. The net result of this is a quasi-complementary pulse train to the top and bottom switches rather than being strictly complementary. Fig. 8 shows the effect on a 'pure' PWM pulse train of pulse delay. The delay period can be predetermined by writing one byte to the MA818 and is also a function of the carrier frequency in order to provide a very wide range of values for all types of power switches. The range of delay times exceeds 4000:1.

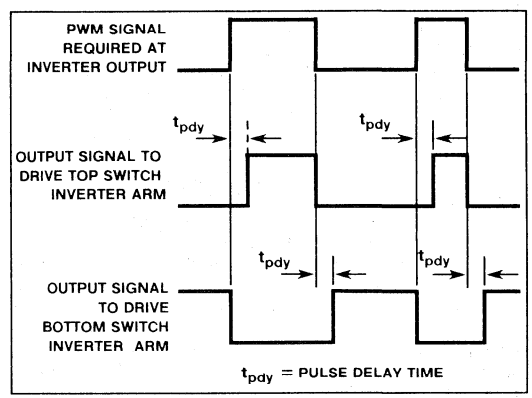


Fig. 8 Effect of pulse delay on PWM pulse train

The power dissipation of the power switches is largely dependent upon the number of switching events which the power devices have to endure in a given time. In order to minimise these losses, the MA818 deletes all pulses in the train of less than a pre-determined period. In this case no change of state will occur and the switching loss is reduced.This time is generally selected to correspond with the period of time taken for the power switch to turn on and immediately off again. Fig. 9 shows the effect of pulse deletion diagramatically.

The pulse deletion time is selected by writing one byte to the IC in the same way as pulse delay.

Other Features

The MA818 features six PWM outputs corresponding to the top and bottom switches of three phases. In addition, the device includes a low-going TTL signal to indicate the zero-crossing point (i.e. 0° point) of the red phase. This may be used to provide closed-loop speed control and is of particular use in slip compensated systems.

Another useful feature incorporated into this device is an emergency trip. The SET TRIP pin, when taken high, acts to disable all the TTL outputs without software intervention, effecting an immediate shutdown of the power electronics. A TRIP acknowledge signal is provided for monitoring purposes.

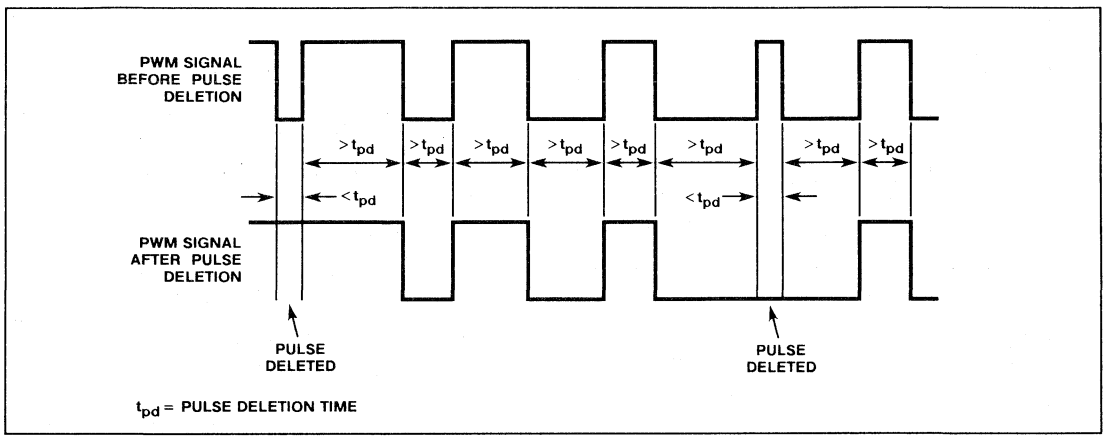


Fig. 9 Effect of pulse deletion on PWM pulse train

APPLICATIONS

Fig. 10 shows a typical application circuit for the MA818 in a drive system. Generally, a microcontroller having on-chip ROM and RAM will give a minimum component system, whilst still having enough I/O port lines to directly interface to the keypad, display and watchdog inputs.

Alternatively, a microprocessor can be used with separate ROM, RAM and I/O ports.

Clearly, it is possible to produce a working system using only three integrated circuits: a microcontroller, an MA818 and a waveform ROM. This represents a considerable saving in hardware development time compared to other alternatives.

Similar systems may be developed to provide soft start and dynamic braking using the MA818.

Note that once the various parameters have been written into the working registers within the MA818, the PWM sequence will begin and *no* further intervention from the microprocessor is required until, for example, the rotational speed needs to be changed. This frees the microprocessor to carry out other tasks , such as keypad scanning, display driving and watchdog functions. As a result of the small software overhead, the software development time and costs are considerably reduced.

The product range is backed up by a comprehensive range of literature, development hardware and software, including an Exercise Module operating from BASIC environment and a Demonstration Module containing typical software for use in a variable frequency drive environment. (All software is public domain and can be used in customer systems in order to reduce their development time). In addition, on line applications support is provided at all times to potential and existing customers.

The MA818 is available in production quantities and is currently designed into many commercial AC drives throughout the world.

FUTURE PRODUCTS

GEC Plessey Semiconductors has expanded its range of PWM generator ICs to include the MA828 family of devices. These are functionally identical to the MA818 but integrate the waveform ROM on-chip, thereby obviating the need for an external ROM. The MA828-1 is pre-programmed to emulate a sinewave plus superimposed third harmonic component whilst the MA828-2 emulates a pure sinewave. (Other waveforms may be supplied to order).

In addition a single phase version, the MA838, has on-chip ROM for use in motor control of white goods. This enables manufacturers to use a robust induction motor in preference to the traditional brushed universal motor thus making white goods inherently more reliable.

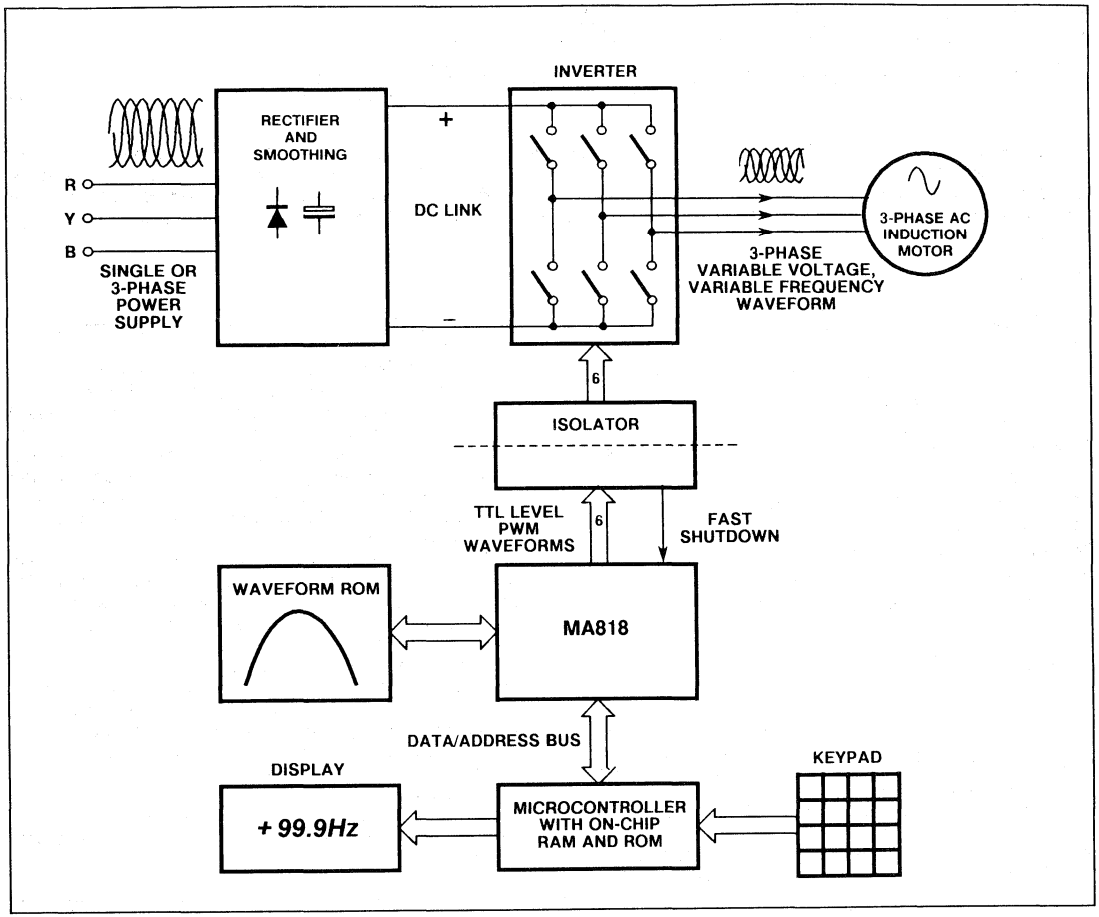


Fig.10 Typical AC drive incorporating an MA818

PWM Family: Three Phase Motor Drive Demonstrator Module

The PWM Family Demonstrator Module has been manufactured in order to minimise the hardware and software development time needed to integrate the MA818/MA828/MA838 PWM generator ICs into a variable speed motor drive system. It comprises an Intel 8031 microprocessor-based board with relocatable software, for easy adaptation to the user's specific requirements. The six PWM outputs can be connected to an inverter bridge via suitable isolation.

FEATURES

- Fully Digital PWM Generation
- Full Microprocessor Control
- Speed Variable between ±0Hz and ±4000Hz
- Software Programmable Acceleration and Deceleration Times
- Software Programmable Minimum Pulse Width and Underlap Times
- Direct Keypad Entry of Machine Parameters
- Full Display Capability
- RS232 Interface for Remote Control
- 'Jog' Facility to allow Machine Positioning
- Easily Interfaced to Inverter Bridge

GENERAL DESCRIPTION

The PWM Family Demonstrator Module has been manufactured in order to minimise the hardware and software development time needed to integrate the MA818/MA828/MA838 PWM generator ICs into a variable speed motor drive system.

It comprises an Intel 8031 microprocessor-based board with relocatable software, for easy adaptation to the user's specific requirements. The six PWM outputs can be connected to an inverter bridge via suitable isolation.

The board has two modes of operation, selectable via a DIP switch:

1. MAXMODE- Has full numeric keypad for data entry and a 32 character alphanumeric display.
2. MINMODE- Has ↑ and ↓ keys for speed control and a 4-digit LED display

All parameters are software selectable – including pulse deletion, underlap time, carrier frequency and maximium power frequency. The acceleration and deceleration times may be altered to match the nameplate values of the motor in question.

Both modes feature forward and reverse rotation to 12-bit accuracy between 0 and 4000Hz. Both fan and motor V/f curves are catered for and are software selectable. A variable boost voltage can be entered and, if necessary, the entire V/f curve can be altered.

The system incorporates a braking facility via the PWM generator and also a 'JOG' key to allow the machine to be inched into position. This may be of particular use in the machine tool industry where positioning is important.

An RS232 port allows the board, and hence the entire drive system, to be controlled from a remote source such as a mainframe or PC.

The system is supplied on a double-sided printed circuit board. Full software and documentation is supplied with each board.

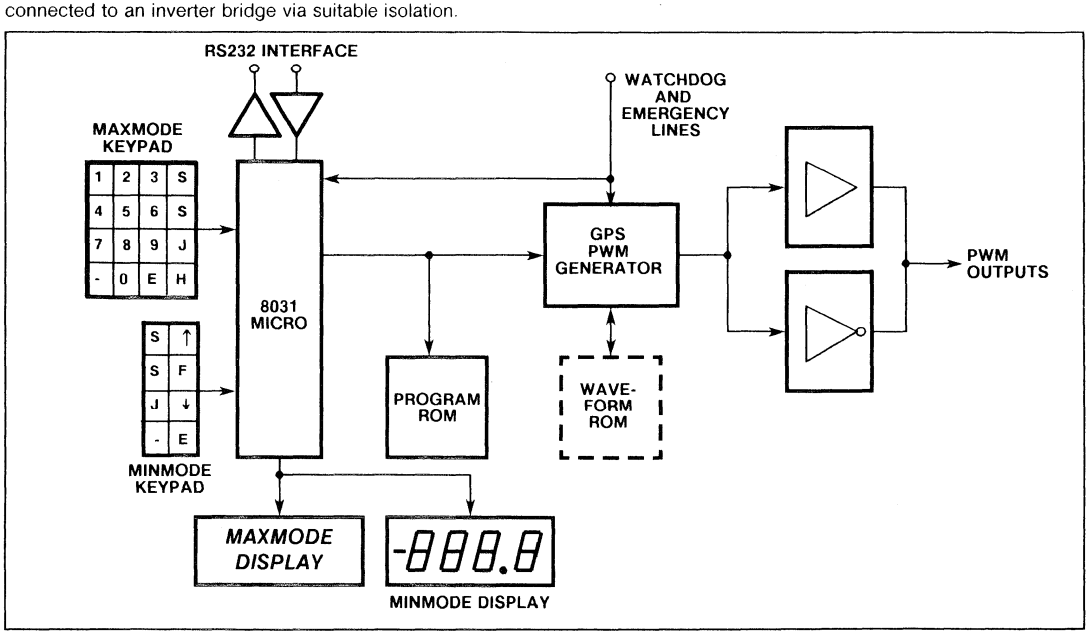
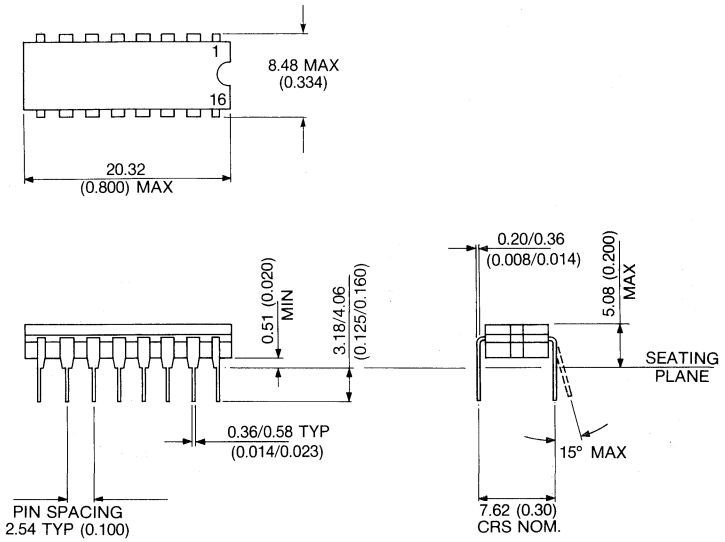


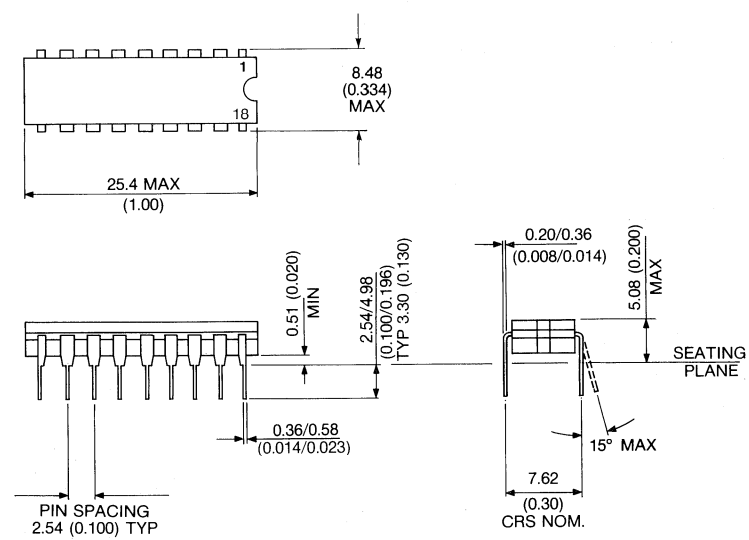
Fig.1 PWM family demonstrator board block diagram

Section 9
Package Outlines

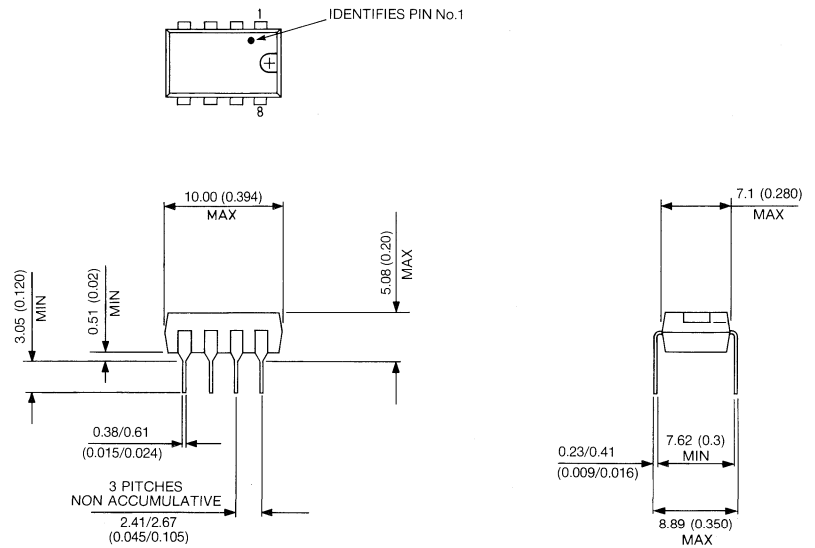
NOTE: On all package outlines, dimensions are shown thus: mm (in).



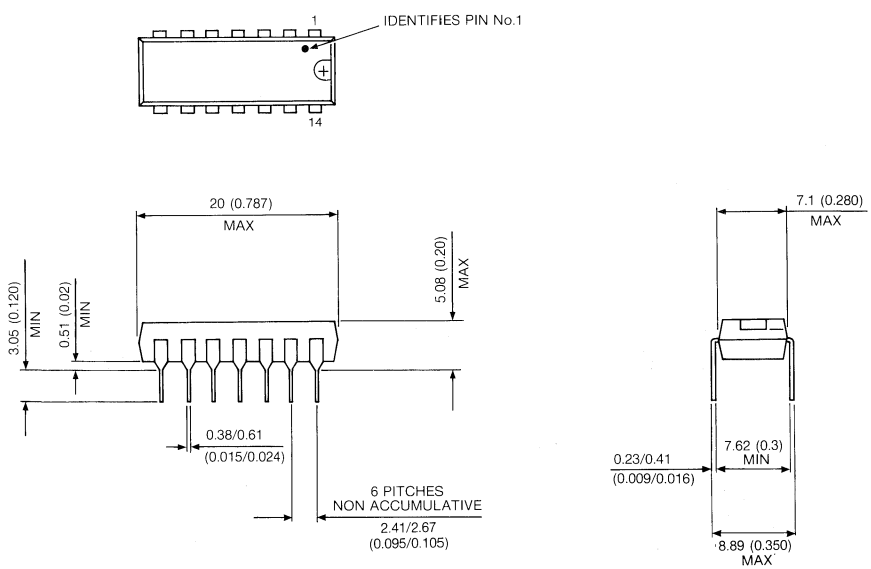
16-LEAD CERAMIC DIL - DG16



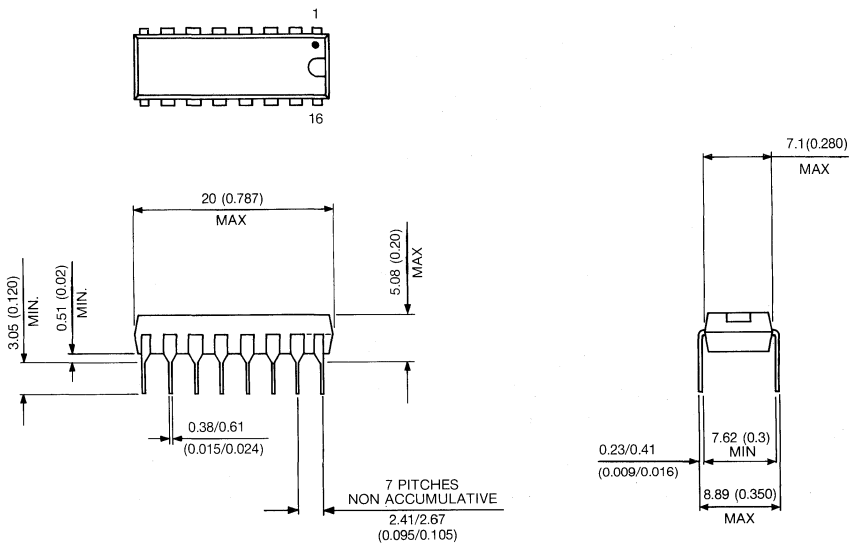
18-LEAD CERAMIC DIL - DG18



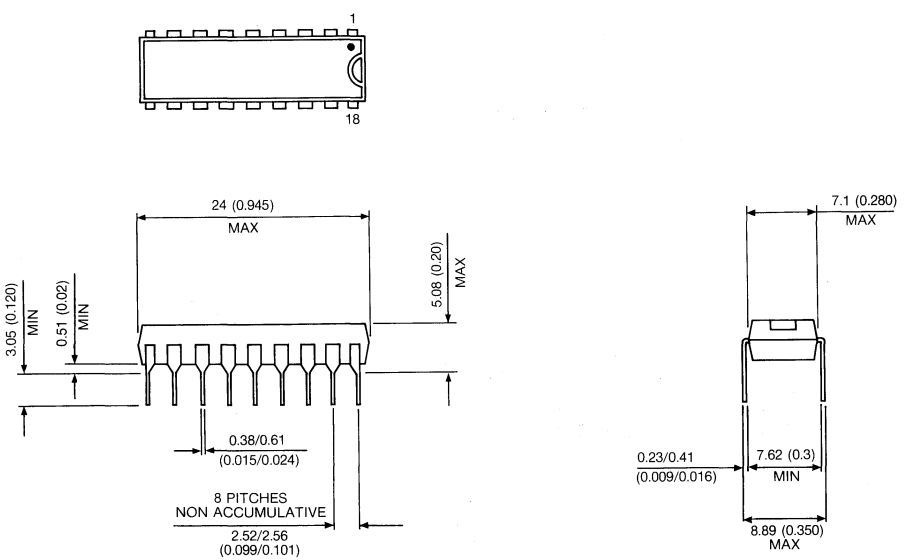
8-LEAD PLASTIC DIL - DP8



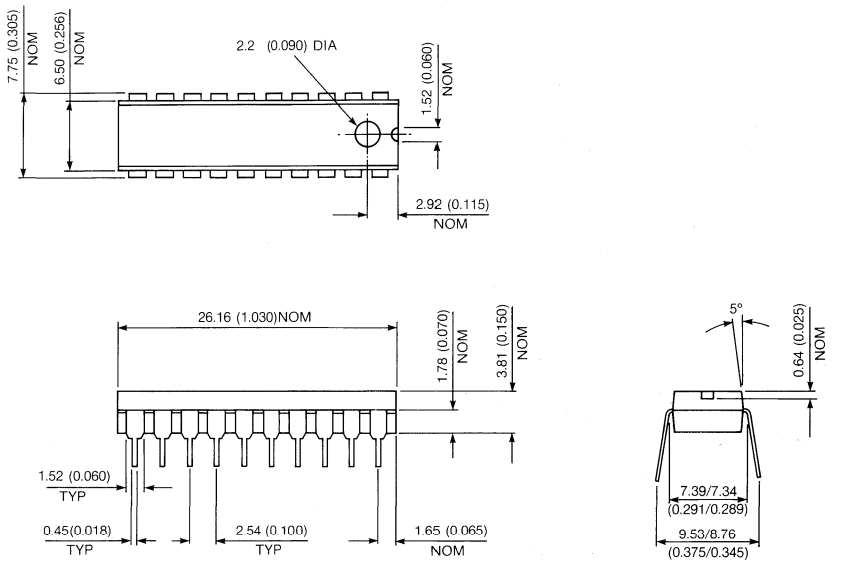
14-LEAD PLASTIC DIL - DP14



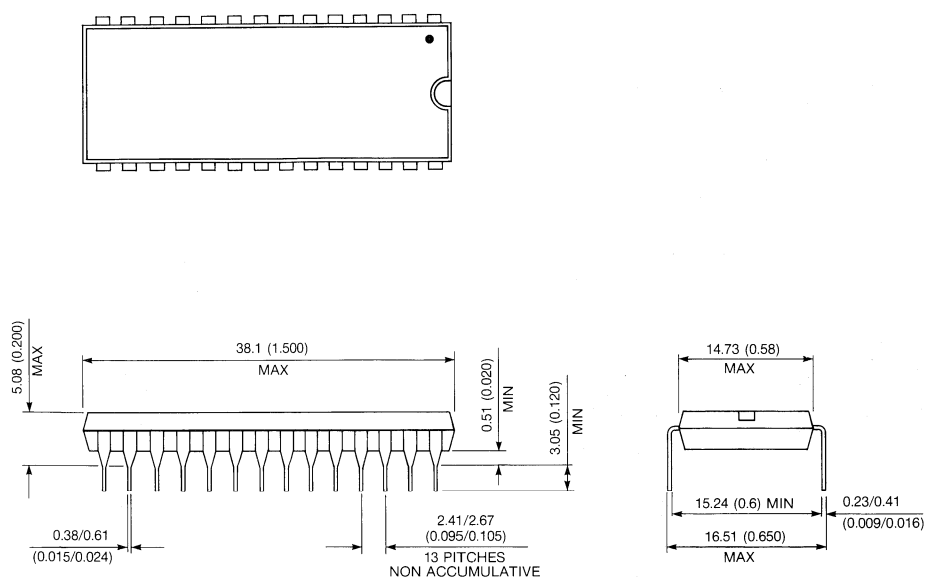
16-LEAD PLASTIC DIL - DP16



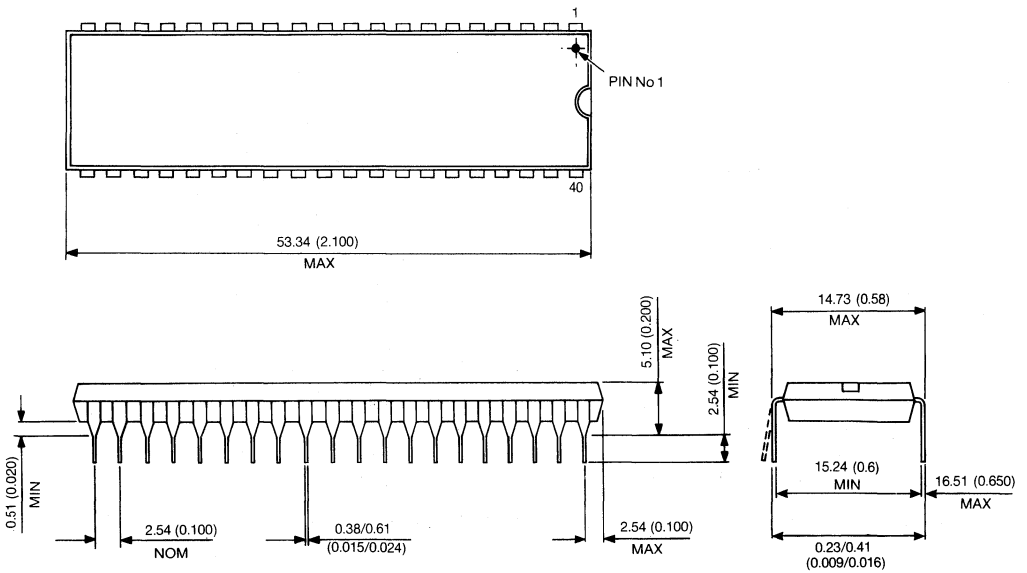
18-LEAD PLASTIC DIL - DP18



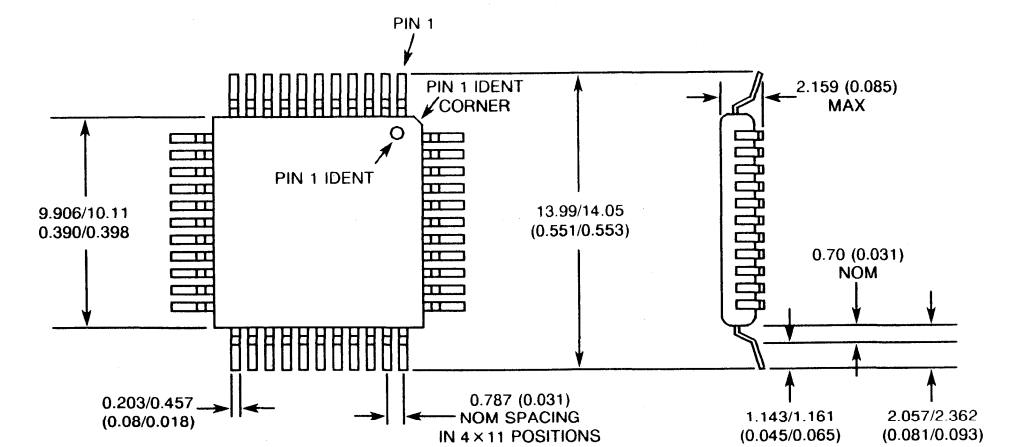
20 LEAD PLASTIC DIL – DP20



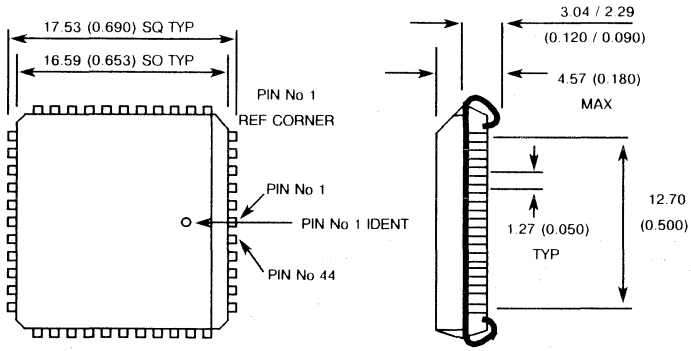
28-LEAD PLASTIC DIL - DP28



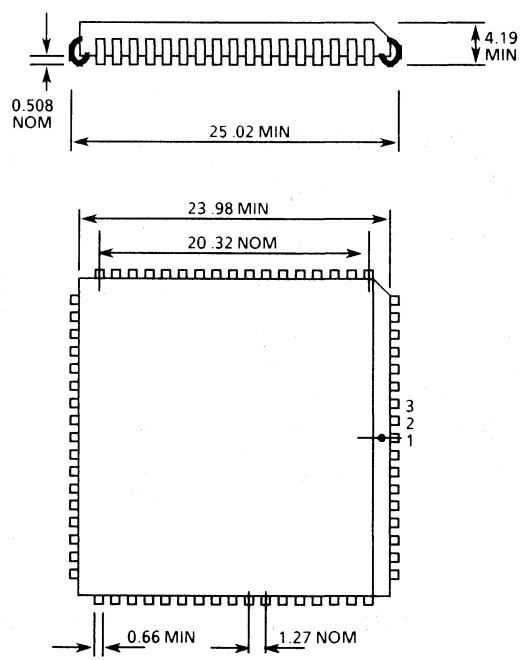
40 LEAD PLASTIC DIL - DP40



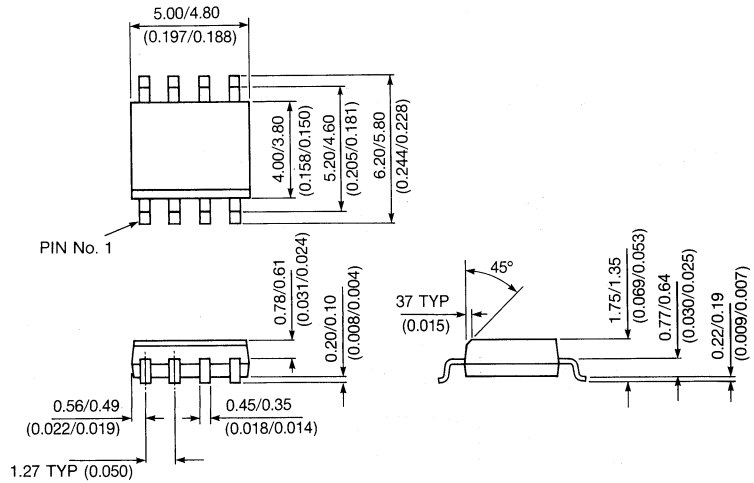
44-LEAD PLASTIC QUAD FLATPACK - GP44



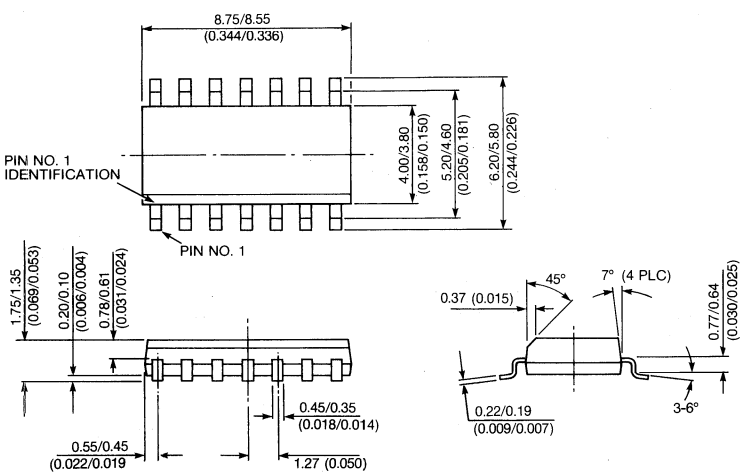
44 LEAD QUAD PLASTIC J LEAD - HP44



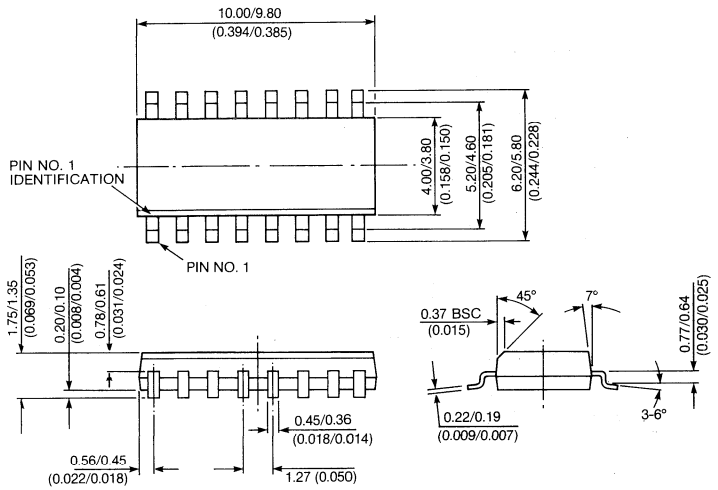
68-LEAD MOULDED PLASTIC J LEAD - HP 68



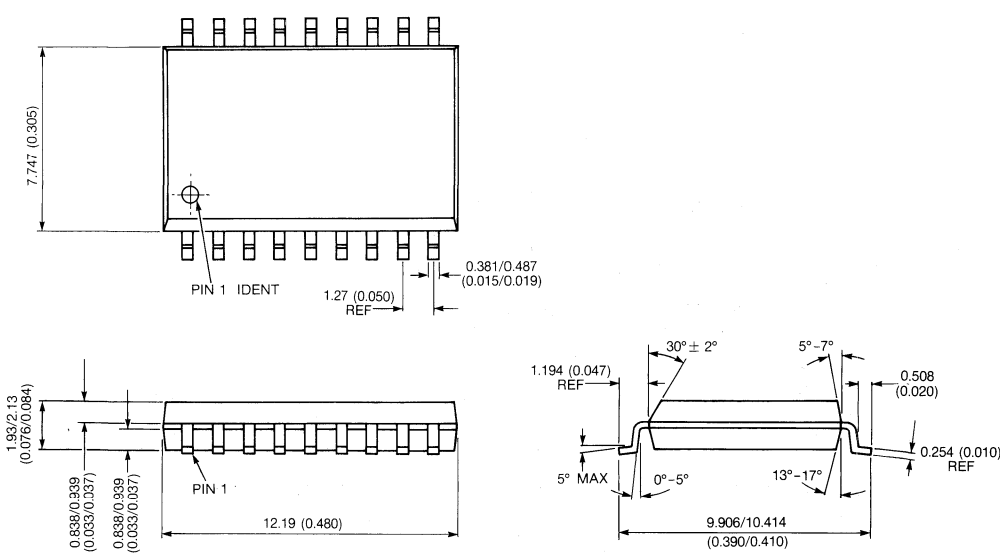
8-LEAD MINIATURE PLASTIC DIL - MP8



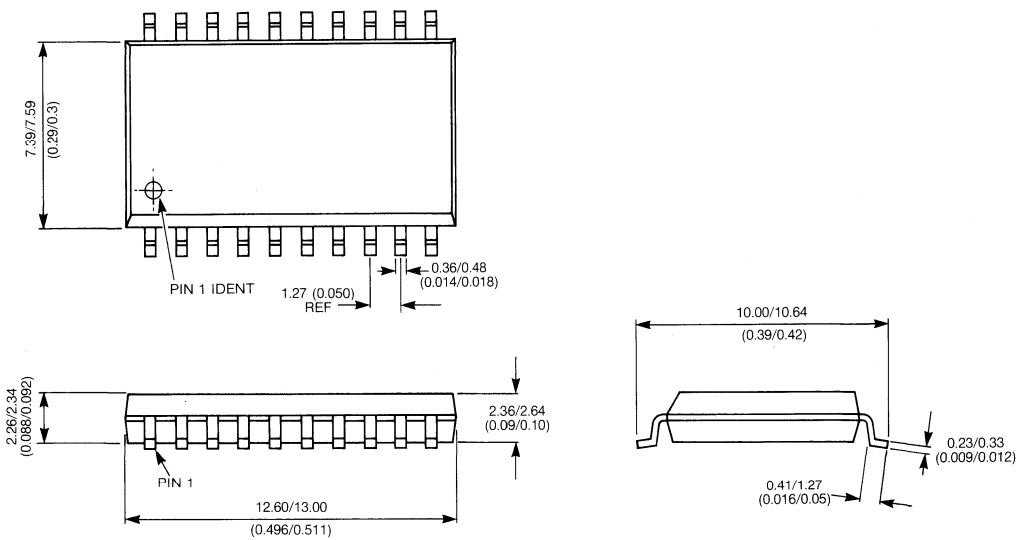
14-LEAD MINIATURE PLASTIC DIL - MP14



16-LEAD MINIATURE PLASTIC DIL - MP16



18-LEAD MINIATURE PLASTIC DIL - MP18



20-LEAD MINIATURE PLASTIC DIL - MP20

Section 10
Locations

HEADQUARTERS OPERATIONS

UNITED KINGDOM	Cheney Manor, Swindon, Wiltshire SN2 2QW, United Kingdom. Tel: (0793) 518000 Tx: 449637 Fax: 0793 518411
NORTH AMERICA	Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, USA. Tel:(408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576

CUSTOMER SERVICE CENTRES

FRANCE & BENELUX	Z.A. Courtaboeuf, Miniparc-6, Avenue des Andes, Bat. 2-BP 142, 91944, Les Ulis Cedex A. France. Tel: (1) 64 46 23 45 Fax: (1) 64 46 06 07 Tlx: 602 858 F
GERMANY, AUSTRIA and SWITZERLAND	Ungererstraße 129, 8000 Munchen 40, Germany. Tel: 089/36 0906-0. Fax: 089/360906-55 Tx: 523980
ITALY	Viale Certosa, 49 20149 Milano. Tel: (02) 33 00 10 44/45. Fax: (GR3) 31 69 04. Tlx: 331347
JAPAN	Nichiyo Building 6F, 11-12, Kanda - Mitoshirocho, Chiyoda-ku, Tokyo 101. Tel: (03) 3296-0281. Fax: (03) 3296-0228
NORTH AMERICA	**Integrated Circuits** Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, USA. Tel: (408) 438 2900 ITT Twx: 4940840 Fax: (408) 438 7023 **Microwave and Hybrid Products** 160 Smith Street. Farmingdale, NY11735, USA. Tel: (516) 293 8636 Fax: (516) 293 0061.
SOUTH EAST ASIA	152 Beach Road, #04-05 Gateway East, Singapore 0718. Tel: 2919291. Fax: 2916455
SWEDEN	Ostmästargränd 4, GS-12173 Johanneshov. Tel: 46 8 7228690 Fax: 46 8 7227879
UNITED KINGDOM and SCANDINAVIA	Unit 1,Crompton Road,Groundwell Industrial Estate, Swindon, Wilts SN2 5AY, U.K. Tel: (0793) 518510. Tx: 444410 Fax: (0793) 518582.

WORLD-WIDE AGENTS

AUSTRALIA and NEW ZEALAND	**GECGeorge Brown Electronics,** Unit 1, 38 South Street, Rydalmere, NSW 2116, Australia. Tel: 612 638 1888. Fax:: 612 638 1798
EASTERN EUROPE	**CTL Empexion Ltd..** Falcon House, 19 Deer Park Road, London SW19 3WX, U.K. Tel: (081) 543 0911. Tx: 928472. Fax: (081) 540 0034. **FA Bernhart GmbH,** Melkstattweg 27, PO Box 1628, D 8170 Bad Toelz., Germany. Tel: 80 41 41 676 Fax: 80 41 71 504 Tx: 526246 FABD.
HONG KONG	**YES Products Ltd.,** Block E, 15/F Golden Bear Industrial Centre, 66-82 Chaiwan Kolk Street,Tsuen Wan, N.T. Hong Kong. Tel: 4144241-6. Tx: 36590. Fax: 4136078.
INDIA	**Mekaster Telecom PVT Ltd.,** 908 Ansal Bhawan, 16 Katuba Ghandi Marg, New Delhi, 100 001 India Tel: 11 3312110 Fax: 11 3712155.
JAPAN	**Cornes & Company Ltd.,** Maruzen Building, 2-3-10 Nihonbashi, Chuo-ku. Tokyo 103. Tel: 3 272 5771. Tx: 24874. Fax: 3 271 1479. **Cornes & Company Ltd.,** 1-Chome Nishihonmachi, Nishi-Ku, Osaka 550. Tel: 6 532 1012.Tx: 525-4496. Fax: 6 541-8850. **Microtek Inc.,** Itoh Bldg, 7-9-17 Nishishinijuku. Tokyo 160. Tel: 3 371 1811. Tx: 27466. Fax: 3 369 5623.
KOREA	**KML Corporation,** 3rd Floor, Bang Bae Station Building, 981-15 Bang Bae, 3-Dong Shucho-Gu, Seoul, Korea, CPO Box 7981. Tel: 2 588 2011/6. Tx: K25981. Fax: 2 588 2017.
MALAYSIA	**Adequip Enterprise Sdn Bhd,** #6-01 6th Floor, Wisjma Stephens, 88 Jalan Raya Chulan, 50200 Kualar Lumpur, Malaysia. Tel: 2423522. Fax: 2423264.
SCANDINAVIA: Denmark	**Scansupply A/S,** 18 Nannasgade, DK-2200 Copenhagen N. Tel: 31 83 50 90. Tx: 19037. Fax: 31 83 25 40. **Scansupply A/S,** Marselisborg Havnevej 36, 8000 Arhus C. Tel: 45 86 12 77 88. Fax: 45 86 12 77 18.
Finland	**Oy Ferrado AB,** P.O.Box 54, SF-00381 Helsinki 38. Tel: 98 0550 002. Tx: 122214. Fax: 98 0551 117.
Norway	**Skandinavisk Elektronikk A/S,** Ostre Aker Vei 99, 0596 Oslo. Tel: 2 64 11 50. Tx: 71963 Fax: 2 643443.
TAIWAN	**King and King's Technology Ltd.,** 4, Alley 6, Lane 118, Ho Ping East Road. Taipei 10636. Taiwan, R.O.C. Tel: 02-738-9145. Fax: 02-738-9146.
THAILAND	**Westech Electronics Co. Ltd,** 77/113 Moo Ban Kitikorn, Ladprao Soi 3, Ladprao Road, Ladyao, Jatujak, Bangkok 10900. Thailand. Tel: 2 5125531. Fax: 2 2365949.

WORLD-WIDE DISTRIBUTORS

AUSTRALIA	**GECGeorge Brown Electronics,** Unit 1, 38 South Street, Rydalmere, NSW 2116, Australia. Tel: 612 638 1888. Fax: 612 638 1798.
AUSTRIA	**Moor Lackner GmbH,** Lamezanstrasse 10, A-1230 Wien Tel: 222 610620. Tx: 135701. Fax: 222 61062151.
BELGIUM	**Heynen,** De Koelen 6, B-3530 Koutmalen. Tel: 011/52 57 57. Tx: 39047. Fax: 011/52 57 77. **Tekelec Airtronic NV,** Bergensesteenweg 501, B-1500 Halle. Tel: 02 362 1288 Fax: 02 360 3807
FRANCE	**Mateleco:** **Ile de France**, 66 Avenue Augustin Dumont, 92240 Malakoff. Tel: 010 33 1 46 57 70 55. Tx: 203436. **Rhône-Alpes**, 2, Rue Emile Zola, 38130 Echirolles. Tel: 010 33 76 40 38 33 Tx: 980837. **ICC:** **Bordeaux**, Rue de la Source, 33170 Gradignan. Tel: 56 31 17 17 Tx: 541539 Fax: 61 48 11 25. **Clermont-Ferrand**, 2 bis, Avenue Fonmaure, 63400 Chamalières. Tel: 73 36 71 41 Tx: 990928. **Marseille**, Z.A. Artizanord 11, 13015 Marseille. Tel: 91 03 12 12. Tx: 441313. **Toulouse**, 78, Chemin Lanusse, 31200 Toulouse. Tel: 61 26 14 10. Tx: 520897.

CGE Composants SA:
Ile de France-6, Avenue Maréchal-Juin - Z.I, Grange-Dame-Rose, 92363 Meudon La Forêt.
Tel: (1) 40 94 84 00. Tx: 632253. Fax: (1) 46 30 01 29.
Aquitaine, Avenue Gustave Eiffel, 33605 Pessac Cedex. Tel: 56 36 40 40. Tx: 571224 F.
Bretagne-9, Rue du Général Nicolet, 35015 Rennes Cedex. Tel: 99 50 40 40 Tx: 740311 F.
Centre/Pays-de-Loire, Allée de la Détente, 86360 Chasseneuil du Poitou. Tel: 49 52 88 88. Tx: 791525 F.
Est-27, Rue Kleber, 68000 Colmar. Tel: 89 41 15 43. Tx: 870569 F.
Midi-Pyrénées, 55, Avenue Louis Breguet, 31400 Toulouse. Tel: 61 20 82 38. Tx: 530957 F.
Nord, 2 Rue de la Créativité, 59650 Villeneuve-d'Ascq. Tel: 20 67 04 04. Tx: 136887 F.
Provence/Cote d'Azur, Avenue Donadei, Bat.B-06700 Staint. Laurent-du-Var. Tel: 93 07 77 67. Tx: 461481 F.
Rhône-Alpes, 101, Rue Dedieu, 69100 Villeurbanne. Tel: 78 68 32 29. Tx: 305301 F.
Aquitech:
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Astronic GmbH, Gruenwalderweg 30, 8024 Deisenhofen. Tel: 089 6130303. Tx: 5216187. Fax: 089 6131668.
Micronetics GmbH, Weil de Staedter Str. 45, 7253 Renningen 1. Tel: 071 59 6019. Tx: 724708. Fax: 071 59 5119.
Weisbauer Elektronik GmbH, Heiliger Weg 1, 4600 Dortmund 1. Tel: 0231 57 95 47. Tx: 822538. Fax: 0231 57 75 14.

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Con Systems SRL, Via Gramsci 156, 20037 Padereno Dugnano, Milano. Tel: 02 99 04 19 77 Fax: 02 99 04 1981.
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Eurelettronica SpA, Via E. Fermi 8, 20090 Assago Milan. Tel: 2 4880022. Tlx: 350037. Fax: 2 4880275.
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Tel: 0279 626777. Tlx: 818801. Fax: 0279 441687.
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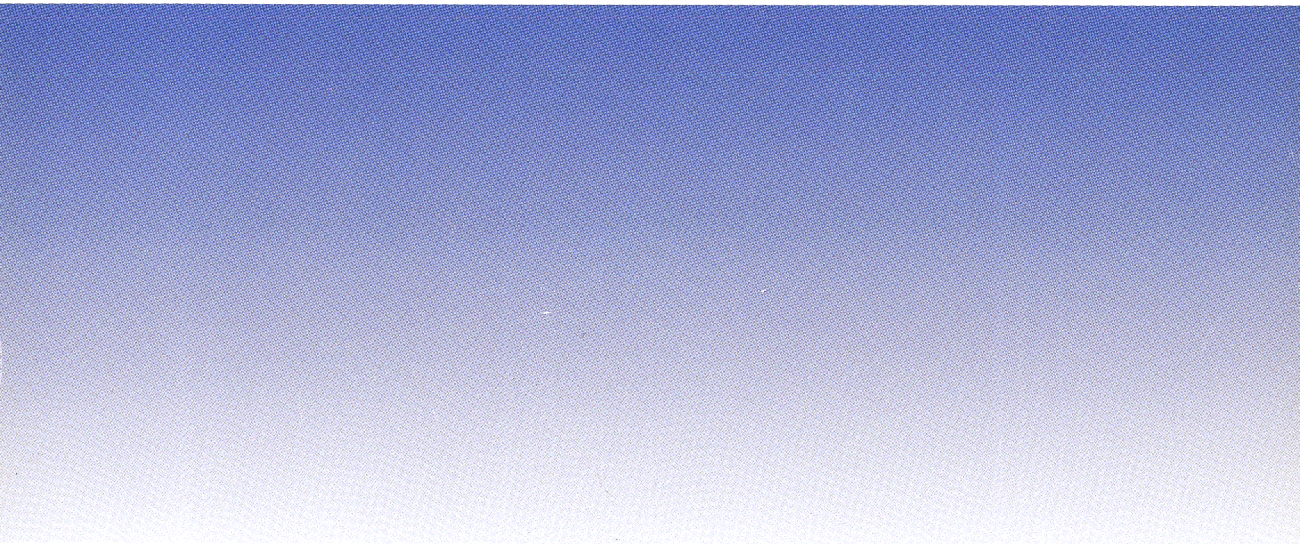

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Marconi Electronic Devices Limited and Plessey Semiconductors Limited have been grouped together to form GEC Plessey Semiconductors.

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